HARRIS Semiconductor

HC6094

OBSOLETE PRODUCT
NO RECOMMENDED REPLACEMENT
Call Central Applications 1-800-442-7747
or email: centapp@harris.com

February 1999

ADSL Analog Front End Chip

Features

- **14-Bit 5 MSPS DAC**
- **Programmable Gain Stages**
- **Anti-Aliasing and Reconstruction Filters**

Applications

- **FDM DMT ADSL**
- **CAP ADSL**
- **EC DMT ADSL**
- **Communications Receiver**

Description

The HC6094 performs the Analog processing for the ADSL chip set. The transmit chain has a 14 Bit DAC, a third-order Chebyshev reconstruction filter and a programmable attenuator (-12 to 0dB) capable of driving a 220Ω differential load. The receiver chain has a high impedance input stage, programmable gain stage (0 to 24dB), additional programmable gain (-9 to 18dB) and a third-order Chebyshev anti-aliasing filter for driving an off-chip A/D.

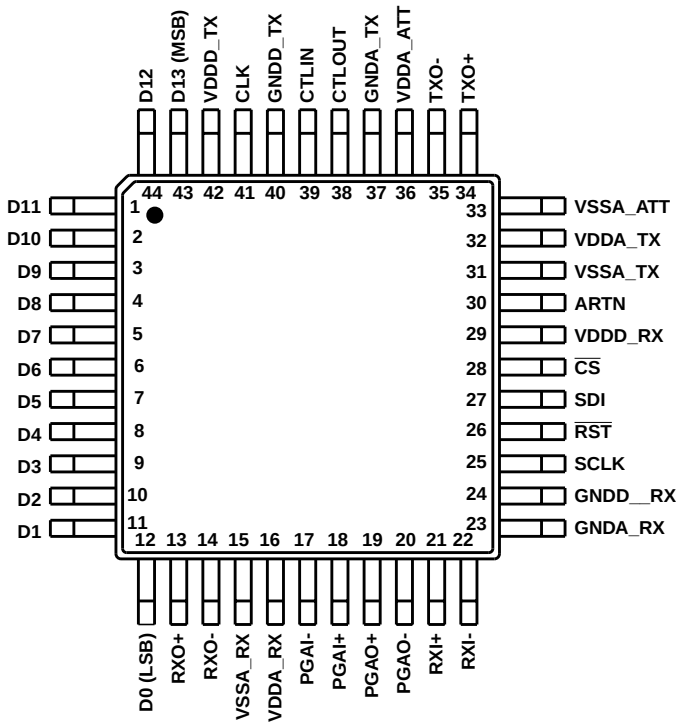
Laser trimmable thin-film resistors are used to set the filter cutoff frequency and DAC linearity. The transmit and receive signal chains are specified at 65dB MTPR.

Ordering Information

PART NUMBER	TEMP. RANGE (^{O}C)	PACKAGE	PKG. NO.
HC6094IN	-40 to 85	44 Ld MQFP	Q44.10x10

Pinout

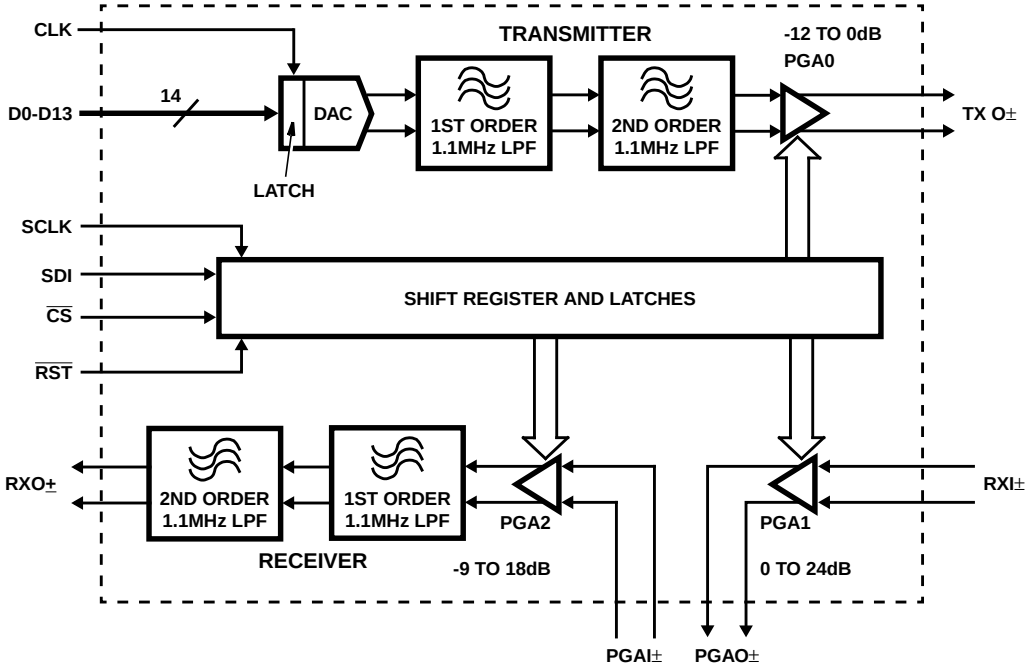
HC6094
(MQFP)
TOP VIEW



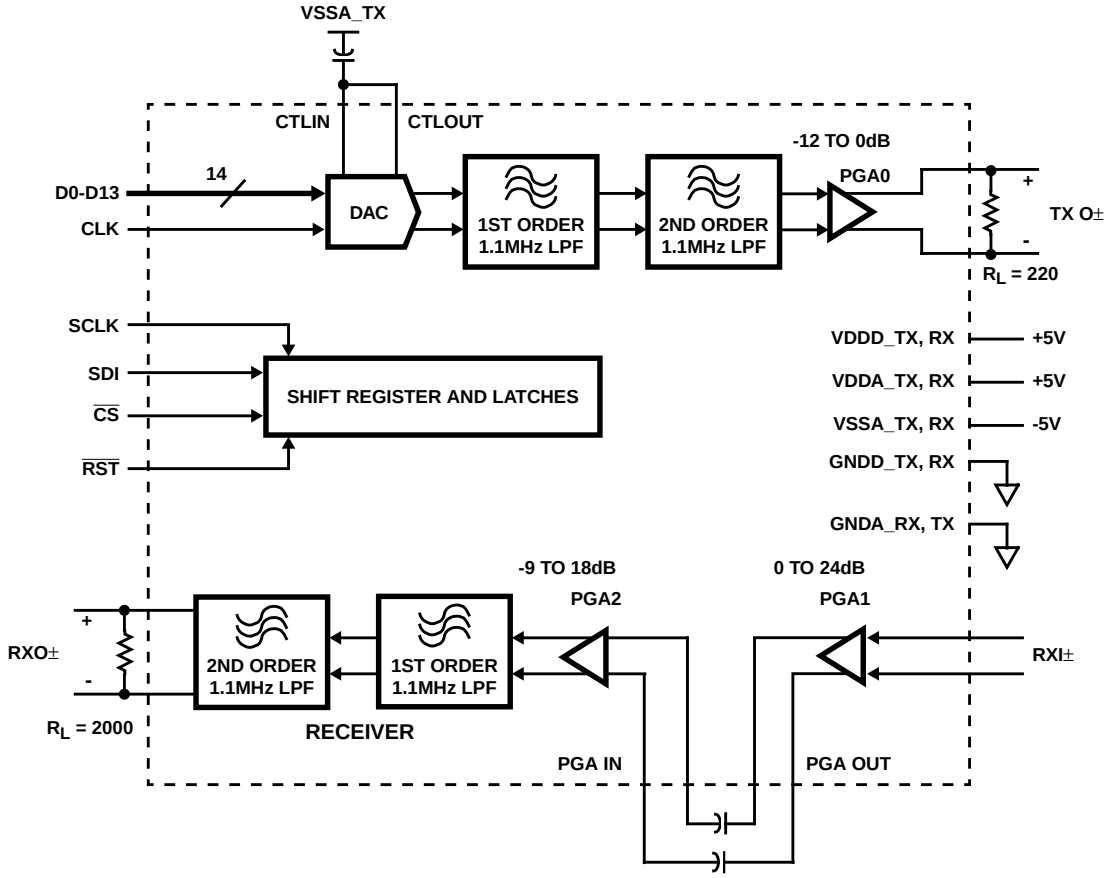
CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

File Number **4260.2**

Functional Block Diagram



Typical Setup



Absolute Maximum Ratings $T_A = 25^oC$

Supply Pins . . . . . ±5.5V
Analog Input Voltage to Ground . . . . . V_{DD} +0.5, V_{SS} -0.5V
Digital Input Voltage to Ground. . . . . V_{DD} +0.5V, -0.5V

Operating Conditions

Temperature Range . . . . . -40^oC to 85^oC

Thermal Information

Thermal Resistance (Typical, Note 1) θ_{JA} ($^oC/W$)
MQFP 55
Maximum Power Dissipation. 1.18W
Maximum Junction Temperature (T_J) . . . . . 150^oC
Maximum Storage Temperature Range . . . . . -65^oC to 150^oC
Maximum Lead Temperature (Soldering 10s) . . . . . 300^oC
(Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

V_{DD} = 5V, V_{SS} = -5V, R_L Open, Over Temperature Range; Unless Otherwise Specified. Designed for ±5% Power Supply.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
OVERALL						
Supply Currents	I_{DD}	V_{DD} (Note 2)	-	66	-	mA
	I_{SS}	V_{SS} (Note 3)	-	-79	-	mA
	I_{CC}	V_{CC}	-	0	-	µA
Power Dissipation	PD	Quiescent, No Load	-	725	-	mW
DIGITAL INTERFACE						
Input Voltage Thresholds	V_{IL}		-	-	0.8	V
	V_{IH}		2.7	-	-	V
Input Currents	I_{IL}	V_{IN} = 0V	-10.0	0	10.0	µA
	I_{IH}	V_{IN} = V_{DD}	-10.0	0	10.0	µA
Serial Clock Period	T1		0.1	-	5.0	µs
CS Active Before Shift Edge	T2		T1/2 -10	-	-	ns
Write Data Valid After Shift Edge	T3		-	-	10	ns
CS Inactive After Latch Edge	T4		T1 - 10	-	T1 +10	ns
Write Data Hold After Latch Edge	T5		T1/2 -5	-	T1/2 +5	ns
DAC Setup Time	t_S		-	-	100	ns
DAC Hold Time	t_H		-	-	100	ns
14-BIT DAC						
Resolution/Monotonicity			14	-	-	Bits
Integral Linearity	I_{LE}	Measured at T_X Outputs	-	±1.5	-	LSB
Differential Linearity	D_{LE}		-	±0.9	-	LSB
Max Sample Rate			4.416	-	-	Ms/s
TRANSMITTER OUTPUT						
Output Drive	TXOD	Sink or Source	30	55	-	mA
Differential Output Swing	TXOS	R_L = 220Ω	11.7	12.03	12.3	V_{PP}
Differential Balance	TXDB	Gain Match Between Outputs	-	0.5	-	%
Transmit Output Offset	TXOFF	Max Gain Single Ended (Note 4)	-200	25	200	mV
Multi-Tone Power Ratio	TXMTPR	R_L = 220Ω	-	65	-	dB
Power Supply Rejection	PSRR	Input Referred - V_{DD}	40	65	-	dB
		Input Referred - V_{SS}	55	84	-	dB

Electrical Specifications V_{DD} = 5V, V_{SS} = -5V, R_L Open, Over Temperature Range; Unless Otherwise Specified. Designed for ±5% Power Supply. **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
TRANSMITTER GAIN STAGE						
Gain Error	TXPG	R_L = 220Ω, 0dB Setting	-0.22	±0.02	0.22	dB
		R_L= 220Ω, Each Step Relative to 0dB	-0.15	0.02	0.15	dB
TRANSMITTER FREQUENCY RESPONSE						
Gain Ripple Peak to Peak	GP	Across 1.104MHz Bandwidth	-	0.2	0.6	dB
Stopband Attenuation	GS	At 2.65MHz	14	17	-	dB
Floor Attenuation	GM	At 9.94MHz	-	58	-	dB
RECEIVER INPUT (PGA1 AND PGA2)						
Input Swing	RXIS	Differential	-	-	12	V_{PP}
Input Impedance	RXRIN	PGA1	1.0		-	MΩ
		PGA2	1.0	12	-	kΩ
Common Mode Rejection	RXCMRR	1.1MHz	-	90	-	dB
Common Mode Range	RXCMIR		-0.25	-	0.25	V
Continuous Input Voltage			V_{SS}-0.5		V_{DD} +0.5	V
RECEIVER OUTPUT (INCLUDING PGA1 OUT)						
Differential Output Swing	RXOS	RX_{OUT} (R_L = 2000Ω)	12.0	15.8	-	V_{PP}
		$PGA1_{OUT}$ (R_L = 2000Ω)	12.0	16.0	-	V_{PP}
Differential Balance	RXDB	End to End (RX_{IN} to RX_{OUT})	-	0.5	-	%
PGA1 Output Offset	RXOFF	Max Gain Single Ended (Note 4)	-200	40	200	mV
PGA2 Output Offset	RXOFF	Max Gain Single Ended (Note 4)	-200	30	200	mV
Multi-Tone Power Ratio	RXMTPR	R_L = 2000Ω	-	65	-	dB
Power Supply Rejection	PSRR	Input Referred - V_{DD}	45	69	-	dB
		Input Referred - V_{SS}	55	84	-	dB
RECEIVER GAIN STAGE						
Absolute Gain Error	RXPG	Any Step (RX_{IN} to RX_{OUT})	-0.3	0.01	0.3	dB
RECEIVER FREQUENCY RESPONSE						
Gain Ripple Peak to Peak	GP	Across 1.104MHz Bandwidth	-	0.4	0.6	dB
Stopband Attenuation	GS	At 2.65MHz	14	19.4	-	dB
Floor Attenuation	GM	At 9.94MHz	-	53	-	dB
TRANSMITTER AND RECEIVER FILTER CUTOFF FREQUENCY						
TX Filter F_C	TX_{FC}	-0.15dB point	1.104	1.18	1.25	MHz
RX Filter F_C	RX_{FC}	-0.15dB point	1.104	1.125	1.16	MHz

NOTES:

2. V_{DD} = 5V typical, supply range ±5%.
3. V_{SS} = -5V typical, supply range ±5%.
4. Single ended operation for reference only. Probed to these limits, but not packaged tested.

Definitions

1. Supply currents/power dissipation measured in a quiescent (static) state with R_L open.
2. Logic input levels and timing are verified by using them as conditions for testing DAC and filter.
3. Digital input currents are measured at 0V and V_{CC}.
4. DAC resolution and monotonicity guaranteed by ILE and DLE tests.
5. DAC ILE is relative to best fit straight line.
6. Output drive current is the output current at 0V for each output when they are driven to ± Full Scale.
7. Output offset measured with V_{IN} = 0V differential for the R_X, and the DAC at mid scale for the T_X.
8. PSRR is the change in differential input voltage vs. change in supply voltage at DC.
9. T_X Gain is calculated as $20*Log((TXout_{DACFS} - TXout_{DACZS})/12V)$ at DC.
10. R_X input swing is verified by using this as condition for gain testing.
11. R_X Input Impedance is calculated as $\Delta V_{IN}/\Delta I_{IN}$ where V_{IN} is the maximum input voltages, with the PGA set to 0dB.
12. R_X CMRR is calculated as $20*Log(V_{OUT}/V_{IN})$-PGA Gain. V_{IN} is set to 250mV_{PEAK} (CMIR) at 1.1MHz, and PGA gain is set to maximum.
13. R_X Gain is calculated as $20*Log(dV_{OUT}/dV_{IN})$, where V_{IN} is set to give a nominal ± Output Swing, or the maximum input swing, whichever is smaller. It is tested DC.
14. Filter Gain/Attenuation is relative to low frequency passband gain. T_X tested by driving the DAC (with sinX/X correction), R_X tested by driving PGA2. Wafer probe will use special test points to bypass the DAC for laser trimming.
15. MTPR - (Multi-Tone Power Ratio). A DMT waveform is generated which has a specific crest factor or peak to average ratio (PAR) with specific carriers missing. The waveform is then passed through the T_X or R_X chain. The total integrated power of the notch at the location of the missing carriers is measured with respect to the adjacent carriers. Notch depth is measured for several DMT waveforms with different PARs. The notch depths for each DMT waveform are averaged to give an MTPR number.

Shift Register Format

Each write operation to a control register involves 16 bits of data. The CS- signal must be enabled low during any serial write operation. The data on SDI shall be clocked in during the rising edge of SCLK. A3-A0 supply the address of the control register, and D7-D0 supply the data.

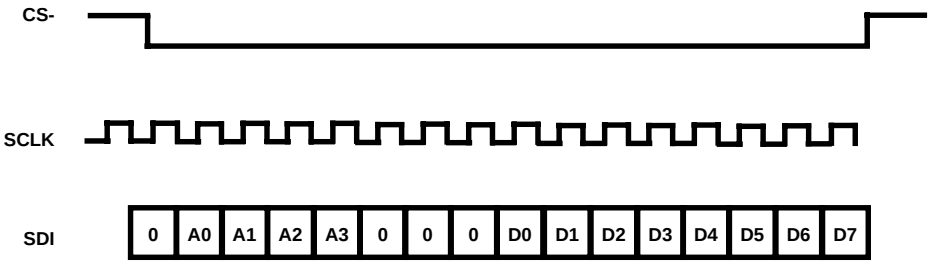


FIGURE 1. SERIAL CONTROL

Logic Timing Definitions

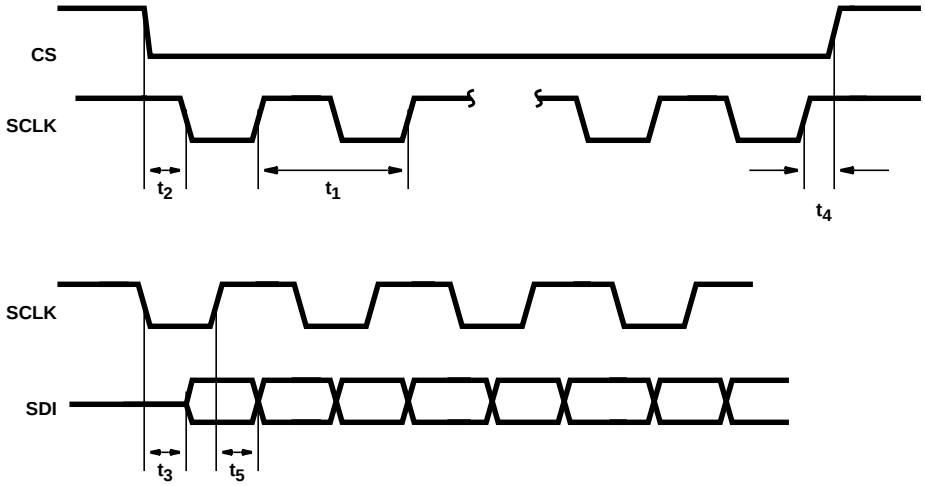


FIGURE 2. SERIAL INTERFACE

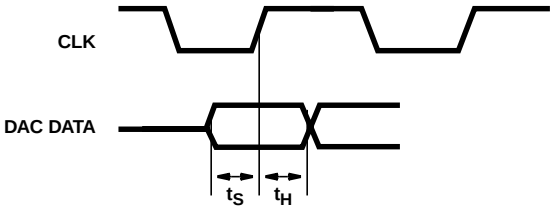


FIGURE 3. DAC INTERFACE

Shift Registers Format

REGISTER	A0	A1	A2	A3	D0	D1	D2	D3	D4	D5	D6	D7
RX Gain	1	0	X	X	PGA1 Gain				PGA2 Gain			
TX Gain	0	0	X	X	PGA0 Gain							

TX PGA0 GAIN

D2	D1	D0	GAIN IN dB
1	1	X	-12
1	0	1	-10
1	0	0	-8
0	1	1	-6
0	1	0	-4
0	0	1	-2
0	0	0	0

RX PGA1 GAIN

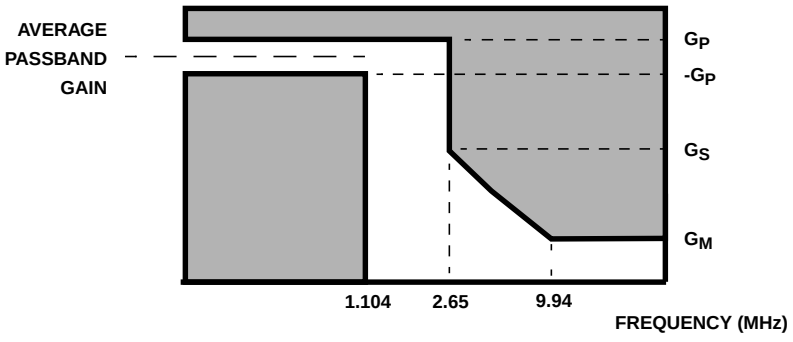
D3	D2	D1	D0	GAIN IN dB
0	0	0	0	0
0	0	0	1	3
0	0	1	0	6
0	0	1	1	9
0	1	0	0	12
0	1	0	1	15
0	1	1	0	18
0	1	1	1	21
1	X	X	X	24

NOTE: PGA1 is an inverting amplifier.

RX PGA2 GAIN

D7	D6	D5	D4	GAIN IN dB
0	0	0	0	-9
0	0	0	1	-6
0	0	1	0	-3
0	0	1	1	0
0	1	0	0	3
0	1	0	1	6
0	1	1	0	9
0	1	1	1	12
1	X	X	0	15
1	X	X	1	18

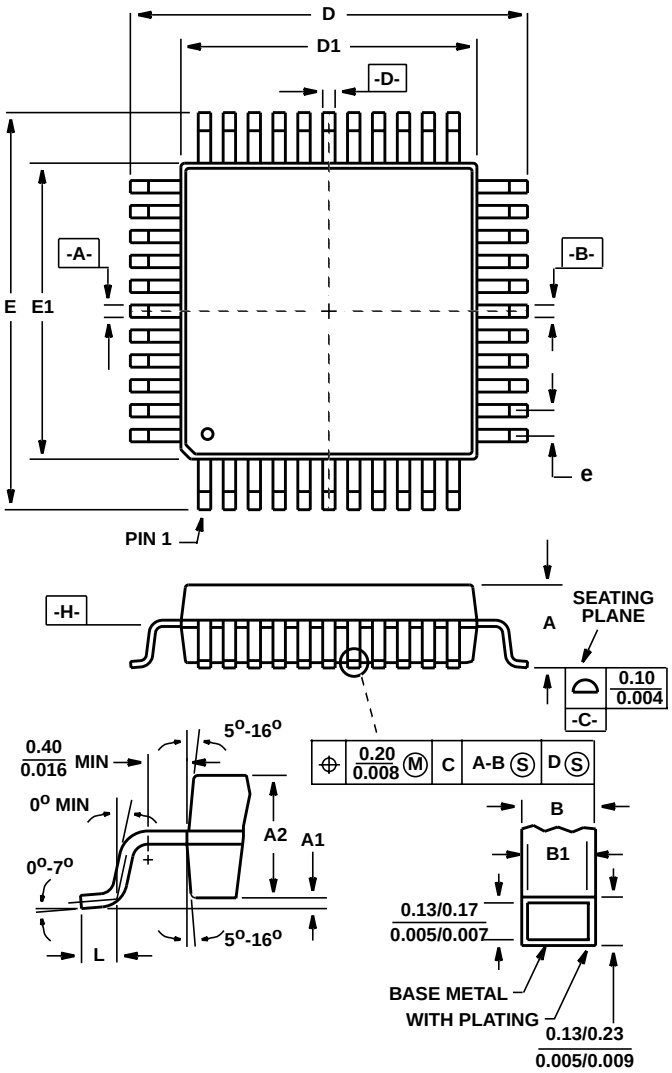
Filter Mask Template



Pin Descriptions

PIN NUMBER	PIN NAME	PIN DESCRIPTION
43, 44	D13-D12	Digital Input bits 13 and 12. D13 is MSB.
1-12	D11-D0	Digital Input bits 11 thru 0. D0 is LSB.
13, 14	RXO±	Receiver differential outputs.
15	VSSA_RX	Receiver -5V supply.
16	VDDA_RX	Receiver +5V supply.
17, 18	PGAI±	PGA2 differential inputs.
19, 20	PGAO±	PGA1 differential outputs.
21, 22	RXI±	Receiver differential inputs (PGA1 inputs).
23	GNDA_RX	Receiver ground.
24	GNDD_RX	Serial interface ground.
25	SCLK	Serial interface clock pin.
26	$\overline{RST}$	Serial interface reset pin.
27	SDI	Serial interface data input.
28	$\overline{CS}$	Serial interface chip select.
29	VDDD_RX	Shift register Digital +5V supply.
30	ARTN	Analog return (ground).
31	VSSA_TX	Transmitter -5V supply.
32	VDDA_TX	Transmitter +5V supply.
33	VSSA_ATT	Attenuator -5V supply.
34, 35	TXO±	Transmitter differential outputs.
36	VDDA_ATT	Attenuator +5V supply.
37	GNDA_TX	Analog ground for transmitter.
38	CTLOUT	Control Amplifier Output. Provides precision control of the current sources. Typically connected to CTLIN.
39	CTLIN	Input to the Current Source Base Rail. Typically connected to CTLOUT. Requires a 0.1µF capacitor to VSSA_TX. Allows external decoupling of the current sources.
40	GNDD_TX	Digital Ground.
41	CLK	DAC input latch clock.
42	VDDD_TX	DAC digital +5V supply.

Metric Plastic Quad Flatpack Packages (MQFP/PQFP)



Q44.10x10 (JEDEC MO-108AA-2 ISSUE A)
44 LEAD METRIC PLASTIC QUAD FLATPACK PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.093	-	2.35	-
A1	0.004	0.010	0.10	0.25	-
A2	0.077	0.083	1.95	2.10	-
B	0.012	0.018	0.30	0.45	6
B1	0.012	0.016	0.30	0.40	-
D	0.510	0.530	12.95	13.45	3
D1	0.390	0.398	9.90	10.10	4, 5
E	0.510	0.530	12.95	13.45	3
E1	0.390	0.398	9.90	10.10	4, 5
L	0.026	0.037	0.65	0.95	-
N	44		44		7
e	0.032 BSC		0.80 BSC		-

Rev. 1 1/94

NOTES:

1. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.
2. All dimensions and tolerances per ANSI Y14.5M-1982.
3. Dimensions D and E to be determined at seating plane -C-.
4. Dimensions D1 and E1 to be determined at datum plane -H-.
5. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25mm (0.010 inch) per side.
6. Dimension B does not include dambar protrusion. Allowable dambar protrusion shall be 0.08mm (0.003 inch) total.
7. “N” is the number of terminal positions.