MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MC9S12H-Family

Product Proposal

16-Bit Microcontroller

All MC9S12H-Family member microcontroller units (MCU) are 16-bit devices composed of standard on-chip peripherals including a 16-bit central processing unit (CPU12), up to 256K bytes of Flash EEPROM, 12K bytes of RAM, 4K bytes of EEPROM, one or two asynchronous serial communications interfaces (SCI), a serial peripheral interface (SPI), an IIC-bus interface (IIC), an 8-channel 16-bit timer (TIM), a 16-channel, 10-bit analog-to-digital converter (ADC), up to six-channel pulse width modulator (PWM), and up to two CAN 2.0 A, B software compatible modules (MSCAN12). In addition, they feature a 28x4 or 32x4 liquid crystal display (LCD) controller/driver and a motor pulse width modulator (PWM) consisting of 24 high current outputs suited to drive up to 6 stepper motors. System resource mapping, clock generation, interrupt control, and bus interfacing are managed by the system integration module. The MC9S12H-Family has full 16-bit data paths throughout. The inclusion of a PLL circuit allows power consumption and performance to be adjusted to suit operational requirements. In addition to the I/O ports available in each module, up to 14 I/O ports are available with Key-Wake-Up capability from STOP or WAIT mode.

Features

NOTE: Not all features listed here are available in all configurations!

- **16-bit CPU12**
  - — Upward compatible with M68HC11 instruction set
  - — Interrupt stacking and programmer's model identical to M68HC11
  - — Instruction queue
  - — Enhanced indexed addressing
- **8-bit and 4-bit ports with Key Wake-Up Interrupt**
  - — Digital filtering
  - — Programmable rising or falling edge trigger
- **Memory options**
  - — 128K, 256K Flash EEPROM
  - — 2K, 4K byte EEPROM
  - — 6K, 12K byte RAM
- **Analog-to-Digital Converter**
  - — 8 or 16 channels, 10-bit resolution
  - — External conversion trigger capability
- **One or two 1M bit per second, CAN 2.0 A, B software compatible modules**
  - — Five receive and three transmit buffers
  - — Flexible identifier filter programmable as 2 x 32 bit, 4 x 16 bit or 8 x 8 bit
  - — Four separate interrupt channels for Rx, Tx, error and wake-up
  - — Low-pass filter wake-up function
  - — Loop-back for self test operation

This document contains information on a new product. Specifications and information herein are subject to change without notice.

- **Timer**
  - — 16-bit main counter with 7-bit prescaler
  - — 8 programmable input capture or output compare channels
  - — Two 8-bit or one 16-bit pulse accumulators
- **2 or 6 PWM channels depending on the package option**
  - — Programmable period and duty cycle
  - — 8-bit 6-channel or 16-bit 3-channel
  - — 8-bit 2 channel or 16-bit 1 channel
  - — Separate control for each pulse width and duty cycle
  - — Center-aligned or left-aligned outputs
  - — Programmable clock select logic with a wide range of frequencies
- **Serial interfaces**
  - — One or two asynchronous Serial Communications Interfaces (SCI)
  - — Synchronous Serial Peripheral Interface (SPI)
  - — Inter-Integrated Circuit interface (IIC) 144LQFP
- **Liquid Crystal Display driver with variable input voltage**
  - — Configurable for up to 32 frontplanes and 4 backplanes or general purpose input or output
  - — 5 modes of operation allow for different display sizes to meet application requirements
  - — Unused frontplane and backplane pins can be used as general purpose I/O
- **24 high current drivers suited for PWM motor control**
  - — 12 PWM channels with common frequency timebase
  - — Each PWM channel switchable between two drivers in an H-bridge configuration
  - — left, right and center aligned outputs
  - — Support for sin and cos drive
  - — Dithering
  - — Output slew rate limitation
- **SIM (System Integration Module)**
  - — CRG (windowed COP watchdog, real time interrupt, clock monitor, clock generation and reset)
  - — MEBI (multiplexed external bus interface)
  - — MMC (memory map and interface)
  - — INT (interrupt control)
  - — BKP (breakpoints)
  - — BDM (background debug mode)
- **Clock generation**
  - — Phase-locked loop clock frequency multiplier
  - — self clock mode in absence of external clock
  - — Low power 0.5 to 16MHz crystal oscillator reference clock
- **144-Pin or 112-Pin QFP package**
  - — I/O lines with 5V input and drive capability
  - — 5V A/D converter inputs
  - — Operation at 32MHz equivalent to 16MHz Bus Speed
  - — Development support
  - — Single-wire background debug™ mode (BDM)
  - — On-chip hardware breakpoints

Table 1 List of MC9S12H-Family members

Flash	RAM	EEPROM	Package	Device	CAN	SCI	SPI	IIC	A/D	PWM	LCD	Motor	I/O
256K	12K	4K	144LQFP	H256	2	2	1	1	16	6	32x4	24/6	93
			112LQFP	H256	2	1	1	0	8	2	28x4	24/6	61
128K	6K	2K	112LQFP	H128	2	1	1	0	8	2	28x4	24/6	61

- **Pin out explanations:**
  - — A/D is the number of A/D channels.
  - — Motor denotes the number of high current drive pins/number of stepper motors which can be driven
  - — I/O is the sum of ports capable to act as digital input or output.

    144 Pin Packages:

    Port A = 8, B = 8, E = 6 + 2 input only, H = 8, J = 4, K = 5, L=8, M = 6, P = 6, S = 8, T = 8, PAD = 16 input only.

    14 inputs provide Interrupt capability (H = 8, J = 4, IRQ, XIRQ)

    112 Pin Packages:

    Port A = 8, B = 8, E = 6 + 2 input only, K=5, L=4, M = 4, P = 2, S = 6, T = 8, PAD = 8 input only.

    2 inputs provide Interrupt capability (IRQ, XIRQ)

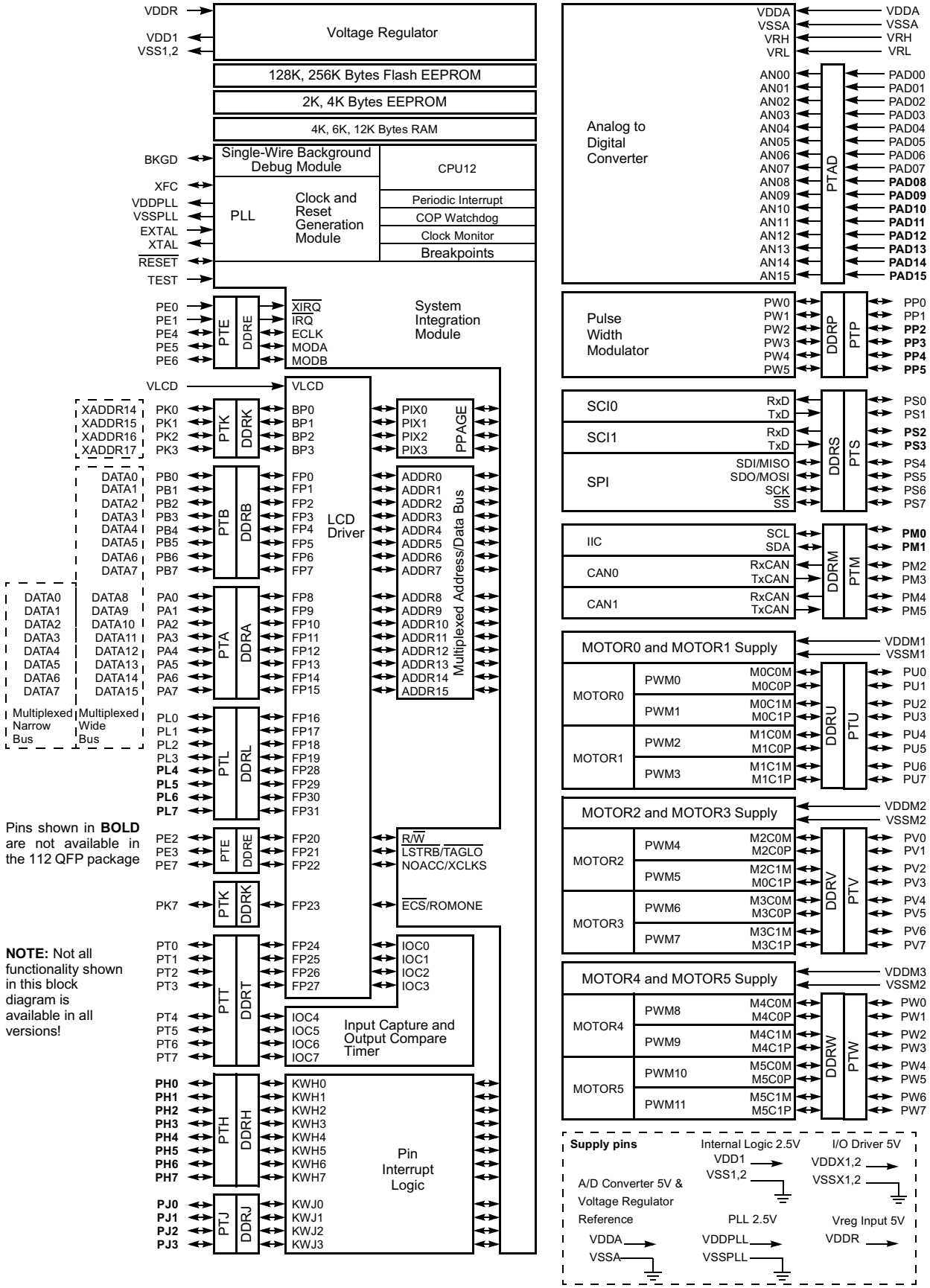


Figure 1. MC9S12H-Family Block Diagram

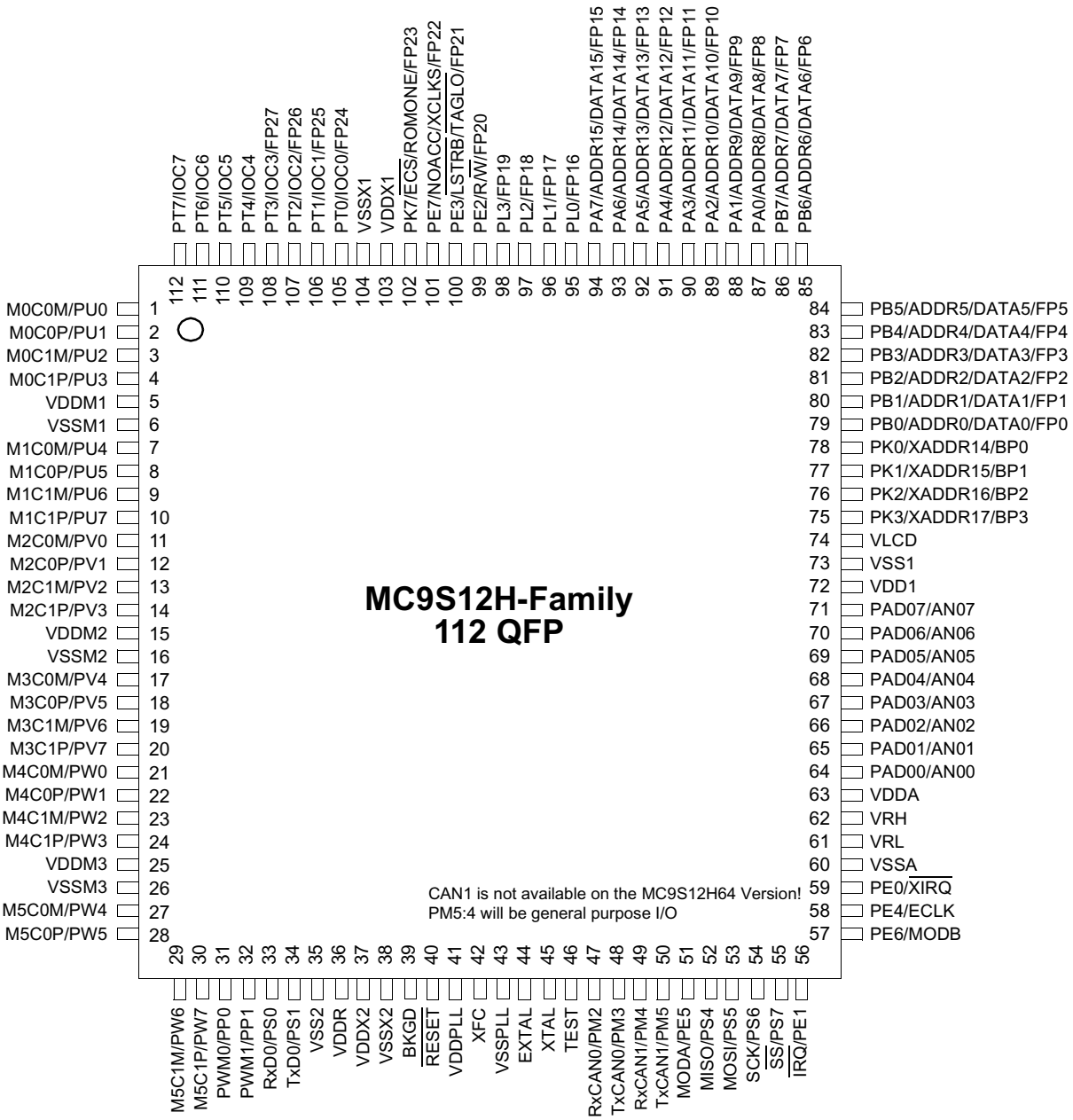


Figure 2. MC9S12H-Family Pin Assignments, 112 pin QFP package

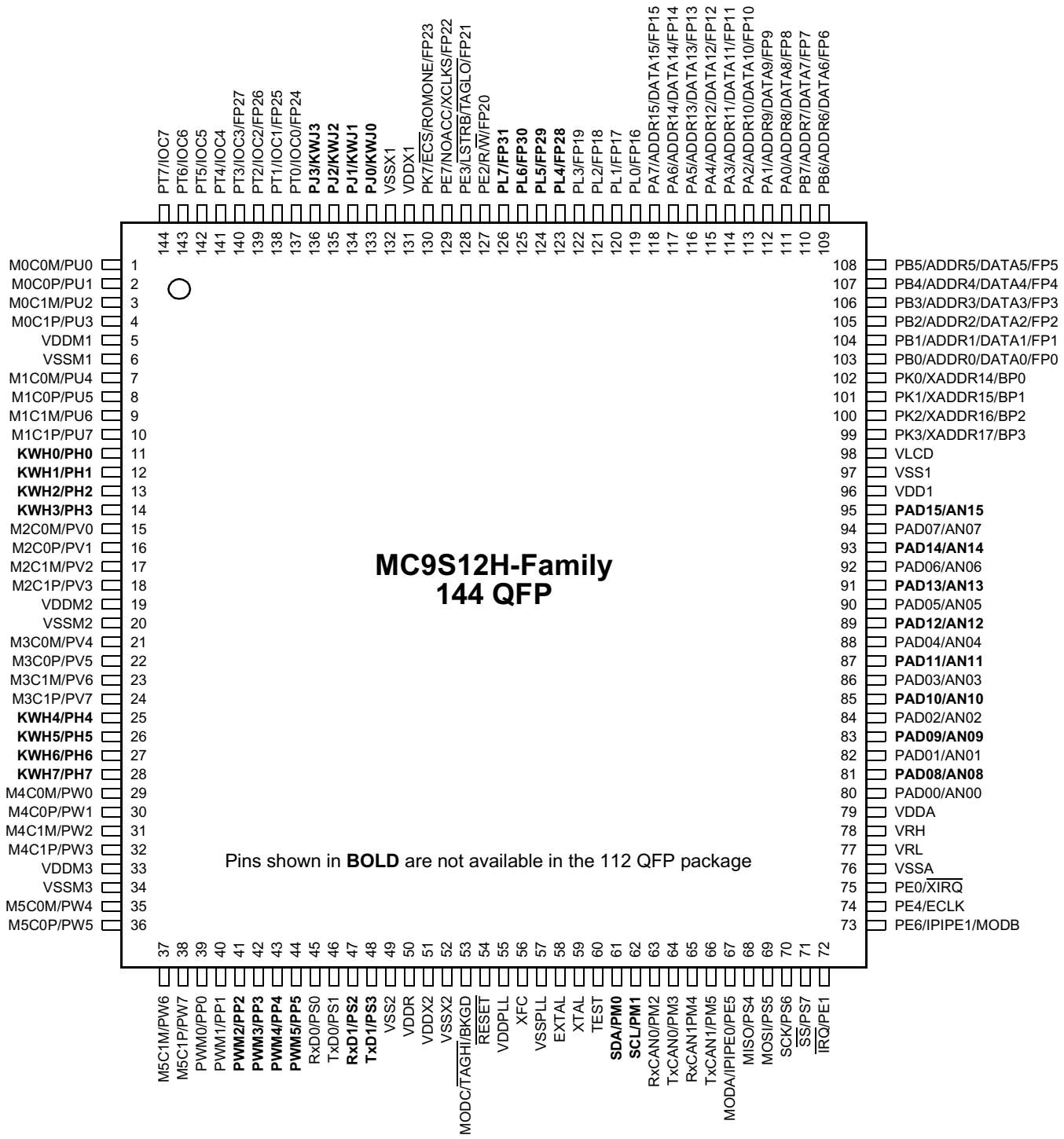


Figure 3. MC9S12H-Family Pin Assignments, 144 Pin QFP package

Table 1. Pin Descriptions

Note: Features shown in bold are not available in the 112 pin QFP package.

Pin Name Function 1	Pin Name Function 2	Pin Name Function 3	Description
PU[3:0]	M0C0M, M0C0P, M0C1M, M0C1P	—	Function 1: General purpose input/output pins. Function 2: High current PWM output pins which can be used for motor drive. These pins interface to the coils of motor 0. PWM output on M0C0M results in a positive current flow through coil 0 when M0C0P is driven to a logic high state. PWM output on M0C1M results in a positive current flow through coil 1 when M0C1P is driven to a logic high state.
VDDM1, VSSM1	—	—	Supply input pins for motor 0 and motor 1 output drivers. Tolerance = 5 V ± 10%.
PU[7:4]	M1C0M, M1C0P, M1C1M, M1C1P	—	Function 1: General purpose input or output pin. Function 2: High current PWM output pins which can be used for motor drive. These pins interface to the coils of motor 1. PWM output on M1C0M results in a positive current flow through coil 0 when M1C0P is driven to a logic high state. PWM output on M1C1M results in a positive current flow through coil 1 when M1C1P is driven to a logic high state.
PH[3:0]	**KWH[3:0]**	—	**Function 1: General purpose input or output pin. Function 2: Key wake-up interrupt pin. When configured as an input, can generate an interrupt causing the MCU to exit STOP or WAIT mode.**
PV[3:0]	M2C0M, M2C0P, M2C1M, M2C1P	—	Function 1: General purpose input or output pin. Function 2: High current PWM output pins which can be used for motor drive. These pins interface to the coils of motor 2. PWM output on M2C0M results in a positive current flow through coil 0 when M2C0P is driven to a logic high state. PWM output on M2C1M results in a positive current flow through coil 1 when M2C1P is driven to a logic high state.
VDDM2, VSSM2	—	—	Supply input pins for motor 2 and motor 3 output drivers. Tolerance = 5 V ± 10%.
PV[7:4]	M3C0M, M3C0P, M3C1M, M3C1P	—	Function 1: General purpose input or output pin. Function 2: High current PWM output pins which can be used for motor drive. These pins interface to the coils of motor 3. PWM output on M3C0M results in a positive current flow through coil 0 when M3C0P is driven to a logic high state. PWM output on M3C1M results in a positive current flow through coil 1 when M3C1P is driven to a logic high state.
PH[7:4]	**KWH[7:4]**	—	**Function 1: General purpose input or output pin. Function 2: Key wake-up interrupt pin. When configured as an input, can generate an interrupt causing the MCU to exit STOP or WAIT mode.**
PW[3:0]	M4C0M, M4C0P, M4C1M, M4C1P	—	Function 1: General purpose input or output pin. Function 2: High current PWM output pins which can be used for motor drive. These pins interface to the coils of motor 4. PWM output on M4C0M results in a positive current flow through coil 0 when M4C0P is driven to a logic high state. PWM output on M4C1M results in a positive current flow through coil 1 when M4C1P is driven to a logic high state.
VDDM3, VSSM3	—	—	Supply input pins for motor 4 and motor 5 output drivers. Tolerance = 5 V ± 10%
PW[7:4]	M5C0M, M5C0P, M5C1M, M5C1P	—	Function 1: General purpose input or output pin. Function 2: High current PWM output pins which can be used for motor drive. These pins interface to the coils of motor 5. PWM output on M5C0M results in a positive current flow through coil 0 when M5C0P is driven to a logic high state. PWM output on M5C1M results in a positive current flow through coil 1 when M5C1P is driven to a logic high state.

Table 1. Pin Descriptions

Note: Features shown in bold are not available in the 112 pin QFP package.

Pin Name Function 1	Pin Name Function 2	Pin Name Function 3	Description
PP[1:0]	PWM[1:0]	—	Function 1: General purpose input or output pin. Function 2: Pulse Width Modulator (PWM) channel output pin.
PP[5:2]	**PWM[5:2]**	—	**Function 1: General purpose input or output pin.** **Function 2: Pulse Width Modulator (PWM) channel output pin.**
PS[1:0]	TxD0, RxD0	—	Function 1: General purpose input or output pin. Function 2: RxD0 is the receive pin and TxD0 is the transmit pin of Serial Communication Interface 0 (SCI0).
PS[3:2]	**TxD1, RxD1**	—	**Function 1: General purpose input or output pin.** **Function 2: RxD1 is the receive pin and TxD1 is the transmit pin of Serial Communication Interface 1(SCI1).**
VSS2	—	—	Core ground.
VDDR	—	—	Power supply input pin for voltage regulator. Nominal 5V
BKGD	$\overline{\text{TAGHI}}$	MODC	Function 1: Pseudo-open-drain communication pin for the background debug function. Function 2: In MCU expanded modes of operation when instruction tagging is on, an input low on this pin during the falling edge of E-clock tags the high half of the instruction word being read into the instruction queue. Function 3: At the rising edge during reset, the state of this pin is latched to the MODC bit to set the MCU operating mode.
$\overline{\text{RESET}}$	—	—	An active low bidirectional control signal, it acts as an input to initialize the MCU to a known start-up state, and an output when an internal MCU function causes a reset.
VDDPLL, VSSPLL	—	—	PLL supply output pins. No load allowed except for bypass capacitors.
XFC	—	—	Dedicated pin used to create the PLL loop filter.
EXTAL, XTAL	—	—	Crystal driver and external clock input pins. On reset all the device clocks are derived from the EXTAL input frequency. XTAL is the crystal output.
TEST	—	—	Pin reserved for test.
PM[1:0]	**SCL, SDA**	—	**Function 1: General purpose input or output pin.** **Function 2: SDA is the serial data pin and SCL is the serial clock pin for the Inter-IC Bus Interface (IIC).**
PM[3:2]	TxCAN0, RxCAN0	—	Function 1: General purpose input or output pin. Function 2: RxCAN0 is the receive pin and TxCAN0 is the transmit pin for the Motorola Scalable Controller Area Network controller 0 (msCAN0).
PM[5:4]	TxCAN1, RxCAN1	—	Function 1: General purpose input or output pin. Function 2: RxCAN1 is the receive pin and TxCAN1 is the transmit pin for the Motorola Scalable Controller Area Network controller 1 (msCAN1). CAN1 is not available for the MC9S12H64 Version!
PE[6:5]	MODB, MODA	IPIPE1, IPIPE0	Function 1: General purpose input or output pin. Function 2: The state of the MODA and MODB pins during reset determine the initial operating mode of the MCU. Function 3: Instruction queue tracking signals.
PS4	MISO	—	Function 1: General purpose input or output pin. Function 2: Master input (during master mode) or slave output (during slave mode) pin for the Serial Peripheral Interface (SPI).

Table 1. Pin Descriptions

Note: Features shown in bold are not available in the 112 pin QFP package.

Pin Name Function 1	Pin Name Function 2	Pin Name Function 3	Description
PS5	MOSI	—	Function 1: General purpose input or output pin. Function 2: Master output (during master mode) or slave input (during slave mode) pin for the Serial Peripheral Interface (SPI).
PS6	SCK	—	Function 1: General purpose input or output pin. Function 2: Serial clock pin for the Serial Peripheral Interface (SPI).
PS7	$\overline{SS}$	—	Function 1: General purpose input or output pin. Function 2: Slave select pin for the Serial Peripheral Interface (SPI).
PE1	$\overline{IRQ}$	—	Function 1: General purpose input pin. Function 2: Maskable interrupt request input provides a means of applying asynchronous interrupt requests. Will wake up the MCU from STOP or WAIT mode.
PE4	ECLK	—	Function 1: General purpose input or output pin. Function 2: ECLK is the internal bus clock output. ECLK can be used as a timing reference.
PE0	$\overline{XIRQ}$	—	Function 1: General purpose input pin. Function 2: Nonmaskable interrupt request input provides a means of applying asynchronous interrupt requests. Will wake up the MCU from STOP or WAIT mode.
VRH, VRL	—	—	Reference voltage input pins for the analog to digital converter.
VDDA, VSSA	—	—	Supply input pins for the voltage regulator and the analog to digital converter. Tolerance = 5V ± 5%.
PAD[07:00]	AN[07:00]	—	Function 1: General purpose input pin. Function 2: Analog inputs for the analog to digital converter.
PAD[15:08]	**AN[15:08]**	—	**Function 1: General purpose input pin.** **Function 2: Analog inputs for the analog to digital converter.**
V_{DD1}, V_{SS1}	—	—	Core supply output pins. No load allowed except for bypass capacitors.
V_{LCD}	—	—	Supply input pin for the LCD driver. Adjusting the voltage on this pin will change the display contrast.
PK[3:0]	BP[3:0]	XADDR[17:14]	Function 1: General purpose input or output pin. Function 2: LCD backplane segment driver output pin. Function 3: In MCU expanded modes of operation, expanded address pins for the external bus.
PB[7:0]	FP[7:0]	ADDR[7:0]/ DATA[7:0]	Function 1: General purpose input or output pin. Function 2: LCD frontplane segment driver output pin. Function 3: In MCU expanded modes of operation, these pins are used for the multiplexed external address and data bus.
PA[7:0]	FP[15:8]	ADDR[15:8]/ DATA[15:8]	Function 1: General purpose input or output pin. Function 2: LCD frontplane segment driver output pin. Function 3: In MCU expanded modes of operation, these pins are used for the multiplexed external address and data bus.
PL[3:0]	FP[19:16]	—	Function 1: General purpose input or output pin. Function 2: LCD frontplane segment driver output pin.
PL[7:4]	**FP[31:28]**	—	**Function 1: General purpose input or output pin.** **Function 2: LCD frontplane segment driver output pin.**
PE2	FP20	R/$\overline{W}$	Function 1: General purpose input or output pin. Function 2: LCD frontplane segment driver output pin. Function 3: In MCU expanded modes of operations, performs the read/ write output signal for the external bus. This pin indicates direction of data on the external bus.

Table 1. Pin Descriptions

Note: Features shown in bold are not available in the 112 pin QFP package.

Pin Name Function 1	Pin Name Function 2	Pin Name Function 3	Description
PE3	FP21	$\overline{\text{LSTRB}}$/ $\overline{\text{TAGLO}}$	Function 1: General purpose input or output pin. Function 2: LCD frontplane segment driver output pin. Function 3: In MCU expanded modes of operation, $\overline{\text{LSTRB}}$ is used for the low-byte strobe function to indicate the type of bus access and when instruction tagging is on, $\overline{\text{TAGLO}}$ is used to tag the low half of the instruction word being read into the instruction queue.
PE7	FP22	NOACC/ XCLKS	Function 1: General purpose input or output pin. Function 2: LCD frontplane segment driver output pin. Function 3: The XCLKS signal selects between an external clock or oscillator configuration during reset. This pin should be at a logic high during reset if an external clock is used on the EXTAL input pin. This pin should be at a logic low during reset if an oscillator circuit is configured on EXTAL and XTAL. Since this pin is an input with a pull-down device during reset, if the pin is left floating, the default configuration is an oscillator circuit on EXTAL and XTAL. During MCU expanded modes of operation, the NOACC signal, when enabled, is used to indicate that the current bus cycle is an unused or “free” cycle. This signal will assert when the CPU is not using the bus.
PK7	FP23	$\overline{\text{ECS}}$/ ROMONE	Function 1: General purpose input or output pin. Function 2: LCD frontplane segment driver output pin. Function 3: During MCU expanded modes of operation, this pin is used to enable the Flash EEPROM memory in the memory map (ROMONE). Also during MCU expanded modes of operation, this pin is used as the emulation chip select signal ($\overline{\text{ECS}}$).
VDDX1,2, VSSX1,2	—	—	Supply input pins for input/output drivers. Tolerance = 5V ± 5%.
PJ[3:0]	**KWJ[3:0]**	—	**Function 1: General purpose input or output pin. Function 2: Key wake-up interrupt pin. When configured as an input, can generate an interrupt causing the MCU to exit STOP or WAIT mode.**
PT[3:0]	IOC[3:0]	FP[27:24]	Function 1: General purpose input or output pin. Function 2: Timer system input capture or output compare pin. Function 3: LCD frontplane segment driver output pin.
PT[7:4]	IOC[7:4]	—	Function 1: General purpose input or output pin. Function 2: Timer system input capture or output compare pin.

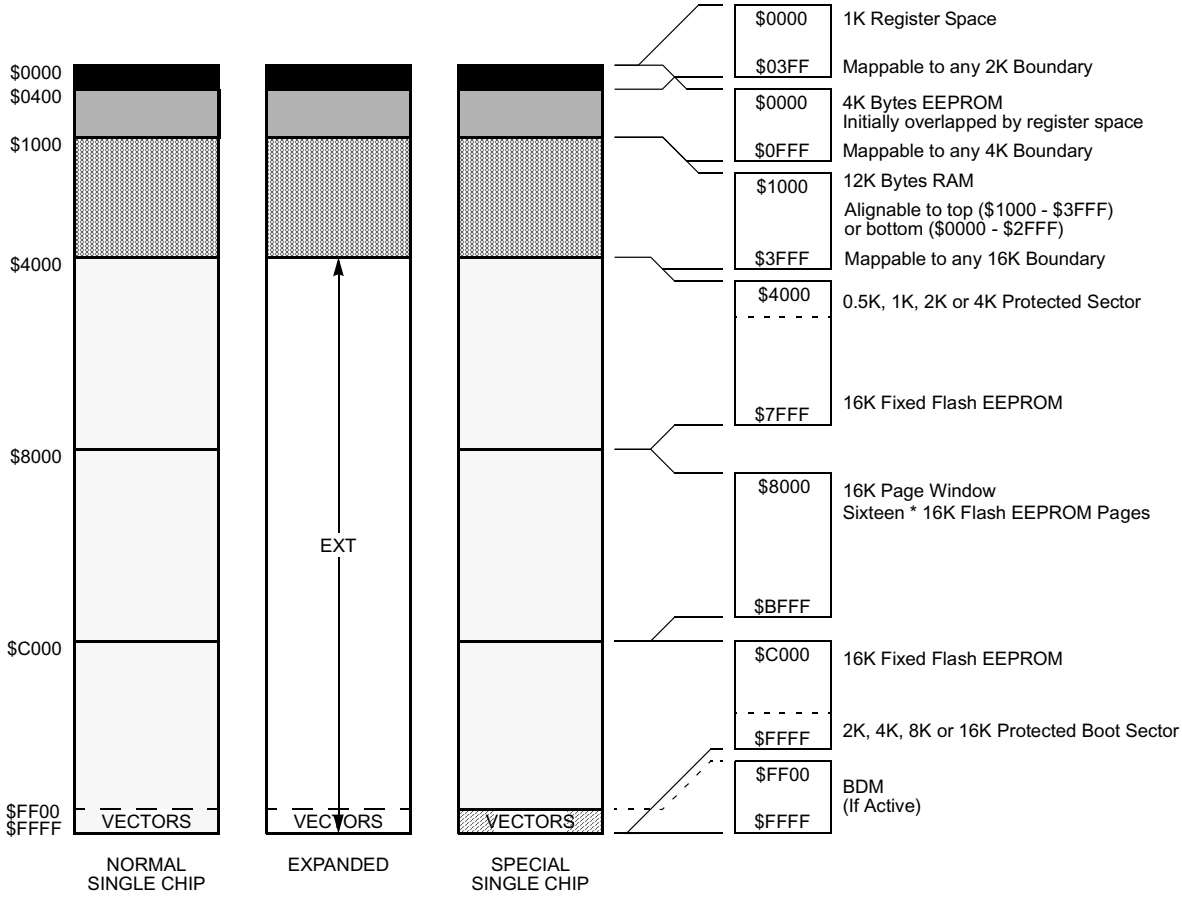
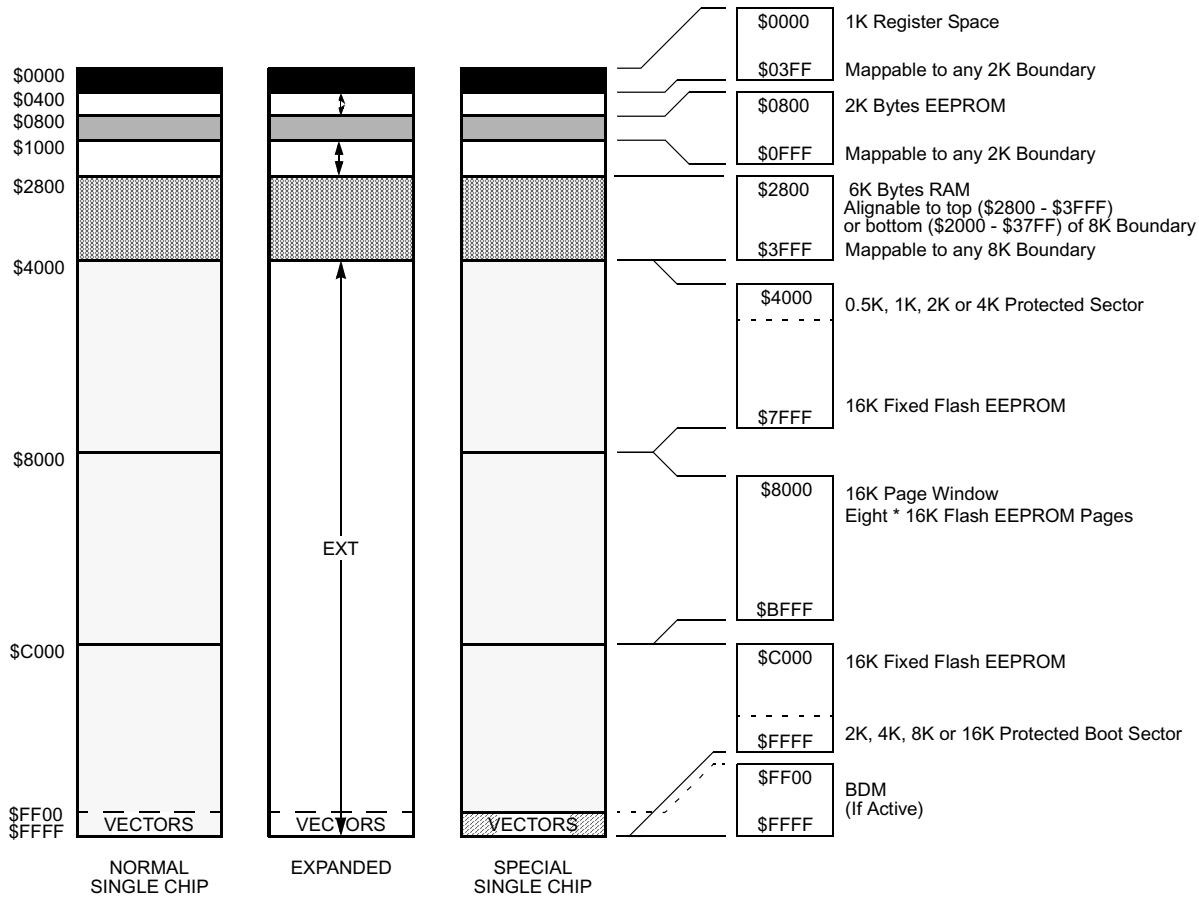


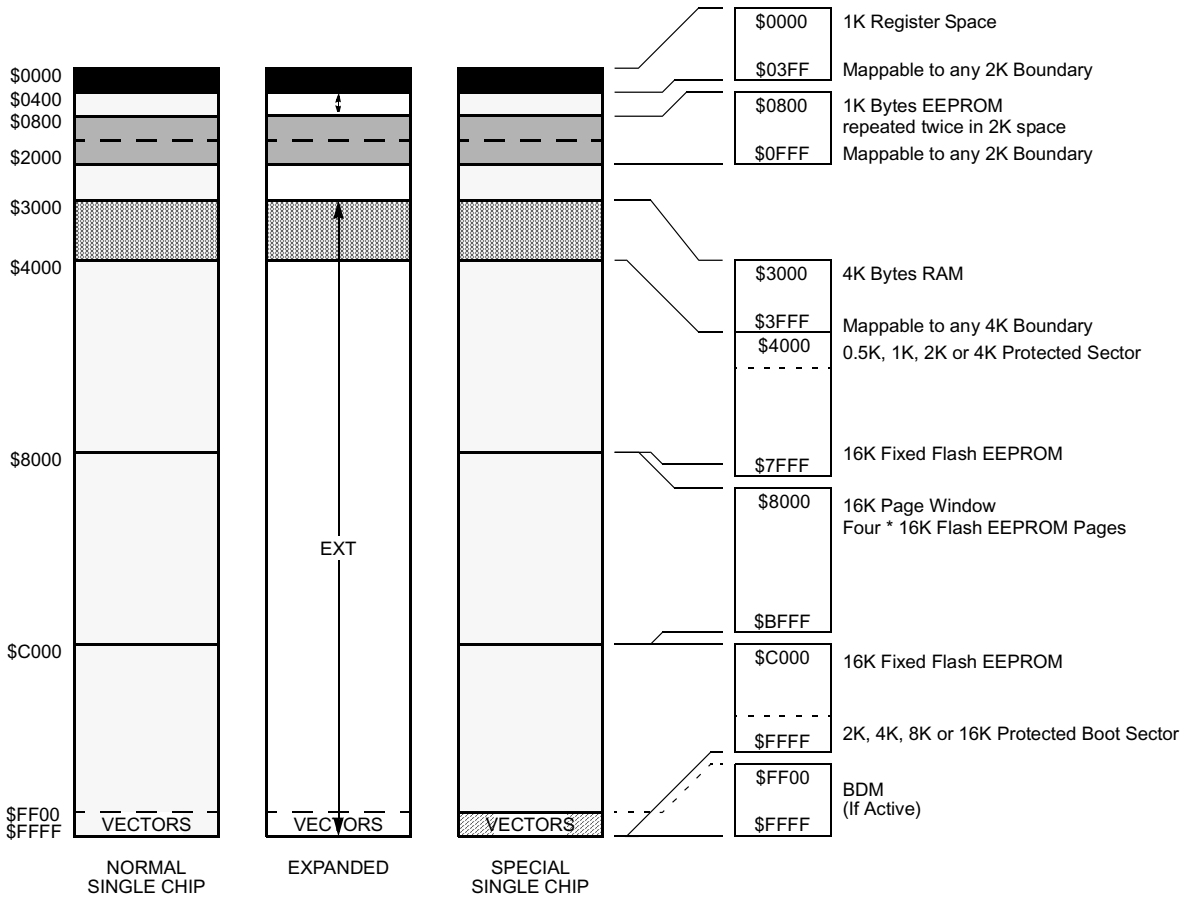
Figure 4. MC9S12H256 User Configurable Memory Map



The figure shows a useful map, which is not the map out of reset. After reset the map is:

$0000 - $03FF: Register Space
$0800 - $1FFF: 6K RAM
$0000 - $07FF: 2K EEPROM (1K not visible)

Figure 5. MC9S12H128 User Configurable Memory Map



The figure shows a useful map, which is not the map out of reset. After reset the map is:

$0000 - $03FF: Register Space
$0000 - $0FFF: 4K RAM (1K not visible)
$0000 - $07FF: 1K EEPROM (repeated twice in 2K address space, not visible)
$1000 - $3FFF: 12K Flash

Figure 6. MC9S12H64 User Configurable Memory Map

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