Data Sheet | July 1999 | FN4626.1

Radiation Hardened Synchronous Counter

Intersil's Satellite Applications Flow™ (SAF) devices are fully tested and guaranteed to 100kRAD total dose. These QML Class T devices are processed to a standard flow intended to meet the cost and shorter lead-time needs of large volume satellite manufacturers, while maintaining a high level of reliability.

The Intersil HCTS160T is a Radiation Hardened High Speed Presettable BCD Decade Synchronous Counter that features an asynchronous reset and look-ahead carry logic. Counting and parallel presetting are accomplished synchronously with the low-to-high transition of the clock. A low level on the synchronous parallel enable input, $\overline{SPE}$, disables counting and allows data at the preset inputs, P0 - P3, to be loaded into the counter. The counter is reset by a low on the master reset input, $\overline{MR}$. Two count enables, PE and TE are provided for n-bit cascading. TE also controls the terminal count output, TC. The terminal count output indicates a maximum count for one clock pulse and is used to enable the next cascaded stage to count.

Specifications

Specifications for Rad Hard QML devices are controlled by the Defense Supply Center in Columbus (DSCC). The SMD numbers listed below must be used when ordering.

Detailed Electrical Specifications for the HCTS160T are contained in SMD 5962-95742. Visit our website at: **www.intersil.com/**Intersil's Quality Management Plan (QM Plan), listing all Class T screening operations, is also available on our website.
www.intersil.com/

Ordering Information

ORDERING NUMBER	PART NUMBER	TEMP. RANGE (^oC)
5962R9574201TEC	HCTS160DTR	-55 to 125
5962R9574201TXC	HCTS160KTR	-55 to 125

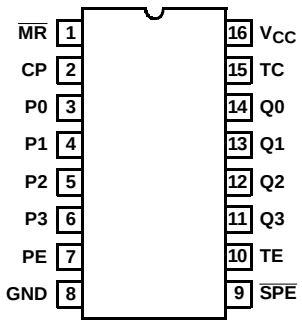
NOTE: ***Minimum order quantity for -T is 150 units through distribution, or 450 units direct.***

Features

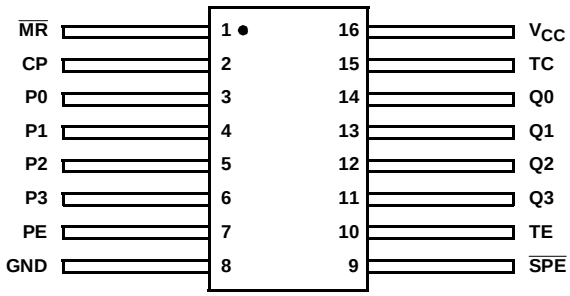
- QML Class T, Per MIL-PRF-38535
- Radiation Performance
  - Gamma Dose (γ) 1 x 10^5 RAD(Si)
  - Latch-Up Free Under Any Conditions
  - SEP Effective LET No Upsets: >100 MEV-cm^2/mg
  - Single Event Upset (SEU) Immunity < 2 x 10^{-9} Errors/Bit-Day (Typ)
- 3 Micron Radiation Hardened SOS CMOS
- Fanout (Over Temperature Range)
  - Standard Outputs 10 LSTTL Loads
- Significant Power Reduction Compared to LSTTL ICs
- DC Operating Voltage Range: 4.5V to 5.5V
- LSTTL Input Compatibility
  - V_{IL} = 0.8V Max
  - $V_{IH} = V_{CC/2}$ Min
- Input Current Levels Ii ≤ 5mA at V_{OL}, V_{OH}

Pinouts

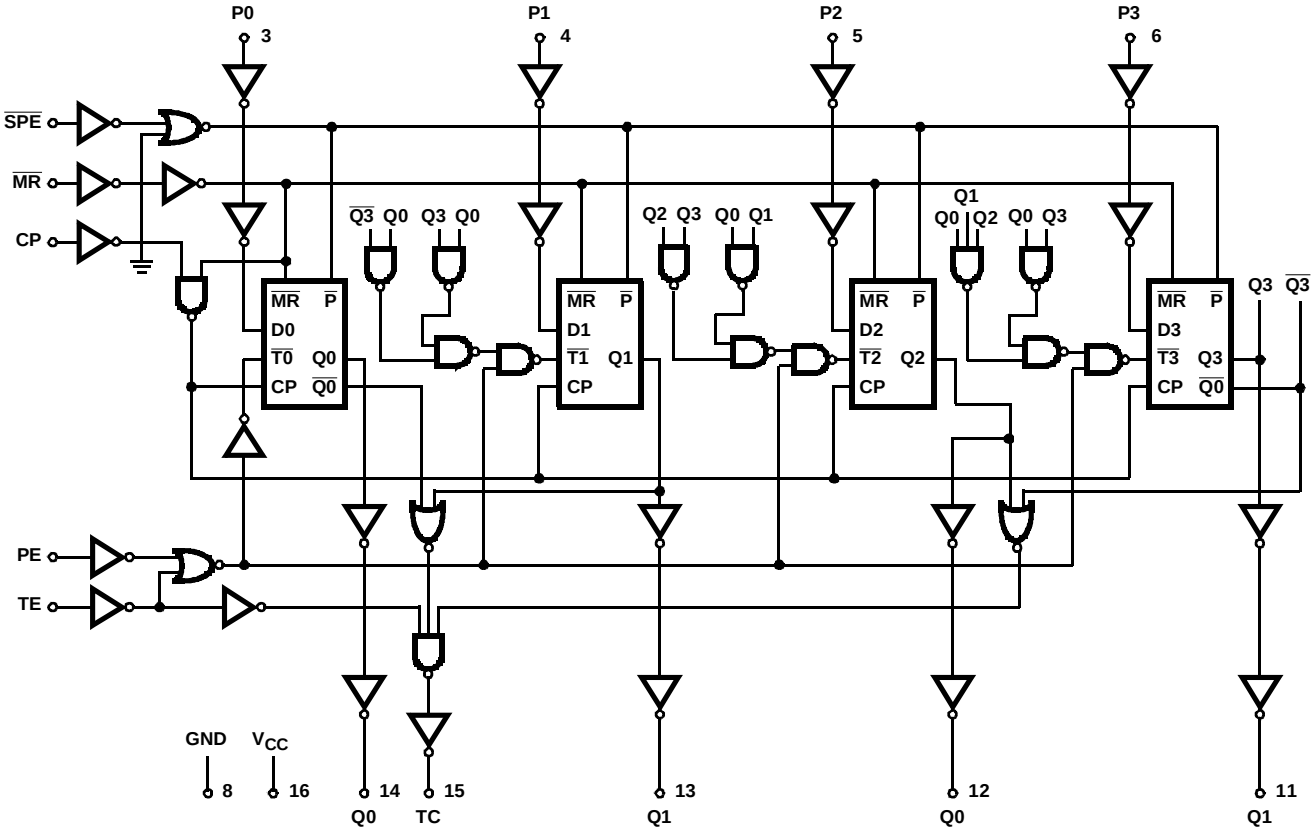
HCTS160DTR (SBDIP), CDIP2-T16
TOP VIEW



HCTS160KTR (FLATPACK), CDFP4-F16
TOP VIEW



Functional Diagram



TRUTH TABLE

OPERATING MODE	INPUTS						OUTPUTS	
	$\overline{MR}$	CP	PE	TE	$\overline{SPE}$	Pn	Qn	TC
Reset (Clear)	L	X	X	X	X	X	L	L
Parallel Load	H	⎍	X	X	l	l	L	L
	H	⎍	X	X	l	h	H	(Note 1)
Count	H	⎍	h	h	h (Note 3)	X	Count	(Note 1)
Inhibit	H	X	l (Note 2)	X	h (Note 3)	X	qn	(Note 1)
	H	X	X	l (Note 2)	h (Note 3)	X	qn	L

H = HIGH voltage level.

L = LOW voltage level.

h = HIGH voltage level one setup time prior to the LOW-to-HIGH clock transition.

l = LOW voltage level one setup time prior to the LOW-to-HIGH clock transition.

X = Immaterial.

q = Lower case letter indicate the state of the referenced output prior to the LOW-to-HIGH clock transition.

⎍ = LOW-to-HIGH clock transition.

NOTES:

1. The TC output is HIGH when TE is HIGH and the counter is at terminal count (HHHH for 161 and HLLH for 160).
2. The HIGH-to-LOW transition of PE or TE on the 54/74161 and 54/74160 should only occur while CP is high for conventional operation.
3. The LOW-to-HIGH transition of $\overline{SPE}$ on the 54/74161 and 54/74160 should only occur while CP is high for conventional operation.

Die Characteristics

DIE DIMENSIONS:

(2642μm x 2184μm x 533μm ±51.0μm)

104 x 86 x 21mils ±2mil

METALLIZATION:

Type: Al Si

Thickness: 11.0kÅ ±1kÅ

SUBSTRATE POTENTIAL:

Unbiased Silicon on Sapphire

BACKSIDE FINISH:

Sapphire

PASSIVATION:

Type: Silox (S_iO_2)

Thickness: 13.0kÅ ±2.6kÅ

WORST CASE CURRENT DENSITY:

< 2.0e5 A/cm^2

TRANSISTOR COUNT:

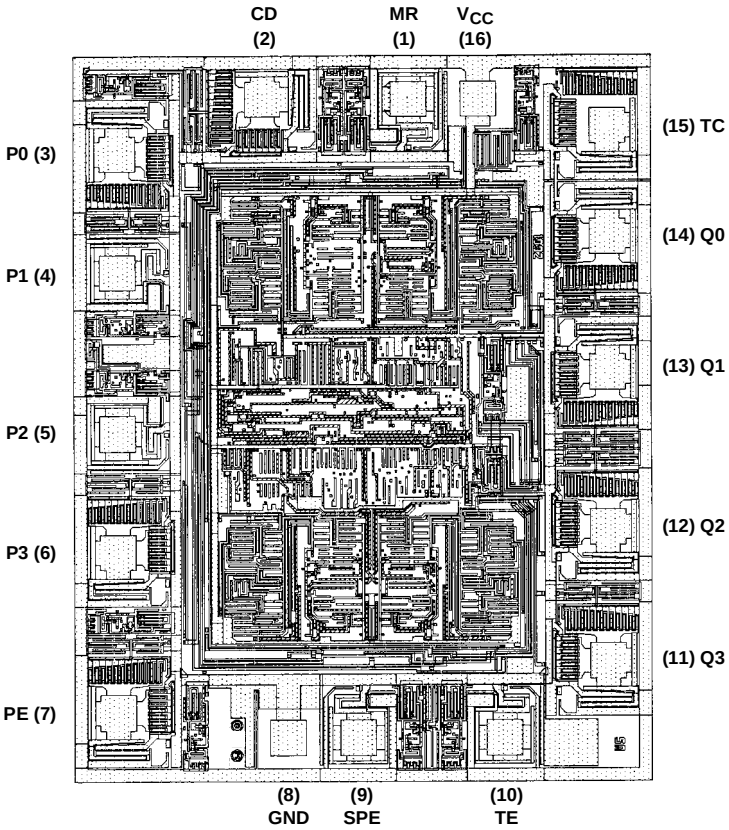
676

PROCESS:

CMOS SOS

Metallization Mask Layout

HCTS160T



NOTE: The die diagram is a generic plot from a similar HCS device. It is intended to indicate approximate die size and bond pad location. The mask series for the HCTS160 is TA14445A.