

## Radiation Hardened Synchronous Counter

Intersil's Satellite Applications Flow™ (SAF) devices are fully tested and guaranteed to 100kRAD total dose. These QML Class T devices are processed to a standard flow intended to meet the cost and shorter lead-time needs of large volume satellite manufacturers, while maintaining a high level of reliability.

The Intersil HCTS160T is a Radiation Hardened High Speed Presettable BCD Decade Synchronous Counter that features an asynchronous reset and look-ahead carry logic. Counting and parallel presetting are accomplished synchronously with the low-to-high transition of the clock. A low level on the synchronous parallel enable input, SPE, disables counting and allows data at the preset inputs, P0 - P3, to be loaded into the counter. The counter is reset by a low on the master reset input, MR. Two count enables, PE and TE are provided for n-bit cascading. TE also controls the terminal count output, TC. The terminal count output indicates a maximum count for one clock pulse and is used to enable the next cascaded stage to count.

### Specifications

Specifications for Rad Hard QML devices are controlled by the Defense Supply Center in Columbus (DSCC). The SMD numbers listed below must be used when ordering.

**Detailed Electrical Specifications for the HCTS160T are contained in SMD 5962-95742.** Visit our website at: [www.intersil.com/Intersil's Quality Management Plan \(QM Plan\)](http://www.intersil.com/Intersil's%20Quality%20Management%20Plan%20(QM%20Plan)), listing all Class T screening operations, is also available on our website. [www.intersil.com/](http://www.intersil.com/)

### Ordering Information

ORDERING NUMBER	PART NUMBER	TEMP. RANGE (°C)
5962R9574201TEC	HCTS160DTR	-55 to 125
5962R9574201TXC	HCTS160KTR	-55 to 125

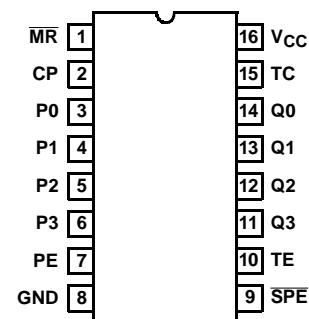
NOTE: **Minimum order quantity for -T is 150 units through distribution, or 450 units direct.**

### Features

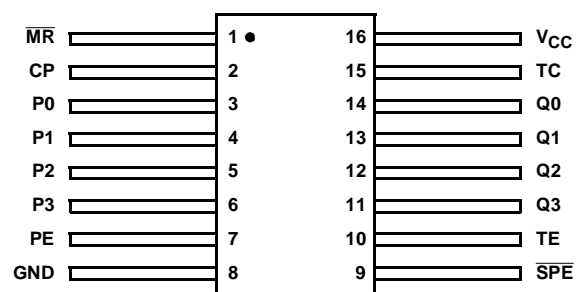
- QML Class T, Per MIL-PRF-38535
- Radiation Performance
  - Gamma Dose ( $\gamma$ )  $1 \times 10^5$  RAD(Si)
  - Latch-Up Free Under Any Conditions
  - SEP Effective LET No Upsets:  $>100$  MEV-cm<sup>2</sup>/mg
  - Single Event Upset (SEU) Immunity  $< 2 \times 10^{-9}$  Errors/Bit-Day (Typ)
- 3 Micron Radiation Hardened SOS CMOS
- Fanout (Over Temperature Range)
  - Standard Outputs 10 LSTTL Loads
- Significant Power Reduction Compared to LSTTL ICs
- DC Operating Voltage Range: 4.5V to 5.5V
- LSTTL Input Compatibility
  - $V_{IL} = 0.8V$  Max
  - $V_{IH} = V_{CC}/2$  Min
- Input Current Levels  $I_i \leq 5mA$  at  $V_{OL}, V_{OH}$

### Pinouts

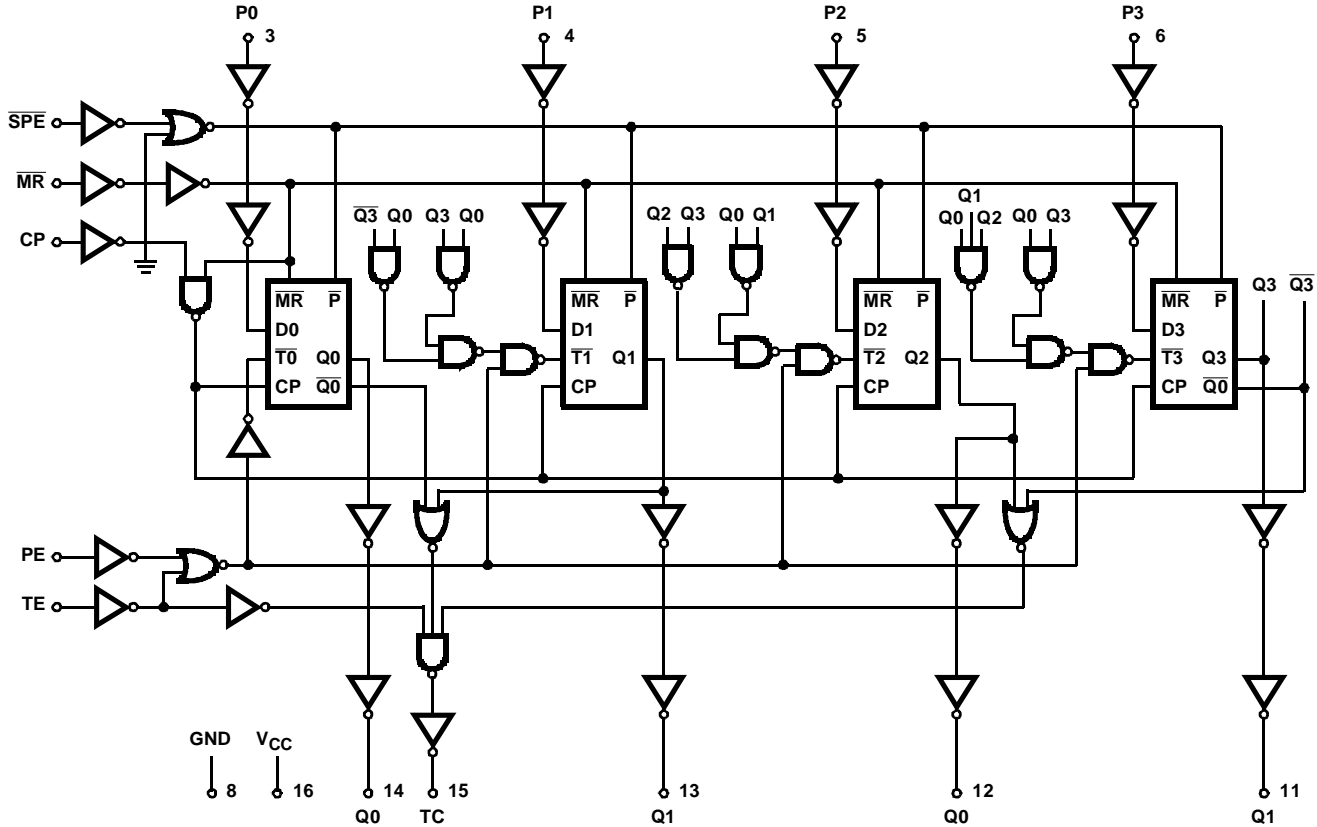
**HCTS160DTR (SBDIP), CDIP2-T16**  
TOP VIEW



**HCTS160KTR (FLATPACK), CDFP4-F16**  
TOP VIEW



Functional Diagram



TRUTH TABLE

OPERATING MODE	INPUTS						OUTPUTS	
	$\overline{MR}$	CP	PE	TE	$\overline{SPE}$	Pn	Qn	TC
Reset (Clear)	L	X	X	X	X	X	L	L
Parallel Load	H		X	X	l	l	L	L
	H		X	X	l	h	H	(Note 1)
Count	H		h	h	h (Note 3)	X	Count	(Note 1)
Inhibit	H	X	l (Note 2)	X	h (Note 3)	X	qn	(Note 1)
	H	X	X	l (Note 2)	h (Note 3)	X	qn	L

H = HIGH voltage level.

L = LOW voltage level.

h = HIGH voltage level one setup time prior to the LOW-to-HIGH clock transition.

l = LOW voltage level one setup time prior to the LOW-to-HIGH clock transition.

X = Immaterial.

q = Lower case letter indicate the state of the referenced output prior to the LOW-to-HIGH clock transition.

= LOW-to-HIGH clock transition.

NOTES:

1. The TC output is HIGH when TE is HIGH and the counter is at terminal count (HHHH for 161 and HLLH for 160).
2. The HIGH-to-LOW transition of PE or TE on the 54/74161 and 54/74160 should only occur while CP is high for conventional operation.
3. The LOW-to-HIGH transition of  $\overline{SPE}$  on the 54/74161 and 54/74160 should only occur while CP is high for conventional operation.

# HCTS160T

## Die Characteristics

### DIE DIMENSIONS:

(2642 $\mu$ m x 2184 $\mu$ m x 533 $\mu$ m  $\pm$ 51.0 $\mu$ m)  
104 x 86 x 21mils  $\pm$ 2mil

### METALLIZATION:

Type: Al Si  
Thickness: 11.0k $\text{\AA}$   $\pm$ 1k $\text{\AA}$

### SUBSTRATE POTENTIAL:

Unbiased Silicon on Sapphire

### BACKSIDE FINISH:

Sapphire

### PASSIVATION:

Type: Silox (SiO<sub>2</sub>)  
Thickness: 13.0k $\text{\AA}$   $\pm$ 2.6k $\text{\AA}$

### WORST CASE CURRENT DENSITY:

< 2.0e5 A/cm<sup>2</sup>

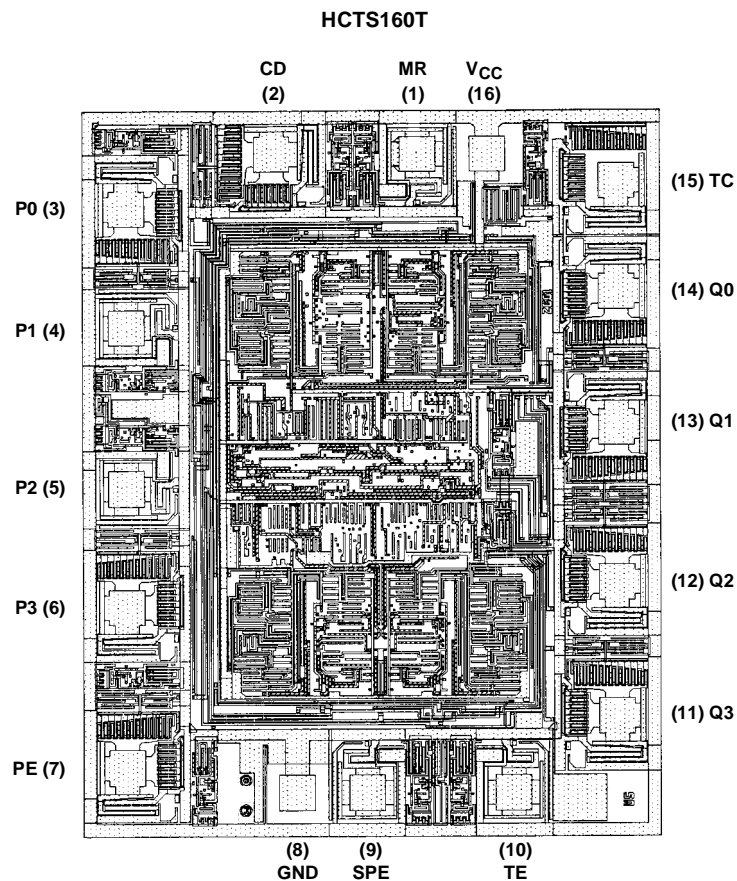
### TRANSISTOR COUNT:

676

### PROCESS:

CMOS SOS

## Metallization Mask Layout



NOTE: The die diagram is a generic plot from a similar HCS device. It is intended to indicate approximate die size and bond pad location. The mask series for the HCTS160 is TA14445A.

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