Data Sheet | July 1999 | FN4618.1

Radiation Hardened Octal Buffer/Line Driver, Three-State

Intersil's Satellite Applications Flow™ (SAF) devices are fully tested and guaranteed to 100kRAD total dose. These QML Class T devices are processed to a standard flow intended to meet the cost and shorter lead-time needs of large volume satellite manufacturers, while maintaining a high level of reliability.

The Intersil HCTS244T is a Radiation Hardened Non-Inverting Octal Buffer/Line Driver, Three-State, with two active-low output enables.

Specifications

Specifications for Rad Hard QML devices are controlled by the Defense Supply Center in Columbus (DSCC). The SMD numbers listed below must be used when ordering.

Detailed Electrical Specifications for the HCTS244T are contained in SMD 5962-95744. Visit our website fat **www.intersil.com/**

Intersil's Quality Management Plan (QM Plan), listing all Class T screening operations, is also available on our website.
www.intersil.com/

Ordering Information

ORDERING NUMBER	PART NUMBER	TEMP. RANGE (^oC)
5962R9574401TRC	HCTS244DTR	-55 to 125
5962R9574401TXC	HCTS244KTR	-55 to 125

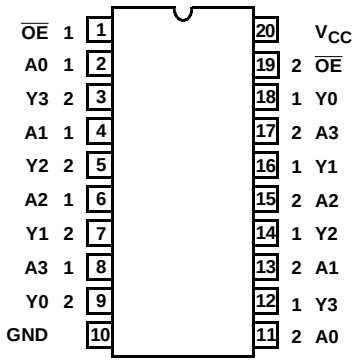
NOTE: ***Minimum order quantity for -T is 150 units through distribution, or 450 units direct.***

Features

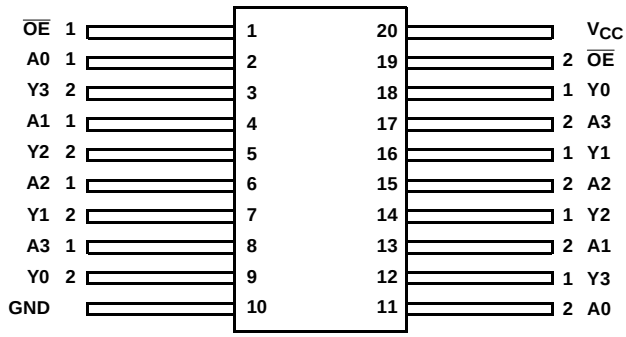
- QML Class T, Per MIL-PRF-38535
- Radiation Performance
  - Gamma Dose (γ) 1 x 10^5 RAD(Si)
  - Latch-Up Free Under Any Conditions
  - SEP Effective LET No Upsets: >100 MEV-cm^2/mg
  - Single Event Upset (SEU) Immunity < 2 x 10^{-9} Errors/Bit-Day (Typ)
- 3 Micron Radiation Hardened CMOS SOS
- Fanout (Over Temperature Range)
  - Bus Driver Outputs - 15 LSTTL Loads
- Significant Power Reduction Compared to LSTTL ICs
- DC Operating Voltage Range: 4.5V to 5.5V
- LSTTL Input Compatibility
  - V_{IL} = 0.8V Max
  - VI_H = $V_{CC/2}$ Min
- Input Current Levels Ii ≤ 5mA at V_{OL}, V_{OH}

Pinouts

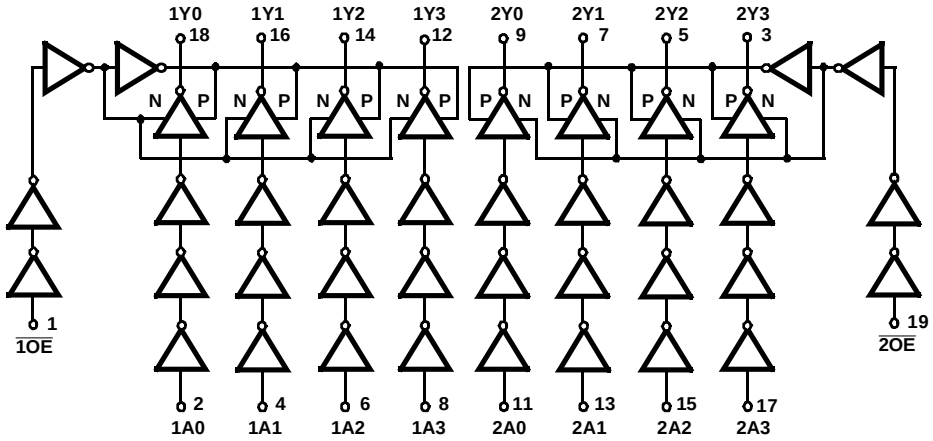
HCTS244DTR (SBDIP), CDIP2-T20
TOP VIEW



HCTS244KTR (FLATPACK), CDFP4-F20
TOP VIEW



Functional Diagram



TRUTH TABLE

INPUTS		OUTPUT
$\overline{1OE}$, $\overline{2OE}$	A	Y
L	L	L
L	H	H
H	X	Z

H = High Voltage Level.
L = Low Voltage Level.
X = Immaterial.
Z = High Impedance.

Die Characteristics

DIE DIMENSIONS:

(2743µm x 2692µm x 533µm ±51µm)

108 x 106 x 21mils ±2mil

METALLIZATION:

Type: Al Si

Thickness: 11.0kÅ ±1kÅ

SUBSTRATE POTENTIAL:

Unbiased Silicon on Sapphire

BACKSIDE FINISH:

Sapphire

PASSIVATION:

Type: Silox (S_iO_2)

Thickness: 13.0kÅ ±2.6kÅ

WORST CASE CURRENT DENSITY:

< 2.0e5 A/cm^2

TRANSISTOR COUNT:

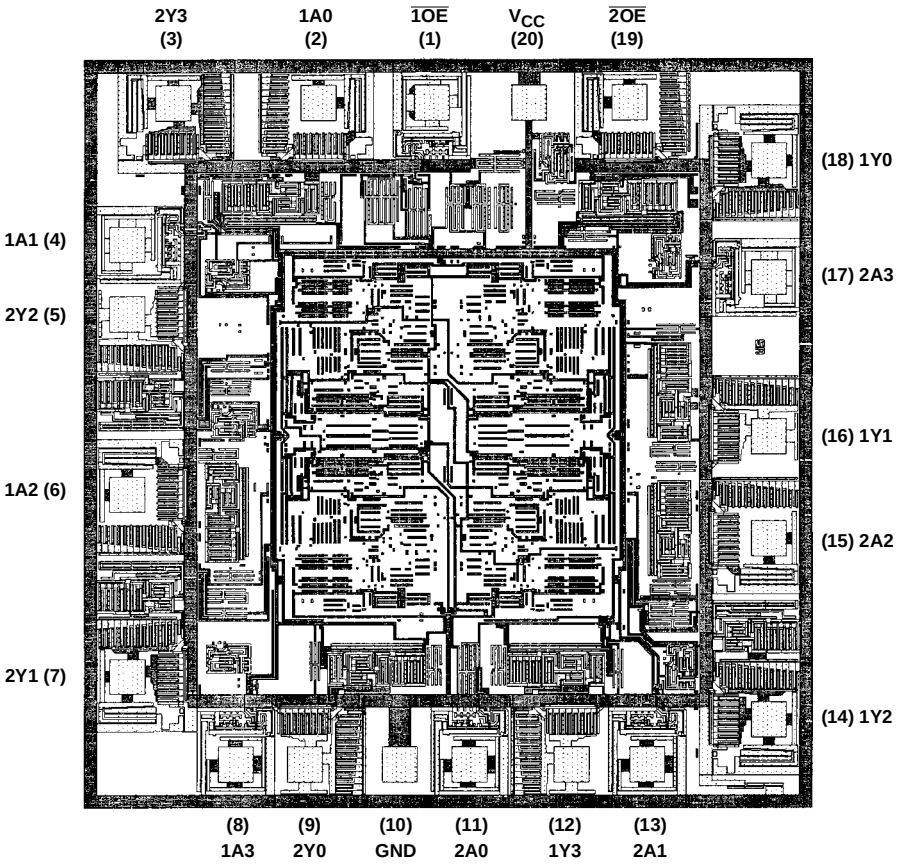
264

PROCESS:

CMOS SOS

Metallization Mask Layout

HCTS244T



NOTE: The die diagram is a generic plot from a similar HCS device. It is intended to indicate approximate die size and bond pad location. The mask series for the HCTS244 is TA14402A.