

### Features

- Throughput Rate ..... 40MHz
- Resolution ..... 8-Bit
- Integral Linearity Error ..... 0.25 LSB
- Low Glitch Noise
- Single Supply Operation ..... +5V
- Low Power Consumption (Max) ..... 80mW
- Evaluation Board Available (HI1171-EV)
- Direct Replacement for the Sony CXD1171

### Applications

- Wireless Telecommunications
- Signal Reconstruction
- Direct Digital Synthesis
- Imaging
- Presentation and Broadcast Video
- Graphics Displays
- Signal Generators

### Description

The HI1171 is an 8-bit, 40MHz, high speed D/A converter. The converter incorporates an 8-bit input data register with blanking capability, and current outputs. The HI1171 features low glitch outputs. The architecture is a current cell arrangement to provide low linearity errors.

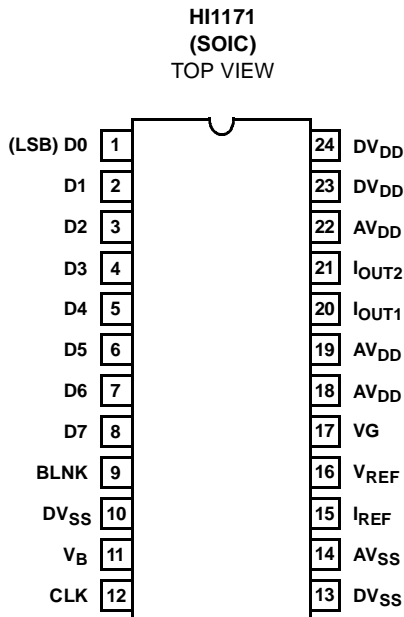
The HI1171 is available in an Industrial temperature range and is offered in a 24 lead (200 mil) SOIC plastic package.

For dual version, please refer to the HI1177 Data Sheet. For triple version, please refer to the HI1178 Data Sheet.

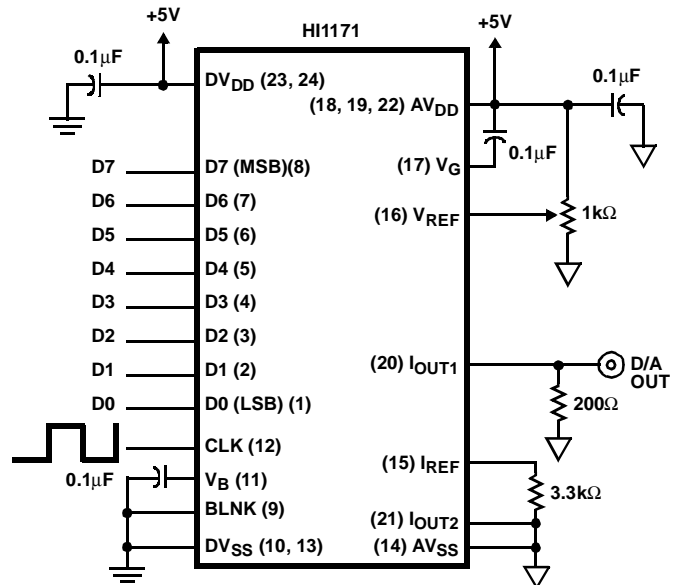
### Ordering Information

| PART NUMBER | TEMP. RANGE (°C) | PACKAGE          | PKG. NO. |
|-------------|------------------|------------------|----------|
| HI1171JCB   | -40 to 85        | 24 Ld SOIC       | M24.2-S  |
| HI1171-EV   | 25               | Evaluation Board |          |

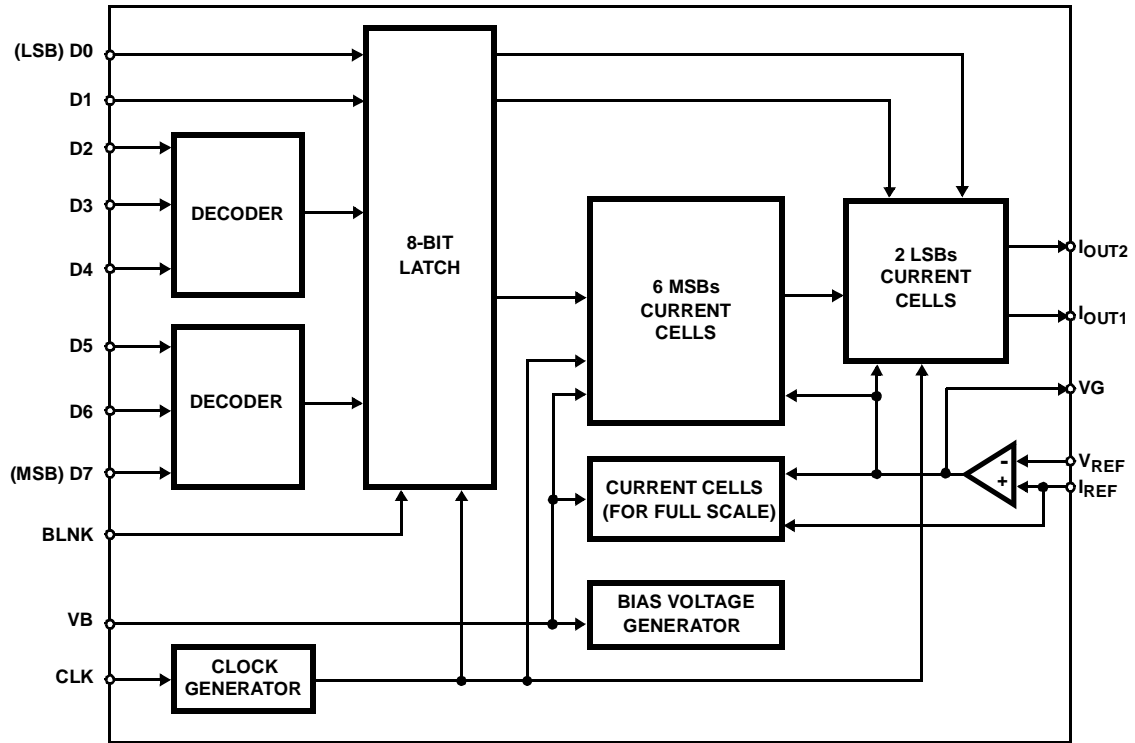
### Pinout



### Typical Application Circuit



**Functional Block Diagram**



# HI1171

## Absolute Maximum Ratings

Digital Supply Voltage  $DV_{DD}$  to  $DV_{SS}$  ..... +7.0V  
 Analog Supply Voltage  $AV_{DD}$  to  $AV_{SS}$  ..... +7.0V  
 Input Voltage .....  $V_{DD}$  to  $V_{SS}$  V  
 Output Current ..... 0mA to 15mA

## Operating Conditions

Temperature Range ..... -40°C to 85°C

*CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.*

### NOTE:

1.  $\theta_{JA}$  is measured with the component mounted on an evaluation PC board in free air.

## Thermal Information

Thermal Resistance (Typical, Note 1)  $\theta_{JA}$  (°C/W)  
 SOIC Package ..... 98  
 Maximum Junction Temperature, Plastic Package ..... 150°C  
 Maximum Storage Temperature Range ..... -65°C to 150°C  
 Maximum Lead Temperature (Soldering 10s) ..... 300°C  
 (SOIC - Lead Tips Only)

**Electrical Specifications**  $AV_{DD} = +4.75V$  to  $+5.25V$ ,  $DV_{DD} = +4.75$  to  $+5.25V$ ,  $V_{REF} = +2.0V$ ,  $f_S = 40MHz$ ,  
 CLK Pulse Width = 12.5ns,  $T_A = 25^\circ C$  (Note 4)

| PARAMETER                                  | TEST CONDITIONS           | MIN  | TYP | MAX   | UNITS  |
|--|---------------------------|------|-----|-------|--------|
| <b>SYSTEM PERFORMANCE</b>                  |                           |      |     |       |        |
| Resolution, n                              |                           | -    | 8   | -     | Bits   |
| Integral Linearity Error, INL              | $f_S = 40MHz$ (End Point) | -0.5 | -   | 1.3   | LSB    |
| Differential Linearity Error, DNL          | $f_S = 40MHz$             | -    | -   | ±0.25 | LSB    |
| Offset Error, $V_{OS}$                     | (Note 2)                  | -    | -   | 1     | mV     |
| Full Scale Error, FSE (Adjustable to Zero) | (Note 2)                  | -    | -   | ±13   | LSB    |
| Full Scale Output Current, $I_{FS}$        |                           | -    | 10  | 15    | mA     |
| Full Scale Output Voltage, $V_{FS}$        |                           | 1.9  | 2.0 | 2.1   | V      |
| Output Voltage Range, $V_{FSR}$            |                           | 0.5  | 2.0 | 2.1   | V      |
| <b>DYNAMIC CHARACTERISTICS</b>             |                           |      |     |       |        |
| Throughput Rate                            | See Figure 7              | 40.0 | -   | -     | MHz    |
| Glitch Energy, GE                          | $R_{OUT} = 75\Omega$      | -    | 30  | -     | pV-s   |
| Differential Gain, $\Delta A_V$ (Note 3)   |                           | -    | 1.2 | -     | %      |
| Differential Phase, $\Delta\phi$ (Note 3)  |                           | -    | 0.5 | -     | Degree |
| <b>REFERENCE INPUT</b>                     |                           |      |     |       |        |
| Voltage Reference Input Range              |                           | 0.5  | -   | 2.0   | V      |
| Reference Input Resistance                 | (Note 3)                  | 1.0  | -   | -     | MΩ     |
| <b>DIGITAL INPUTS</b>                      |                           |      |     |       |        |
| Input Logic High Voltage, $V_{IH}$         | (Note 3)                  | 3.0  | -   | -     | V      |
| Input Logic Low Voltage, $V_{IL}$          | (Note 3)                  | -    | -   | 1.5   | V      |
| Input Logic Current, $I_{IL}$ , $I_{IH}$   | (Note 3)                  | -    | -   | ±5.0  | μA     |
| Digital Input Capacitance, $C_{IN}$        | (Note 3)                  | -    | 5.0 | -     | pF     |
| <b>TIMING CHARACTERISTICS</b>              |                           |      |     |       |        |
| Data Setup Time, $t_{SU}$                  | See Figure 1              | 5    | -   | -     | ns     |
| Data Hold Time, $t_{HLD}$                  | See Figure 1              | 10   | -   | -     | ns     |

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**Electrical Specifications**  $AV_{DD} = +4.75V$  to  $+5.25V$ ,  $DV_{DD} = +4.75$  to  $+5.25V$ ,  $V_{REF} = +2.0V$ ,  $f_S = 40MHz$ ,  
 CLK Pulse Width =  $12.5ns$ ,  $T_A = 25^{\circ}C$  (Note 4) **(Continued)**

| PARAMETER                               | TEST CONDITIONS                       | MIN  | TYP  | MAX  | UNITS |
|---|---------------------------------------|------|------|------|-------|
| Propagation Delay Time, $t_{PD}$        | See Figure 9                          | -    | 10   | -    | ns    |
| Settling Time, $t_{SET}$ (to $1/2$ LSB) | See Figure 1                          | -    | 10   | 15   | ns    |
| CLK Pulse Width, $t_{PW1}$ , $t_{PW2}$  | See Figure 1                          | 12.5 | -    | -    | ns    |
| <b>POWER SUPPLY CHARACTERISITICS</b>    |                                       |      |      |      |       |
| $I_{AV_{DD}}$                           | 14.3MHz, at Color Bar Data Input      | -    | 10.9 | 11.5 | mA    |
| $I_{DV_{DD}}$                           | 14.3MHz, at Color Bar Data Input      | -    | 4.2  | 4.8  | mA    |
| Power Dissipation                       | $200\Omega$ load at $2V_{P-P}$ Output | -    | -    | 80   | mW    |

**NOTES:**

- Excludes error due to external reference drift.
- Parameter guaranteed by design or characterization and not production tested.
- Electrical specifications guaranteed only under the stated operating conditions.

## Timing Diagram

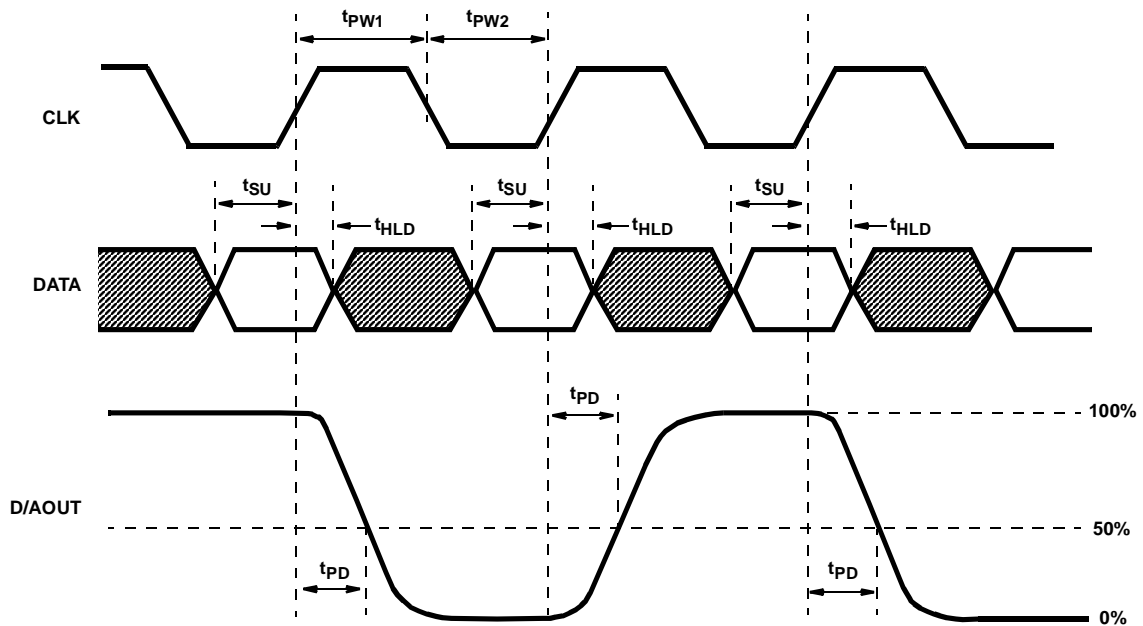


FIGURE 1.

**Typical Performance Curves**

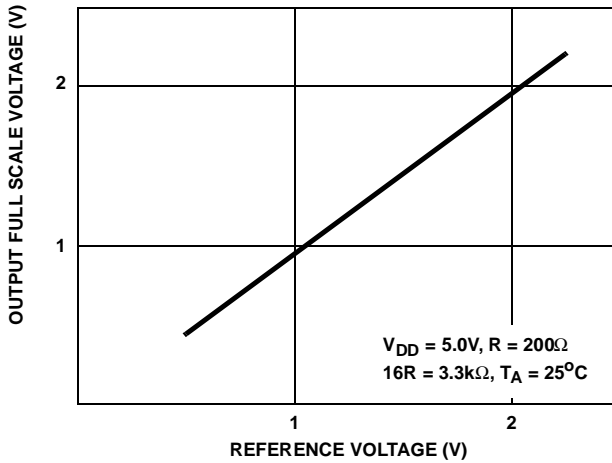


FIGURE 2. OUTPUT FULL SCALE VOLTAGE vs REFERENCE VOLTAGE

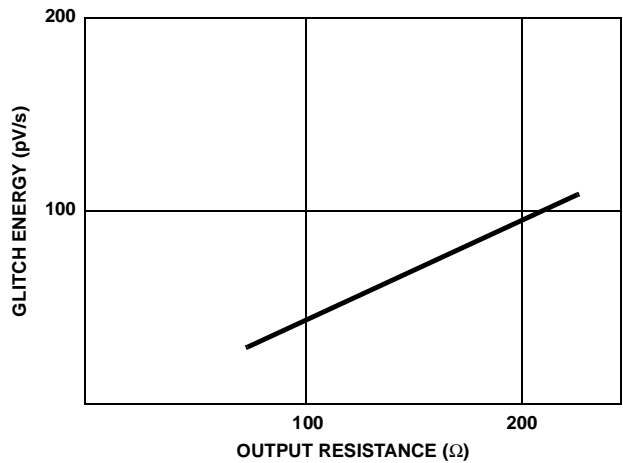


FIGURE 3. OUTPUT RESISTANCE vs GLITCH ENERGY

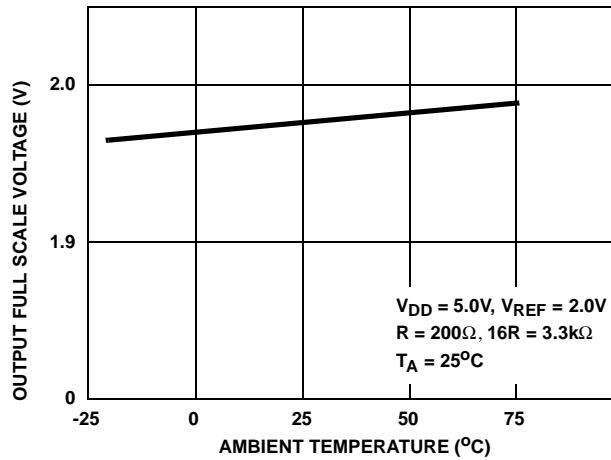


FIGURE 4. OUTPUT FULL SCALE VOLTAGE vs AMBIENT TEMPERATURE

**Pin Descriptions**

| 24 PIN SOIC | PIN NAME             | PIN DESCRIPTION  |
|-------------|----------------------|--|
| 1-8         | D0(LSB) thru D7(MSB) | Digital Data Bit 0, the Least Significant Bit thru Digital Data Bit 7, the Most Significant Bit.   |
| 9           | BLNK                 | Blanking Line, used to clear the internal data register to the zero condition when High, normal operation when Low.  |
| 10, 13      | DV <sub>SS</sub>     | Digital Ground.  |
| 11          | VB                   | Voltage Bias, connect a 0.1μF capacitor to DV <sub>SS</sub> .  |
| 12          | CLK                  | Data Clock Pin 100kHz to 40MHz.  |
| 14          | AV <sub>SS</sub>     | Analog Ground.   |
| 15          | I <sub>REF</sub>     | Current Reference, used to set the current range. Connect a resistor to AV <sub>SS</sub> that is 16 times greater than the resistor on I <sub>OUT1</sub> . (See Typical Applications Circuit). |
| 16          | V <sub>REF</sub>     | Input Reference Voltage used to set the output full scale range.   |

**Pin Descriptions** (Continued)

| 24 PIN SOIC | PIN NAME          | PIN DESCRIPTION  |
|-------------|-------------------|--|
| 17          | VG                | Voltage Ground, connect a 0.1μF capacitor to AV <sub>DD</sub> .                                  |
| 18, 19, 22  | AV <sub>DD</sub>  | Analog Supply 4.75V to 7V.   |
| 20          | I <sub>OUT1</sub> | Current Output Pin.  |
| 21          | I <sub>OUT2</sub> | Current Output pin used for a virtual ground connection. Usually connected to AV <sub>SS</sub> . |
| 23, 24      | DV <sub>DD</sub>  | Digital Supply 4.75V to 7V.  |

**Detailed Description**

The HI1171 is an 8-bit, current out D/A converter. The DAC can convert at 40MHz and run on a single +5V supply. The architecture is an encoded, switched current cell arrangement.

**Voltage Output Mode**

The output current of the HI1171 can be converted into a voltage by connecting an external resistor to I<sub>OUT1</sub>. To calculate the output resistor use the following equation:

$$R_{OUT} = V_{FS} / I_{FS}$$

where V<sub>FS</sub> can range from +0.5V to +2.0V and I<sub>FS</sub> can range from 0mA to 15mA.

In setting the output current the I<sub>REF</sub> pin should have a resistor connected to it that is 16 times greater than the output resistor:

$$R_{REF} = 16 \times R_{OUT}$$

As the values of both R<sub>OUT</sub> and R<sub>REF</sub> increase, power consumption is decreased, but glitch energy and output settling time is increased.

**Clock Phase Relationship**

The internal latch is closed when the clock line is high. The latch can be cleared by the BLNK line. When BLNK is set (HIGH) the contents of the internal data latch will be cleared. When BLNK is low data is updated by the CLK.

**Noise Reduction**

To reduce power supply noise separate analog and digital power supplies should be used with 0.1μF ceramic capacitors placed as close to the body of the HI1171 as possible. The analog (AV<sub>SS</sub>) and digital (DV<sub>SS</sub>) ground returns should be connected together back at the power supply to ensure proper operation from power up.

**Test Circuits**

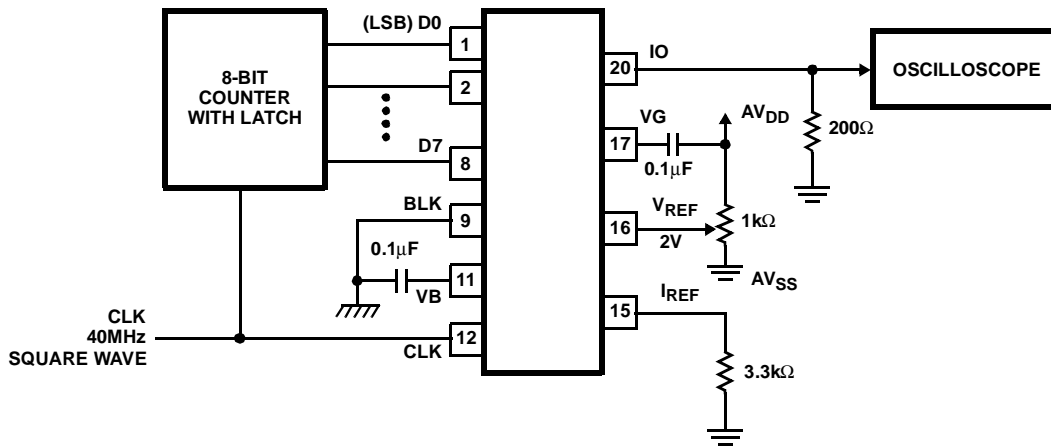


FIGURE 5. MAXIMUM CONVERSION SPEED TEST CIRCUIT

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Test Circuits (Continued)

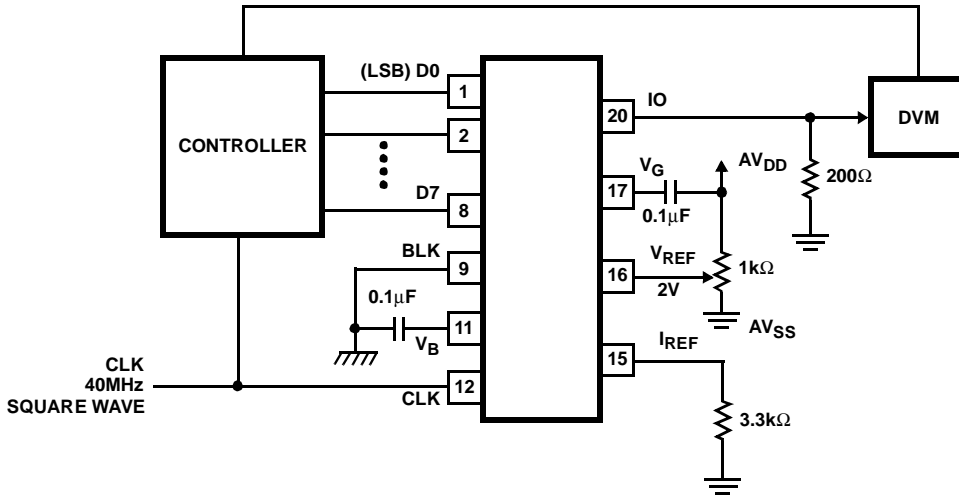


FIGURE 6. DC CHARACTERISTICS TEST CIRCUIT

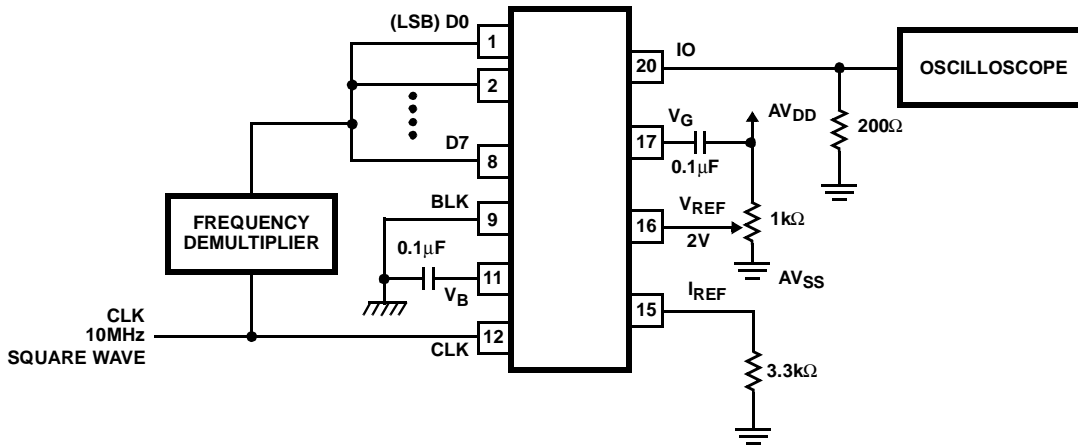


FIGURE 7. PROPAGATION DELAY TIME TEST CIRCUIT

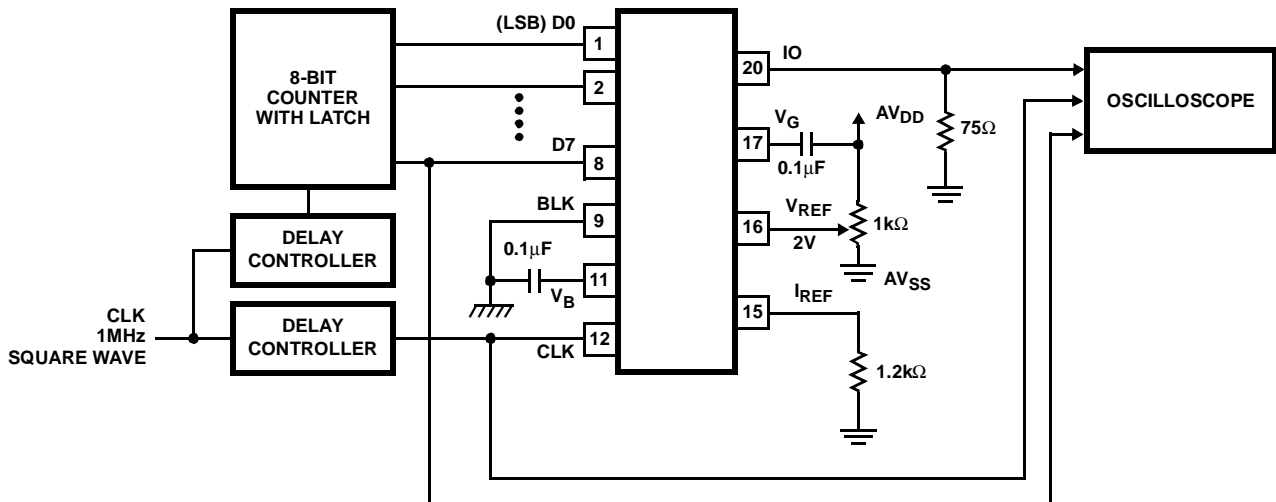


FIGURE 8. SET UP HOLD TIME AND GLITCH ENERGY TEST CIRCUIT