HARRIS Semiconductor

NOT RECOMMENDED FOR NEW DESIGNS
See HI3086

HI1866

October 1998

6-Bit, 140 MSPS, Flash A/D Converter

Features

- **Ultra-High Speed Operation with Maximum Conversion Rate. . . . . 140 MSPS**
- **Low Input Capacitance 7pF**
- **Wide Analog Input Bandwidth 210MHz**
- **Low Power Consumption 325mW**
- **Low Error Rate**
- **Excellent Temperature Characteristics**
- **1:2 Demultiplexed Output (TTL Level)**
- **Direct Replacement for Sony CXA1866**

Applications

- **LCD Panels**
- **Magnetic Recording (PRML)**
- **Communications (QPSK, QAM)**

Description

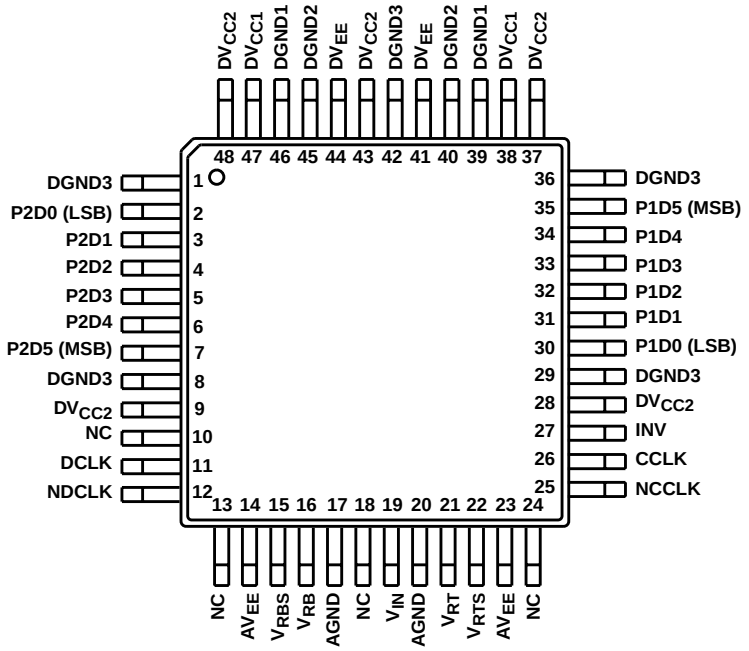
HI1866 is a 6-bit, high-speed, flash A/D converter capable of digitizing analog signals at the maximum rate of 140 MSPS. The digital input level is compatible with the ECL 100K/10KH/10K.

Ordering Information

PART NUMBER	TEMP. RANGE (^{o}C)	PACKAGE	PKG. NO.
HI1866JCQ	-20 to 75	48 Ld MQFP	Q48.12x12-S

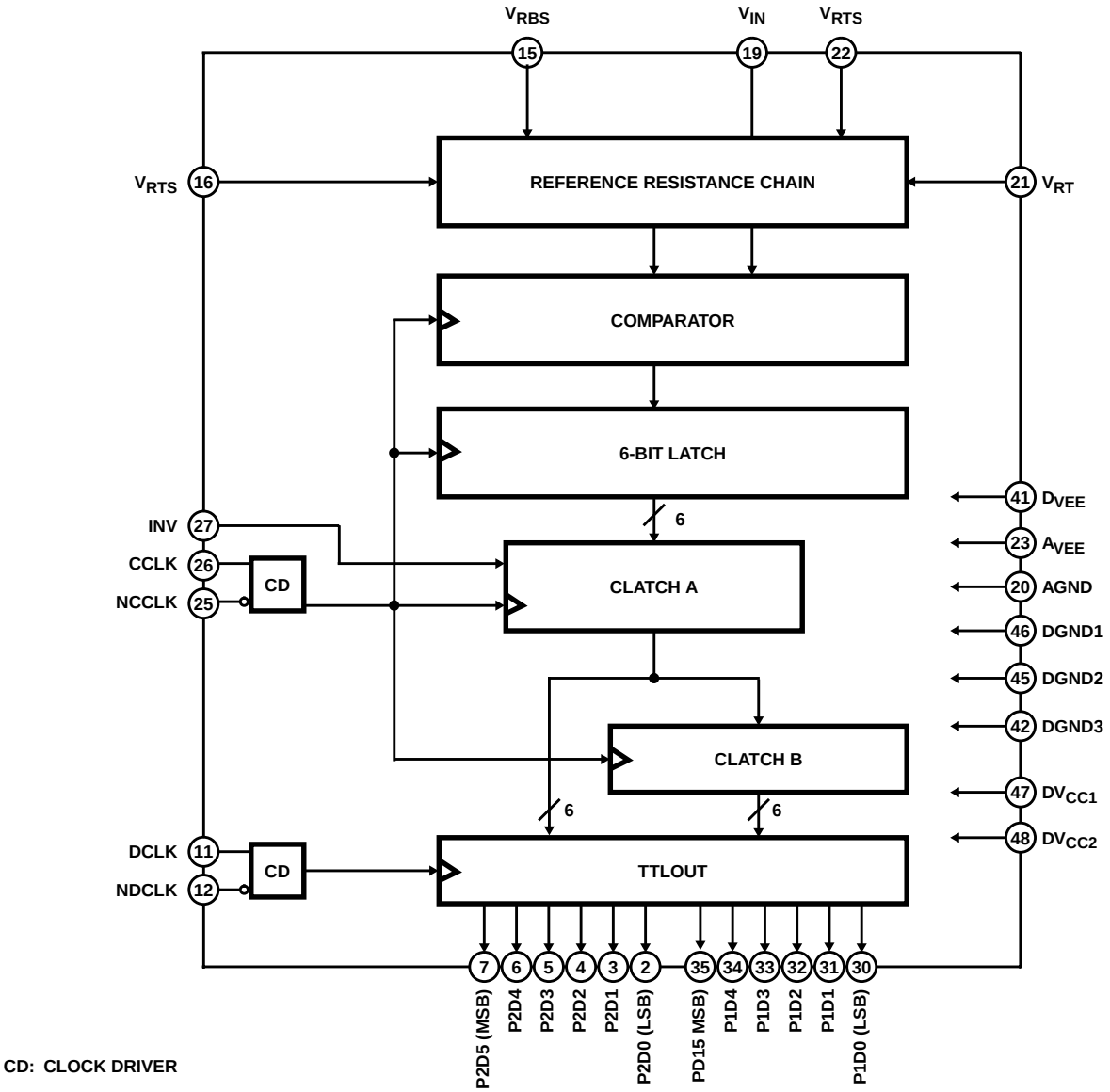
Pinout

HI1866
(MQFP)
TOP VIEW



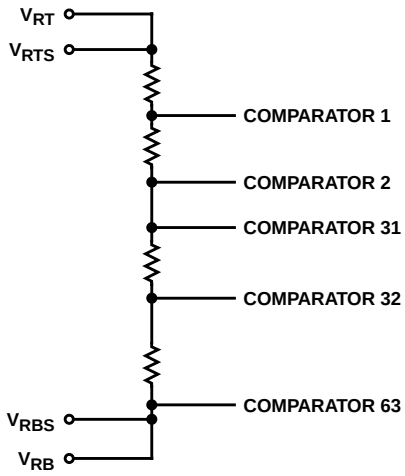
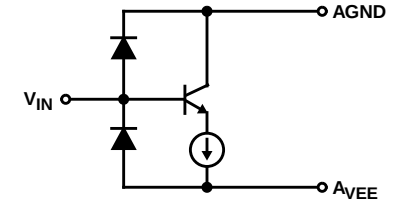
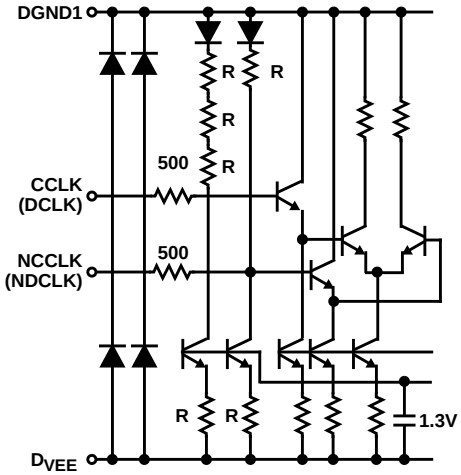
File Number **4108.2**

Functional Block Diagram

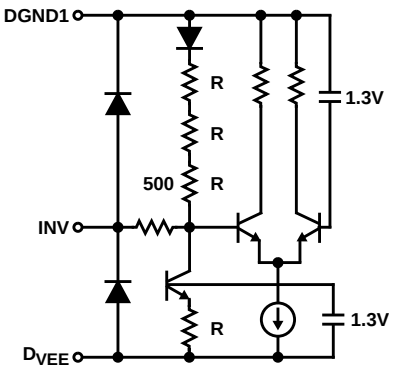
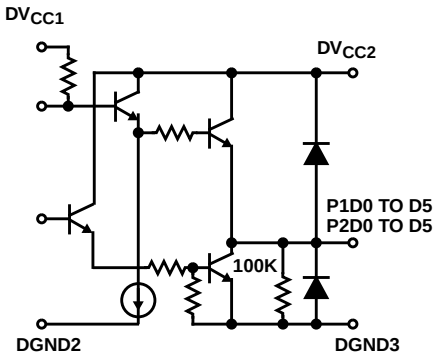


CD: CLOCK DRIVER

Pin Descriptions

PIN NO.	SYMBOL	I/O	TYPICAL VOLTAGE LEVEL	EQUIVALENT CIRCUIT	DESCRIPTION
21	V_{RT}	I	0V		Top reference voltage input (= 0). This is the top reference voltage supplied to the internal resistance chain. The external input can be set in accordance with the peak value on the plus side of the input analog signal amplitude.
22	V_{RTS}	O	0V		V_{RT} sense output. This is the voltage sense pin for V_{RT}.
16	V_{RB}	I	-2V		Bottom reference voltage input (= -2V). This is the bottom reference voltage supplied to the internal resistance chain. The external input can be set in accordance with the peak value on the minus side of the input analog signal amplitude.
15	V_{RBS}	O	-2V		V_{RB} sense output. This is the voltage sense pin for V_{RB}.
19	V_{IN}	I	V_{RTS} to V_{RBS}		Analog input. The input range is $2V_{P-P}$.
26	CCLK	I	ECL		CCLK clock input. This is the conversion clock, and is an ECL level input.
25	NCCLK	I	ECL		CCLK inversion clock input. This is an ECL level input. When left open, this input goes to the ECL threshold potential (-1.3V). Only CCLK input can be used for operation with the NCCLK input left open, but complementary input is recommended to attain fast and stable operation.
11	DCLK	I	ECL		DCLK clock input. This is the 1:2 DMPX latch clock; input a clock of $^1/_2$ frequency of CCLK. Data is output from DMPX port 1 and port 2 synchronously with the rising edge of this signal. This is an ECL level input.
12	NDCLK	I	ECL		DCLK inversion clock input. This is an ECL level input. When left open, this input goes to the ECL threshold potential (-1.3V). Only DCLK input can be used for operation with the NDCLK input left open, but complementary input is recommended to attain fast and stable operation.

Pin Descriptions (Continued)

PIN NO.	SYMBOL	I/O	TYPICAL VOLTAGE LEVEL	EQUIVALENT CIRCUIT	DESCRIPTION
27	INV	I	ECL		Digital output polarity inversion input. This is an ECL level input. This input inverts the polarity of the digital outputs P1D0 to P1D5, and P2D0 to P2D5. (Refer to the Output Code Table.) When left open, this signal is maintained at the low level.
30	P1D0	O	TTL		These pins are for the 6 bits of digital output data for DMPX port 1. P2D5 is the MSB, and P2D0 is the LSB. These are TTL levels outputs.
31	P1D1				
32	P1D2				
33	P1D3				
34	P1D4				
35	P1D5				
2	P2D0				These pins are for the 6 bits of digital output data for DMPX port 2. P2D5 is the MSB, and P2D0 is the LSB. These are TTL level outputs.
3	P2D1				
4	P2D2				
5	P2D3				
6	P2D4				
7	P2D5				
38, 47	DVCC1	-	+5.0V		+5V power supply for TTL level internal circuit.
9, 28, 37, 43, 48	DVCC2	-	+5.0V		+5V power supply for TTL level output buffers (P1D0 to P2D5).
39, 46	DGND1	-	0V		Ground for DV_{EE} digital circuit.
40, 45	DGND2	-	0V		Ground for DV_{CC1} digital circuit.
1, 8, 29, 36, 42	DGND3	-	0V		Ground for DV_{CC2} digital circuit.
17, 20	AGND	-	0V		Ground for AV_{EE} analog circuit. Used as the ground for the comparator input buffers, latches, etc. Separated from DGND.
41, 44	DV_{EE}	-	-5.2V		-5.2V power supply for digital circuit. Connected internally with AV_{EE}. (Resistance is 4Ω to 6Ω.)
14, 23	AV_{EE}	-	-5.2V		-5.2V power supply for analog circuit. Connected internally with DV_{EE}. (Resistance is 4Ω to 6Ω.)

Absolute Maximum Ratings

Supply Voltage (AV_{EE}, DV_{EE}) . . . . . -7V to 0.5V
(DV_{CC}) (Note 2) . . . . . 0.5V to 7.0V
Reference Voltage (V_{RT}, V_{RB}) . . . . . -2.7V to 0.5V
($|V_{RT} - V_{RB}|$) 2.5V
Analog Input Voltage (V_{IN}) . . . . . -2.7V to 0.5V
Digital Input Voltage (DIN) (Note 3) . . . . . -4.0V to 0.5V
($|CCLK–NCCLK|$, $|DCLK–NDCLK|$) 2.5V
Digital Output Current (I_{D0} to I_{D6}) . . . . . -30mA to +30mA
Storage Temperature (T_{STG}) . . . . . -65^oC to 150^oC
Ambient Operating Temperature (T_A) . . . . . -20^oC to 75^oC
Allowable Power Dissipation (P_D) 750mW

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} ($^oC/W$)
MQFP Package	95

Maximum Junction Temperature . . . . . 150^oC
Maximum Storage Temperature Range (T_{STG}) . . . -65^oC to 150^oC
Maximum Lead Temperature (Soldering 10s) . . . . . 300^oC
(Lead Tips Only)

Recommended Operating Conditions

Supply Voltage	MIN	TYP	MAX
AV_{EE}, DV_{EE}	-5.5V	-5.2V	-4.75V
AV_{EE} - DV_{EE}	-0.05V	0V	0.05V
AGND - DGND (Note 4)	- 0.05V	0V	0.05V
DV_{CC} (Note 5)	4.75V	5.0V	5.25V
Temperature Range (T_A)	-20^oC	-	75^oC

Reference Input Voltage	MIN	TYP	MAX
V_{RT}	-0.1V	0V	0.1V
V_{RB}	-2.2V	-2.0V	-0.8V
Analog Input Voltage (V_{IN})	V_{RB}	To	V_{RT}
Digital Input Voltage, DIN (H)	-1.1V	-	-
DIN (L)	-	-	-1.5V
CCLK, NCCLK Frequency (f_{CCLK})(MHz)	-	-	140
DCLK, NDCLK Frequency (f_{DCLK})(MHz)	-	-	70
CCLK, NCCLK Duty (D_{CCLK})(%)	40	50	60
DCLK, NDCLK Duty (D_{DCLK})(%)	40	50	60
CCLK-DCLK Time Difference (t_{DCD})(ns)	$-t_{PWL} + 2$	0	$t_{PWH} + 1$

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.
2. $DV_{CC} = DV_{CC1}, DV_{CC2}$.
3. D_{IN} = CCLK, NCCLK, DCLK, NDCLK, INV.
4. DGND = DGND1, DGND2, DGND3.
5. Refer to Timing Chart 1 for t_{PWL}, t_{PWH}.

Electrical Specifications

$T_A = 25^oC$, $AV_{EE} = DV_{EE} = -5.2V$, $DV_{CC} = 5V$, $V_{RT} = 0V$, $V_{RB} = -2V$

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Resolution, n	n		-	6	-	bits
DC CHARACTERISTICS						
Integral Linearity Error	E_{IL}	f_C = 140MHz	-	-	±0.2	LSB
Differential Linearity Error	E_{DL}	f_C = 140MHz	-	-	±0.2	LSB
No Missing Code			-	Guar-anteed	-	-
ANALOG INPUT						
Analog Input Capacitance	C_{IN}	$V_{IN} = -1V\_0.7V_{RMS}$, DC	-	7	-	pF
Analog Input Resistance	R_{IN}	$-2V \leqq V_{IN} \leqq 0V$	200	-	-	KΩ
Input Bias Current	I_{IN}	$-2V \leqq V_{IN} \leqq 0V$	-	-	110	µA
REFERENCE INPUT						
Reference Resistance	R_{REF}		-	225	-	Ω
Reference Resistance Current	I_{REF}		-	9	-	mA
Offset Voltage V_{RT}	E_{OT}		0	-	25	mV
V_{RB}	E_{OB}		-	-	25	mV
DIGITAL INPUT						
Logic High Level	V_{IH}		-1.13	-	-	V

Electrical Specifications $T_A = 25^oC$, $AV_{EE} = DV_{EE} = -5.2V$, $DV_{CC} = 5V$, $V_{RT} = 0V$, $V_{RB} = -2V$ **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Logic Low Level	V_{IL}		-	-	-1.50	V
Logic High Current	I_{IH}	$V_{IH} = -0.8V$	0	-	50	µA
Logic Low Current	I_{IL}	$V_{IL} = -1.6V$	-50	-	50	µA
Input Capacitance			-	3.5	-	pF
SWITCHING CHARACTERISTICS						
Maximum Conversion Frequency	f_C	Error Rate $1E^{-9}$ TPS (Note 1)	140	-	-	MSPS
Aperture Jitter	t_{AJ}		-	5.0	-	ps
Sampling Delay	t_{DS}		-	1.0	-	ns
DIGITAL OUTPUT						
Logic High Level	V_{OH}	$I_{OUT} = -2mA$	2.7	-	-	V
Logic Low Level	V_{OL}	$I_{OUT} = 1mA$	-	-	0.5	V
Output Delay	t_{DO}	$Z_L = 25pF$	2.0	-	8.0	ns
Output Rising Time	t_r	$Z_L = 25pF$, 0.5V to 2.4V	-	1.2	-	ns
Output Falling Time	t_f	$Z_L = 25pF$, 0.5V to 2.4V	-	1.2	-	ns
DYNAMIC CHARACTERISTICS						
Analog Amplitude Input Bandwidth	F_{INB}	$V_{IN} = 2V_{P-P}$, Peak-to-Peak Value = 3dB Down Input Frequency	210	-	-	MHz
S/N Ratio	SNR1 SNR2 SNR3	$f_C = 140MHz$, $f_{IN} = 1MHz$ $f_C = 140MHz$, $f_{IN} = 35MHz$ $f_C = 140MHz$, $f_{IN} = 70MHz$	-	36 34 32	-	dB dB dB
Error Rate		$f_C = 140MHz$, Error > 4 LSB	-	-10^{-9}	-	TPS (Note 1)
POWER SUPPLY						
Supply Current	I_{CC} I_{EE}	$DV_{CC} = +5V$ $AV_{EE} = DV_{EE} = -5.2V$	- -60	20 -40	32 -	mA mA
Power Consumption	P_D		-	325	-	mW

NOTE:

1. TPS: Times Per Sample

Output Code Table

V_{IN}	STEP	DINV: 1 D5 D0	INV:0 D5 D0
0V	0	000000	111111
	1	000001	111110
		•	•
		•	•
		•	•
-1V	31	011111	100000
	32	100000	011111
		•	•
		•	•
		•	•
	62	111110	000001
-2V	63	111111	000000

NOTE: $V_{RT} = 0V$, $V_{RB} = -2V$.

Timing Diagrams

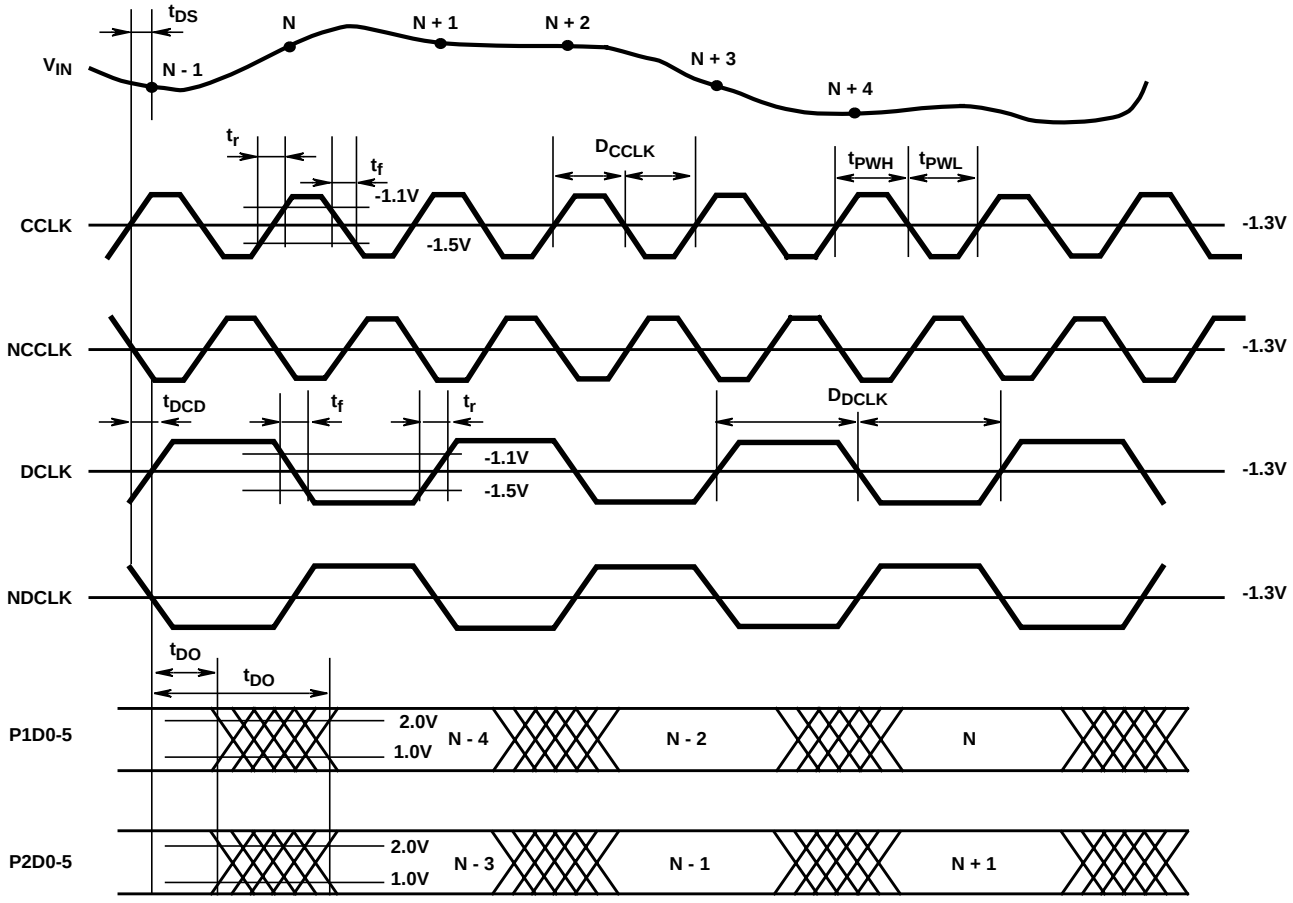
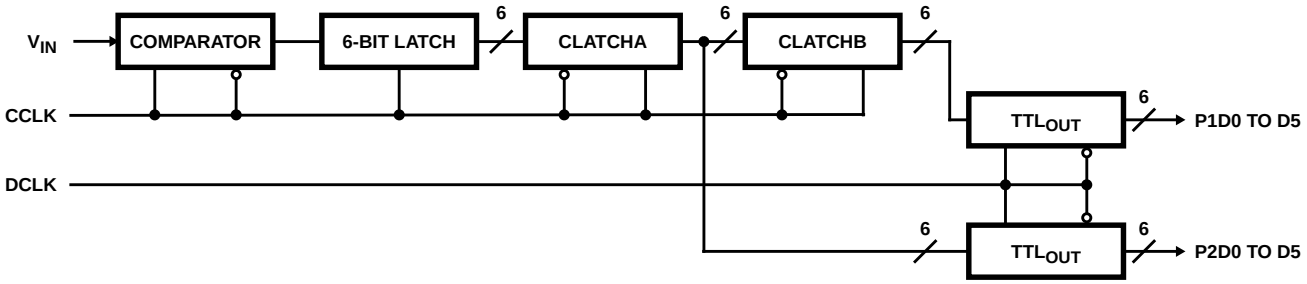


FIGURE 1. TIMING CHART 1

Timing Diagrams (Continued)



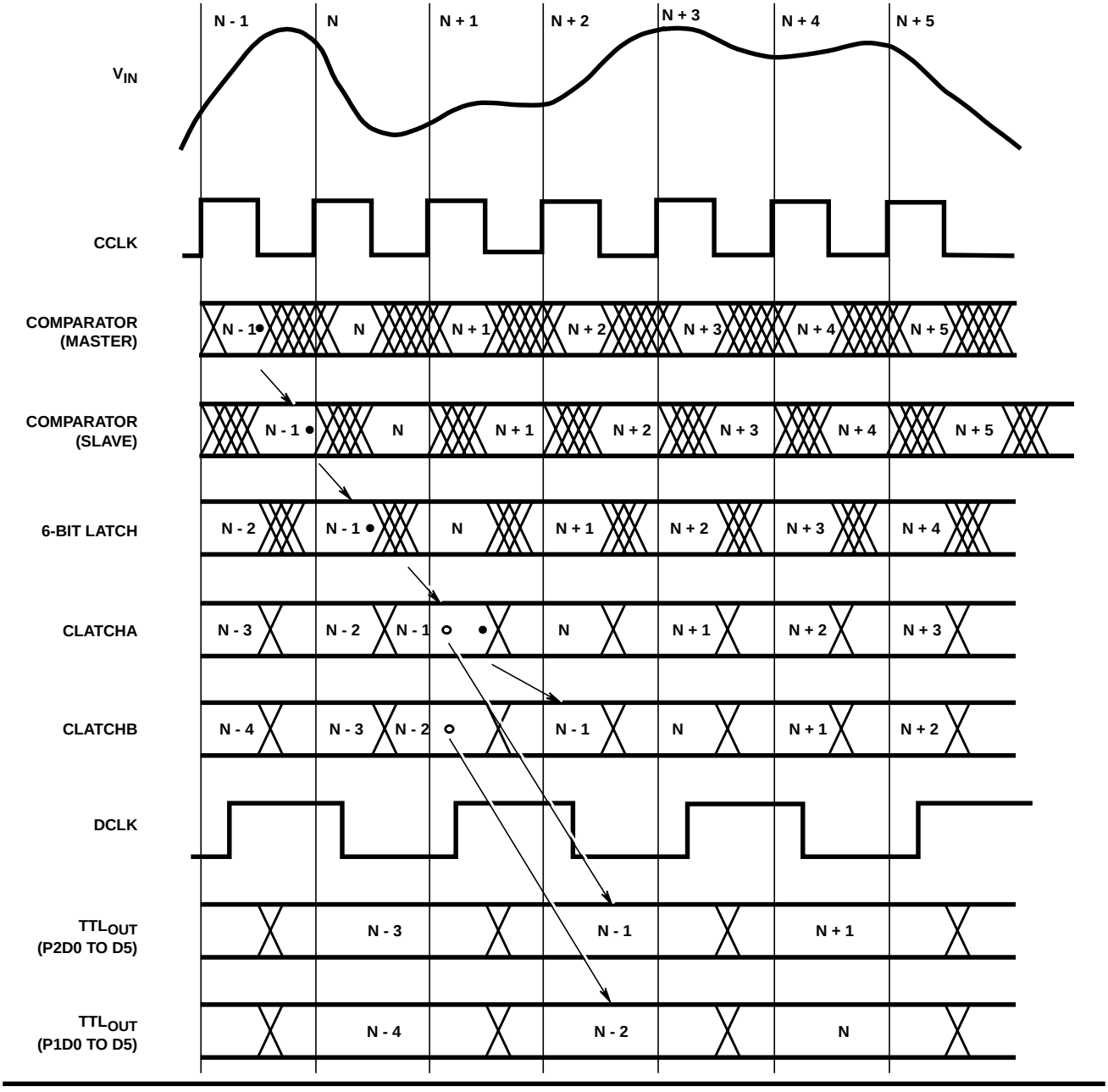


FIGURE 2. TIMING CHART 2

Test Circuits

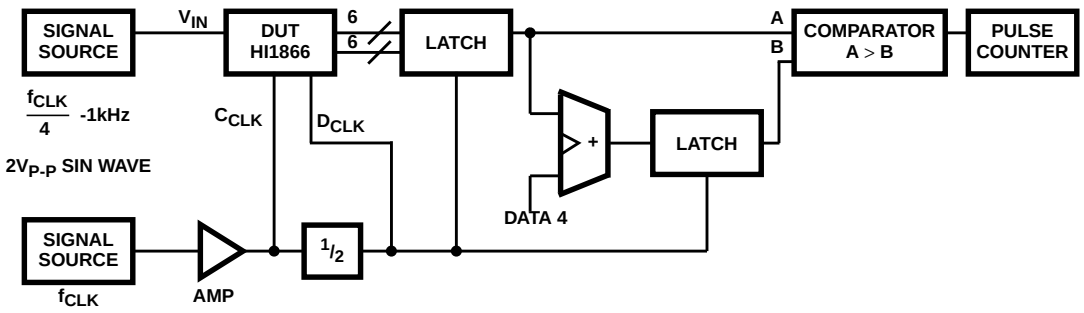


FIGURE 3. MAXIMUM CONVERSION RATE TEST CIRCUIT

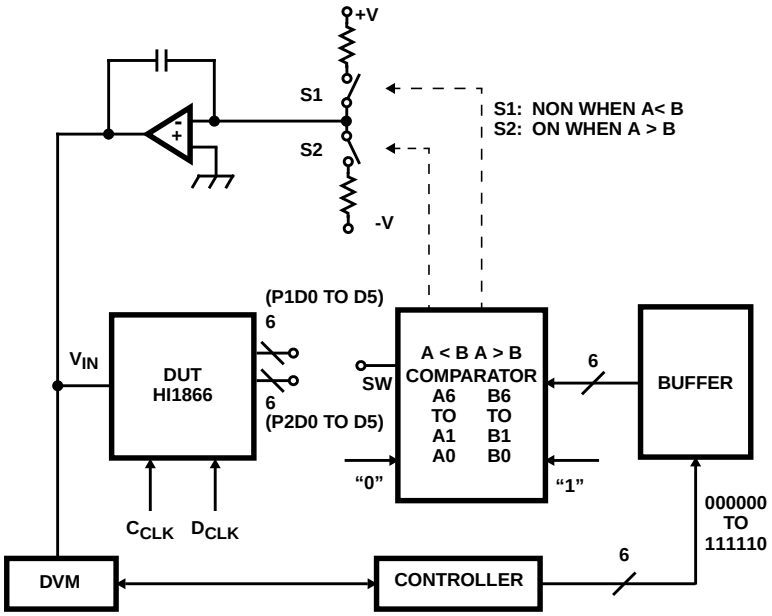


FIGURE 4. INTEGRAL/DIFFERENTIAL LINEARITY ERROR TEST CIRCUIT

Test Circuits (Continued)

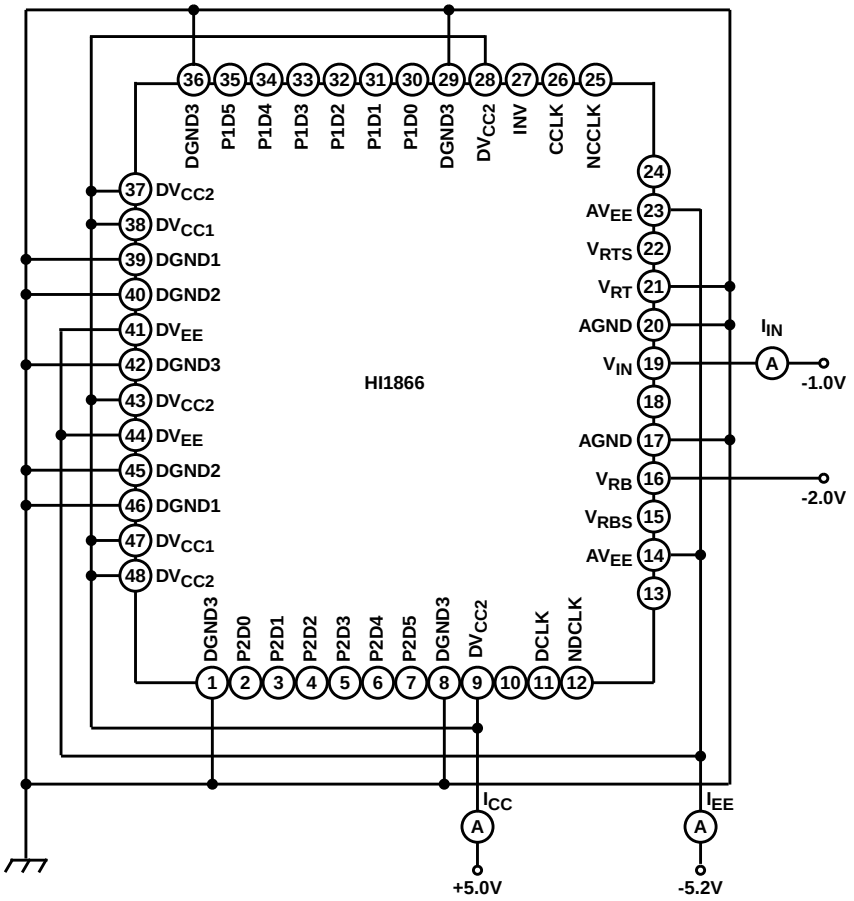


FIGURE 5. CURRENT CONSUMPTION/ANALOG INPUT BIAS TEST CIRCUIT

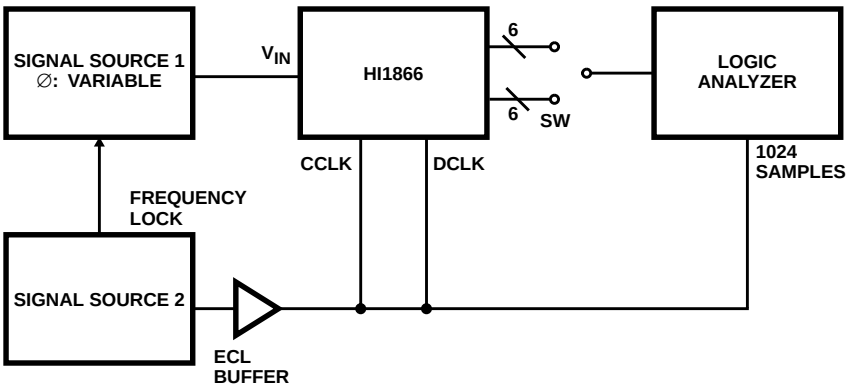


FIGURE 6. SAMPLING DELAY/APERTURE JITTER TEST CIRCUIT

Typical Performance Curves

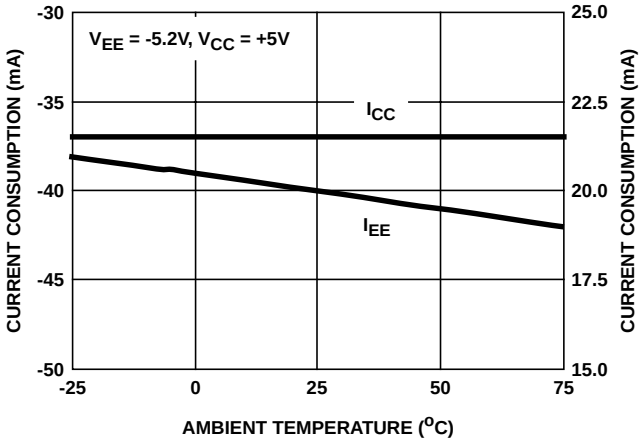


FIGURE 7. CURRENT CONSUMPTION vs AMBIENT TEMPERATURE

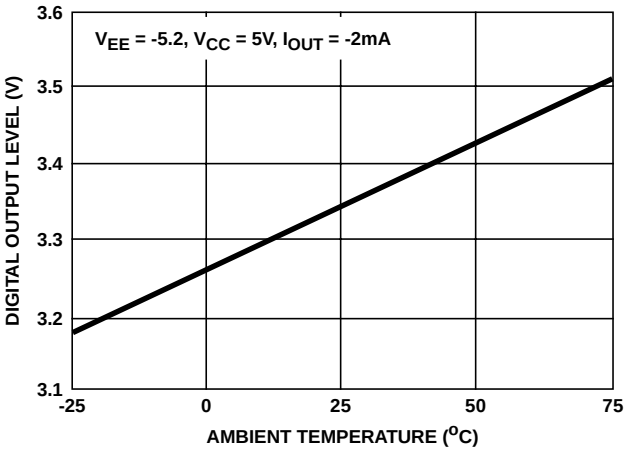


FIGURE 8. V_{OH} vs AMBIENT TEMPERATURE

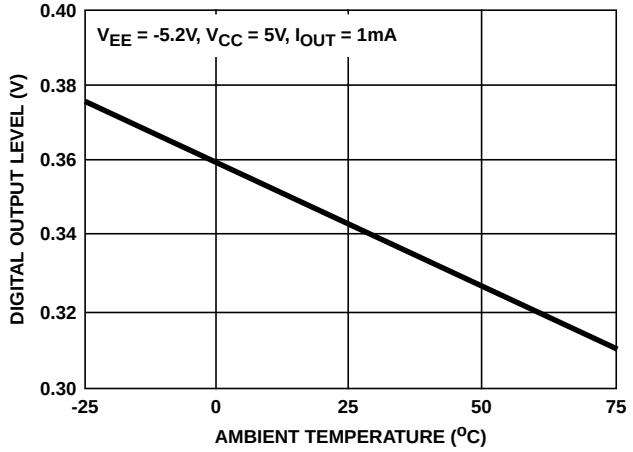


FIGURE 9. V_{OL} vs AMBIENT TEMPERATURE

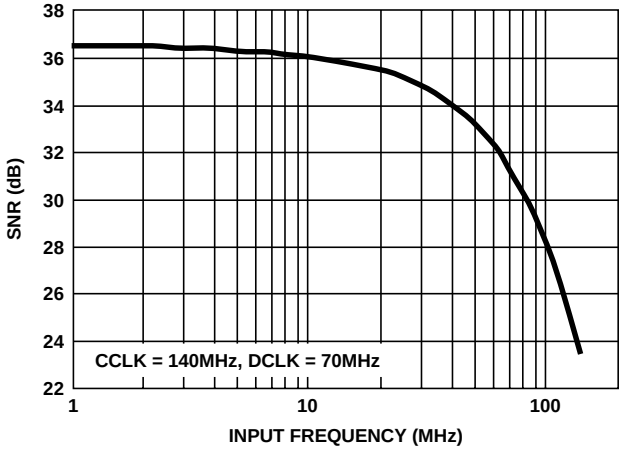


FIGURE 10. SNR vs INPUT FREQUENCY

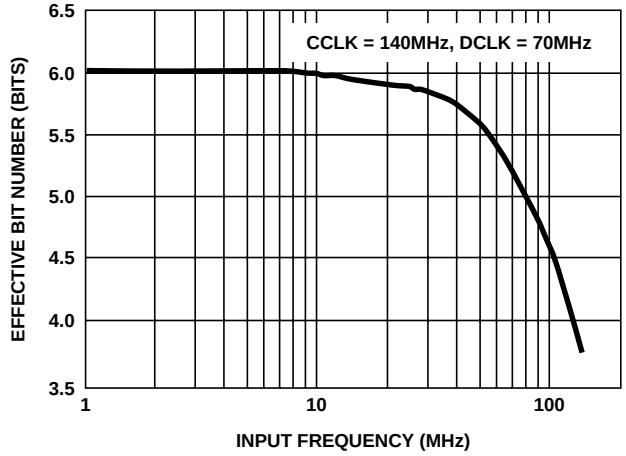


FIGURE 11. EFFECTIVE BIT NUMBER vs INPUT FREQUENCY

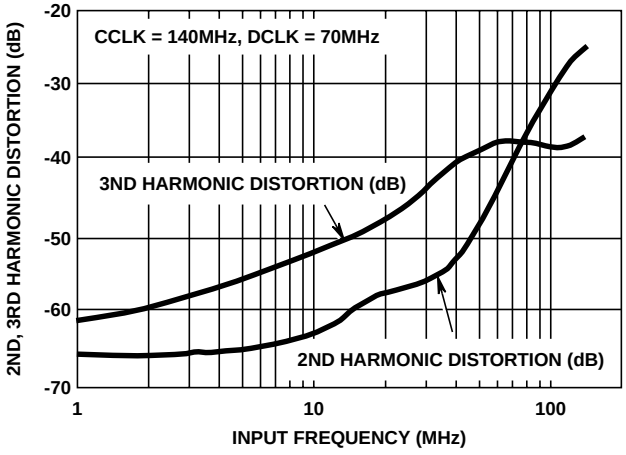


FIGURE 12. 2ND, 3RD HARMONIC DISTORTION vs INPUT FREQUENCY

Notes on Operation

The HI1186 is a high speed A/D converter with ECL level logic input and demultiplexed TT level output. Take notice of the following to ensure optimum performance from this IC.

Power Supply and Grounding

Grounding has a profound influence on converter performance. The higher the frequency is, the more important the way of grounding becomes.

The ground pattern should be as large as possible. It is recommended to make the power supply and ground patterns wider at an inner layer using the multi-layer board.

To prevent interference between the AGND and DGND patterns and between the AV_{EE} and DV_{EE} lines, make sure the respective patterns are separated. To prevent a DC offset in the power supply pattern, connect the AV_{EE} and DV_{EE} lines at one point each via a ferrite-bead filter. Shorting analog and digital ground patterns in one place immediately under the A/D converter improves A/D converter performance.

Ground the power supply pins (AV_{EE}, DV_{EE}, DV_{CC}) as close to each pin as possible with a 0.1µF or larger ceramic chip capacitor. (Connect the AV_{EE} pin to the AGND pattern, DV_{EE} to DGND, and DV_{CC} to DGND.)

Analog Input

Make the connection between the V_{IN} pin and the analog input source as short as possible.

There is a slight offset voltage at reference voltage pins V_{RT} and V_{RB}. If it presents no problem in the application, the voltage can be applied directly. However, if the reference voltage is to be set precisely, apply it via a feedback circuit created, using the V_{RTS} and V_{RBS} pins.

Make adequate bypass for high frequency noise at V_{RT} and V_{RB}. The V_{RT} pin is normally connected to AGND on the board. Bypass the V_{RB} pin to the AGND pattern with a 0.1µF or larger ceramic chip capacitor as short as possible. The 10µF tantalum capacitor connected to V_{RB} in the Application Circuit is to stop oscillation in the reference voltage generation circuit.

Digital Input

Noise at the INV pin may cause misoperation of which the cause is extremely hard to identify. If it is okay for the set voltage level to be low only, leave the pin open. If a high level voltage has to be input, bypass the INV pin to DGND with an about 0.1µF ceramic chip capacitor as short as possible. It is recommended that high level input voltage is about -0.5V to -1.0V, and low level input voltage is about -1.6V to -2.5V. When inputting a high level voltage, avoid connecting directly to DGND.

The HI1186 has input pins for two clocks: CCLK and DCLK. For CCLK, which is used for the internal comparator, input an ECL level clock with up to the maximum conversion frequency. For DCLK, which is used for the multiplex output, input an ECL level clock with a rate half that of CCLK. Take notice of the timing between CCLK and DCLK.

It is recommended that differential signals be input to the clock input pins CCLK, NCCLK, DCLK and NDCLK. The A/D converter can be driven only by the clock input pins CCLK and DCLK, but there is a risk of unstable characteristics at maximum speeds.

If the NCCLK and NDCLK pins are not used, bypass these pins to DGND with an about 0.1µF capacitor. In this time, about -1.3V voltage is generated at the NCCLK and NDCLK pins. However, this is too weak to be used as threshold voltage V_{BB}; it can not directly drive even one ECL input load.

The clock duty cycle is designed for use at 50%. Any diversion from this percentage will have a slight effect on the maximum performance of the A/D converter, but there is no great need for adjustment.

Digital Output

P1D0 (LSB) to P1D5 (MSB), and P2D0 (LSB) to P2D5 (MSB) are demultiplex digital outputs (2 systems), and are output using the DCLK timing. The polarity of the output data can be inverted using the INV signal.

Typical Application Circuit