# intersil

# HI2300

August 1997

## 8-Bit, 18 MSPS, Video A/D Converter with 3.3V Power Supply Operation

## Features

- **Resolution** . . . . . . . . . . . . . . . . . . . . **8-Bit** $\pm^1/_2$ **LSB (DL)**

- **Maximum Sampling Frequency** . . . . . . . . . . . **18 MSPS**

- **Low Power Consumption at 18 MSPS (Typ)
  (Reference Current Excluded)** . . . . . . . . . . . . . . **18mW**

- **Synchronizing Clamp Function**

- **Clamp ON/OFF Function**

- **Reference Voltage Self-Bias Circuit**

- **Input CMOS Compatible**

- **Three-State TTL Compatible Output**

- **Power Supply** . . . . . . . . . . . . . . . . . . . . . . . **3.3V Single**

- **Low Input Capacitance** . . . . . . . . . . . . . . . . . . . . . . . **8pF**

- **Reference Impedance** . . . . . . . . . . . . . . . . . . **330$\Omega$ (Typ)**

- **Direct Replacement for Sony CXD2300**

## Applications

- **Portable Equipment**

- **Hand-Held Instruments**

## Description

The HI2300 is an 8-bit, CMOS A/D converter for video with synchronizing clamp function and can operate on 3.3V power supply. The adoption of 2 step-parallel method achieves ultra-low power consumption and a maximum conversion speed of 18 MSPS.
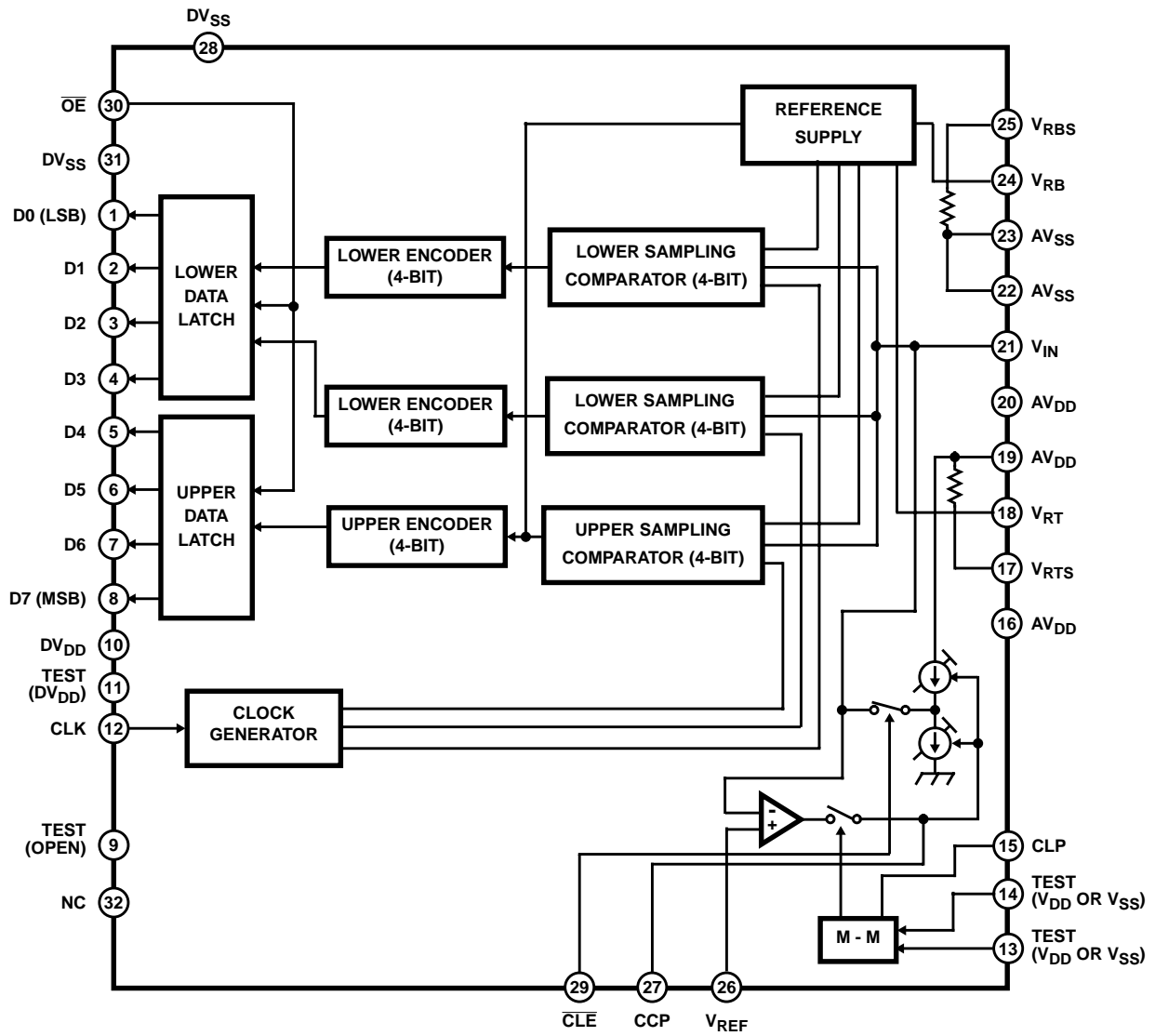
## Ordering Information

| PART NUMBER | TEMP. RANGE ($^o$C) | PACKAGE | PKG. NO. |
|---|---|---|---|
| HI2300JCQ | -40 to 85 | 32 Ld MQFP | Q32.7x7-S |

## Pinout



HI2300
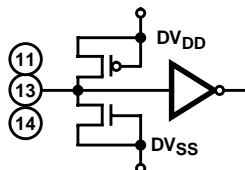(MQFP)
TOP VIEW

File Number **4103.1**
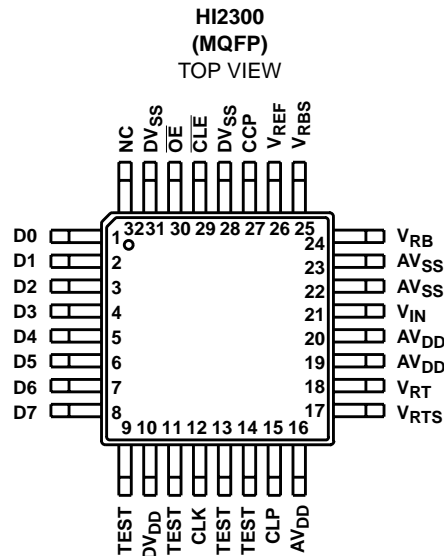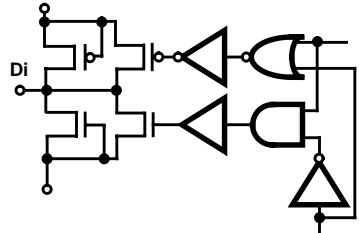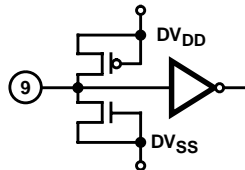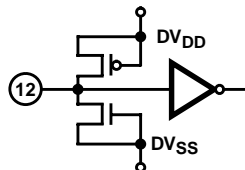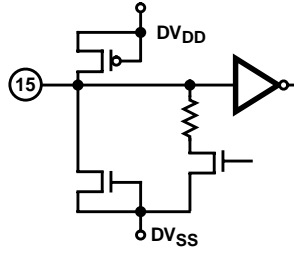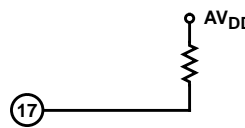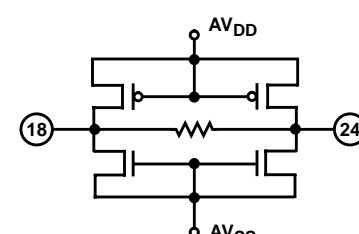
# Functional Block Diagram

# HI2300

## Pin Descriptions

| PIN NUMBER | SYMBOL | EQUIVALENT CIRCUIT | DESCRIPTION |
|---|---|---|---|
| 1 to 8 | D0 to D7 |  | D0 (LSB) to D7 (MSB) Output. |
| 9 | TEST |  | Leave open during normal usage. |
| 10 | $DV_{DD}$ | | Digital +3.3V. |
| 12 | CLK |  | Clock Input. |
| 11, 13, 14 | TEST |  | Fix Pin 11 to $V_{DD}$, Pins 13 and 14 to $V_{DD}$ or $V_{SS}$ during normal usage. |
| 15 | CLP |  | Inputs Clamp Pulse to Pin 15 (CLP). Clamps the signal voltage during Low interval. |
| 16, 19, 20 | $AV_{DD}$ | | Analog +3.3V |
| 17 | $V_{RTS}$ |  | Generates approximately +1.8V when shorted with $V_{RT}$. |
| 18 | $V_{RT}$ |  | Reference Voltage (Top). |
| 24 | $V_{RB}$ | | Reference Voltage (Bottom). |

## Pin Descriptions (Continued)

| PIN NUMBER | SYMBOL | EQUIVALENT CIRCUIT | DESCRIPTION |
|---|---|---|---|
| 21 | $V_{IN}$ | | Analog Input. |
| 25 | $V_{BRS}$ | | Generates approximately +0.4V when shorted with $V_{RB}$. |
| 26 | $V_{REF}$ | | Clamp Reference Voltage Input. Clamps so that the reference voltage and the input signal during clamp interval are equal. |
| 27 | CCP | | Integrates the clamp control voltage. The relationship between the changes in CCP voltage and in $V_{IN}$ voltage is positive phase. |
| 28, 31 | $DV_{SS}$ | | Digital Ground. |
| 29 | $\overline{CLE}$ | | The clamp function is enabled when $\overline{CLE}$ = Low. The clamp function is set to off and the converter functions as a normal A/D converter when $\overline{CLE}$ = High. The clamp pulse can be measured by connecting $\overline{CLE}$ to $DV_{DD}$ through a several-hundred-ohm resistor. |
| 30 | $\overline{OE}$ | | Data is output when $\overline{OE}$ = Low. Pins D0 to D7 are at high impedance when $\overline{OE}$ = High. |
| 32 | NC | | No Connect pin. |

## Absolute Maximum Ratings  $T_A = 25^oC$

Supply Voltage ($V_{DD}$) . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 7V
Reference Voltage ($V_{RT}$, $V_{RB}$) . . . . . . . . . $V_{DD}$ +0.5V to $V_{SS}$ - 0.5V
Input Voltage, Analog ($V_{IN}$) . . . . . . . . . . . $V_{DD}$ +0.5V to $V_{SS}$ - 0.5V
Input Voltage, Digital ($V_{IH}$, $V_{IL}$) . . . . . . . . $V_{DD}$ +0.5V to $V_{SS}$ - 0.5V
Output Voltage, Digital ($V_{OH}$, $V_{OL}$) . . . . . . $V_{DD}$ +0.5V to $V_{SS}$ - 0.5V

## Thermal Information

Thermal Resistance (Typical, Note 1)       $\theta_{JA}$ ($^oC$/W)
   MQFP Package . . . . . . . . . . . . . . . . . . . . . . . . . . . . .      122
Maximum Junction Temperature (Plastic Package) . . . . . . . . 150$^oC$
Maximum Storage Temperature Range . . . . . . . . . .-65$^oC$ to 150$^oC$
Maximum Lead Temperature (Soldering 10s) . . . . . . . . . . . . 300$^oC$
   (MQFP - Lead Tips Only)

## Recommended Operating Conditions

Temperature Range ($t_{OPR}$) . . . . . . . . . . . . . . . . . . . -40$^oC$ to 85$^oC$
Supply Voltage (IDV$_{SS}$ - AV$_{SS}$I) . . . . . . . . . . . . . . . . . . 0 to 100mV
Power Supply (DV$_{DD}$, DV$_{SS}$)(AV$_{DD}$, AV$_{SS}$) . . . . . . . .3.14V to 4.0V
Reference Input Voltage ($V_{RB}$) . . . . . . . . . . . . . . . . . . . . . . . . 0.4V
               ($V_{RT}$) . . . . . . . . . . . . . . . . . . . . . . . . . . .1.8V

Analog Input (ADIN) . . . . . . . . . . . . . . . . . . . . . . . . . . . .  $V_{RT}$ to $V_{RB}$
Clock Pulse width ($t_{PW1}$) . . . . . . . . . . . . . . . . . . . . . . . . 27ns (Min)
                 ($t_{PW0}$) . . . . . . . . . . . . . . . . . . . . . . . . 27ns (Min)

*CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.*

NOTE:

1. $\theta_{JA}$ is measured with the component mounted on an evaluation PC board in free air.

## Electrical Specifications

When using a single power supply; $f_C = 18$ MSPS, $V_{DD} = 3.3$V, $V_{RB} = 0$V, $V_{RT} = 1.5$V, $T_A = 25^oC$

| PARAMETER | SYMBOL | TEST CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| Maximum Conversion Rate | $f_C$ Max | $V_{IN}$ = 0 to 1.5V | | 18 | 32 | - | MSPS |
| Minimum Conversion Rate | $f_C$ Min | $f_{IN}$ = 1kHz Ramp | | - | 32 | 0.5 | MSPS |
| Supply Current | $I_{DD}$ | $f_C$ = 18 MSPS, NTSC Ramp Wave Input | | - | 5.5 | 10 | mA |
| Reference Pin Current | $I_{REF}$ | | | 3.3 | 4.6 | 6.6 | mA |
| Analog Input Band Width | BW | $V_{IN}$ = 1.4$V_{P-P}$, 17.9MHz | | - | -.9 | - | dB |
| Analog Input Capacitance | $C_{IN}$ | $V_{IN}$ = 0.75V + 0.07 $V_{RMS}$ | | - | 8 | - | pF |
| Reference Resistance ($V_{RT}$ to $V_{RB}$) | $R_{REF}$ | | | 230 | 330 | 440 | $\Omega$ |
| Self Bias I | $V_{RB1}$ | Shorts $V_{RB}$ and $V_{RBS}$ | | 0.33 | 0.36 | 0.39 | V |
| | $V_{RT1}$ - $V_{RB1}$ | Shorts $V_{RT}$ and $V_{RTS}$ | | 1.30 | 1.39 | 1.48 | V |
| Offset Voltage | $E_{OT}$ | | | -45 | -25 | -5 | mV |
| | $E_{OB}$ | | | 40 | 60 | 80 | mV |
| Digital Input Voltage | $V_{IH}$ | | | 2.5 | - | - | V |
| | $V_{IL}$ | | | - | - | 0.5 | V |
| Digital Input Current | $I_{IH}$ | $V_{DD}$ = Max | $V_{IH}$ = $V_{DD}$ | - | - | 5 | $\mu$A |
| | $I_{IL}$ | | $V_{IL}$ = 0V | - | - | - | $\mu$A |
| Digital Output Current | $I_{OH}$ | $\overline{OE}$ = $V_{SS}$ | $V_{OH}$ = $V_{DD}$ - 0.5V | -1.0 | - | - | mA |
| | $I_{OL}$ | $V_{DD}$ = Min | $V_{OL}$ = 0.4V | 3.3 | - | - | mA |
| Digital Output Current | $I_{OZH}$ | $\overline{OE}$ = $V_{DD}$ | $V_{OH}$ = $V_{DD}$ | - | - | 16 | $\mu$A |
| | $I_{OZL}$ | $V_{DD}$ = Max | $V_{OL}$ = 0V | - | - | 16 | $\mu$A |
| Output Data Delay | $t_{DL}$ | With TTL 1 Gate and 10pF Load | | 8 | 18 | 30 | ns |
| Three-State Output Enable Time | $t_{PZH}$ | $R_L$ = 1k$\Omega$, $C_L$ = 20pF, $\overline{OE}$ = 3V$\rightarrow$0V | | | | | |
| | $t_{PZL}$ | | | | | | |
| Three-State Output Disable Time | $t_{PHZ}$ | $R_L$ = 1k$\Omega$, $C_L$ = 20pF, $\overline{OE}$ = 0V$\rightarrow$3V | | | | | |
| | $t_{PLZ}$ | | | | | | |
| Integral Nonlinearity Error | $E_L$ | $f_C$ = 18 MSPS $V_{IN}$ = 0 to 1.5V | | - | +0.5 | $\pm$1.3 | LSB |
| Differential Nonlinearity Error | $E_D$ | $f_C$ = 18 MSPS $V_{IN}$ = 0 to 1.5V | | - | $\pm$0.3 | $\pm$0.5 | LSB |
| Aperture Jitter | $t_{AJ}$ | | | - | 30 | - | ps |
| Sampling Delay | $t_{SD}$ | | | - | 4 | - | ns |
| Clamp Offset Voltage | $E_{OC}$ | $V_{IN}$ = DC | $V_{REF}$ = 0.5V | -20 | 0 | +20 | mV |
| | | PWS = 3$\mu$s | $V_{REF}$ = 1.5V | -30 | -10 | +10 | mV |
| Clamp Pulse Delay | $t_{CPD}$ | | | - | 25 | - | ns |

**Digital Output**

The following table shows the relationship between analog input voltage and digital output code.

| INPUT SIGNAL VOLTAGE | STEP | DIGITAL OUTPUT CODE | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | MSB | | | | | | | LSG |
| $V_{RT}$ | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| • | • | | | | • | | | | |
| • | • | | | | • | | | | |
| • | • | | | | • | | | | |
| • | 127 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| • | 128 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| • | • | | | | • | | | | |
| • | • | | | | • | | | | |
| • | • | | | | • | | | | |
| $V_{RB}$ | 255 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

## *Timing Chart*



**o:** Analog Sampling Point
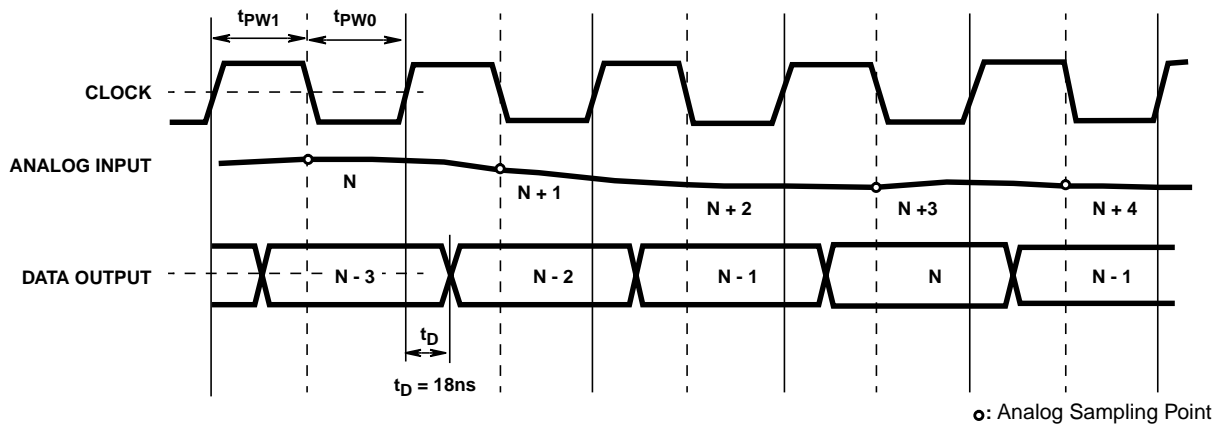
## *Typical Application Circuits*
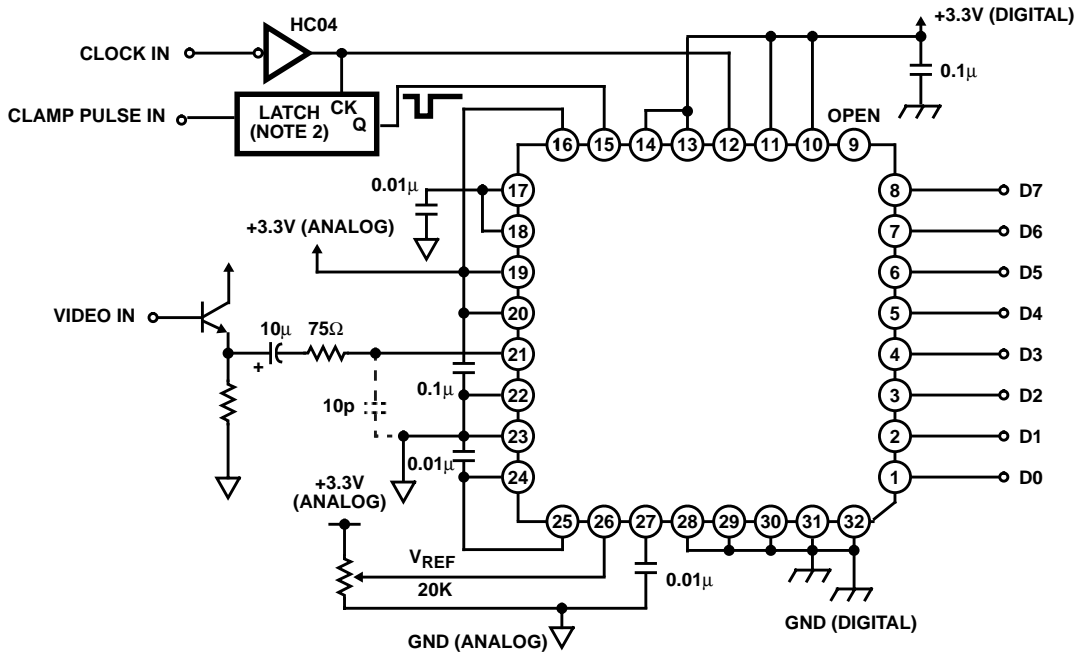


NOTE:

1. The clamp pulse is latched by the sampling clock of ADC, but that is not necessary for basic clamp operaiotn. However, slight small beat may be generated as Vertical sag according to the relationship between the sampling frequency and the clamp pulse frequency. At such time, the latch circuit is efective in this case.

**FIGURE 1.  WHEN CLAMP IS USED (SELF BIAS)**
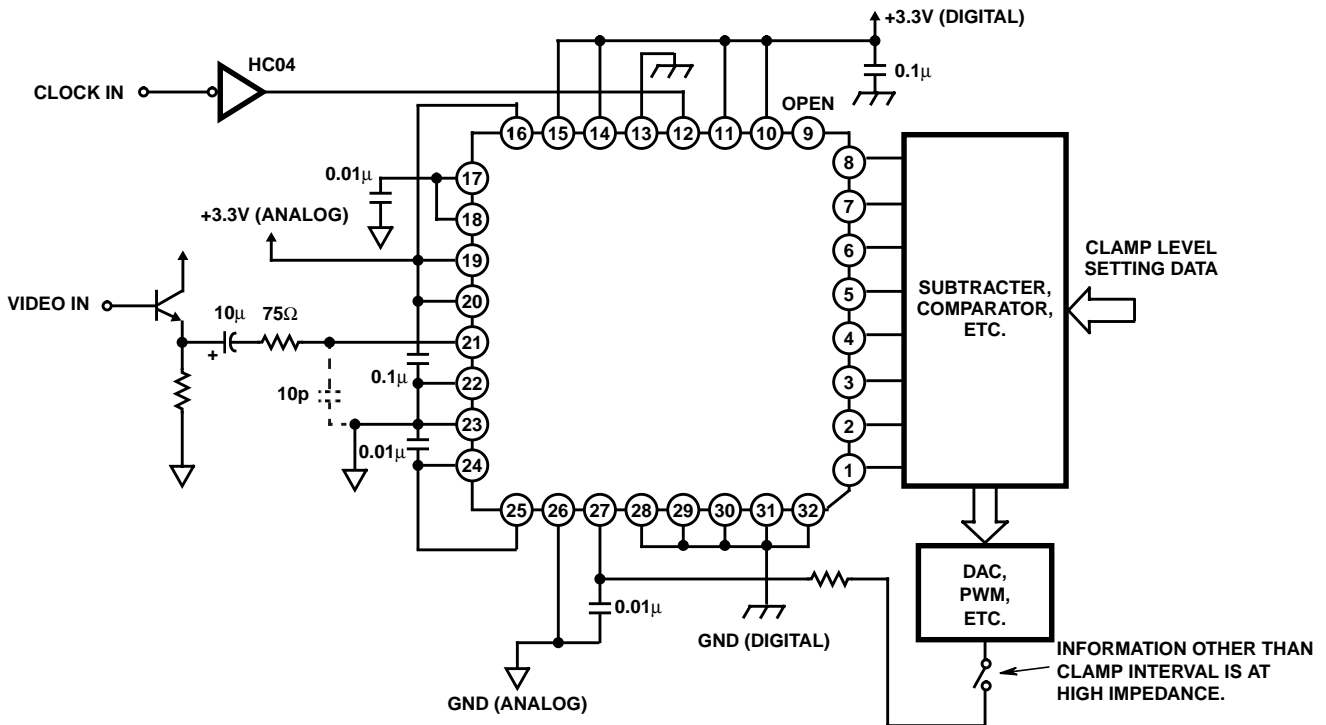


NOTES:

2. The relationship between the changes in CCP voltage (Pin 27) and in $V_{IN}$ voltage is positive phase.

3. $\Delta V_{IN}/\Delta V_{CCP} = 3.0$ ($f_S$ = 20 MSPS).

**FIGURE 2.  DIGITAL CLAMP (SELF BIAS)**

## *Typical Application Circuits* (Continued)

+3.3V (DIGITAL)

HCO4

CLOCK IN

0.1μ

OPEN

16 15 14 13 12 11 10 9

17

18

19

20

21

22

23

24

8 ○ D7

7 ○ D6

6 ○ D5

5 ○ D4

4 ○ D3

3 ○ D2

2 ○ D1

1 ○ D0

25 26 27 28 29 30 31 32

+3.3V (ANALOG)

0.01μ

VIDEO IN

75

0.1μ

10p

0.01μ

GND (ANALOG)

+3.3V (DIGITAL)

GND (DIGITAL)
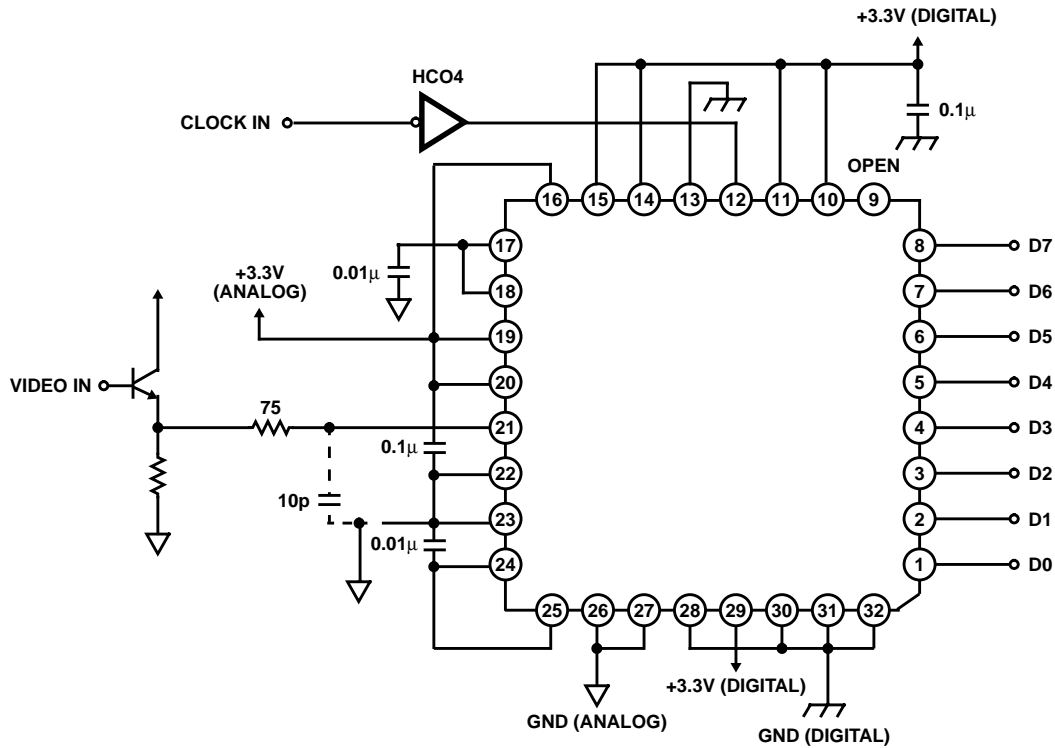
**FIGURE 3. WHEN CLAMP IS NOT USED (SELF BIAS)**