HM-6642/883

March 1997

512 x 8 CMOS PROM

Features

- **This Circuit is Processed in Accordance to MIL-STD-883 and is Fully Conformant Under the Provisions of Paragraph 1.2.1.**
- **Low Power Standby and Operating Power**
  - **ICCSB 100µA**
  - **ICCOP . . . . . 20mA at 1MHz**
- **Fast Access Time 120/200ns**
- **Wide Operating . . . . . -55°C to +125°C**
- **Temperature Range**
- **Industry Standard Pinout**
- **Single 5.0V Supply**
- **CMOS/TTL Compatible Inputs**
- **Field Programmable**
- **Synchronous Operation**
- **On-Chip Address Latches**
- **Separate Output Enable**

Ordering Information

PACKAGE	TEMP. RANGE	120ns	200ns	PKG. NO.
SBDIP	-55°C to +125°C	HM1-6642B/883	HM1-6642/883	D24.6
SLIM SBDIP	-55°C to +125°C	HM6-6642B/883	HM6-6642/883	D24.3
CLCC	-55°C to +125°C	-	HM4-6642/883	J28.A

Description

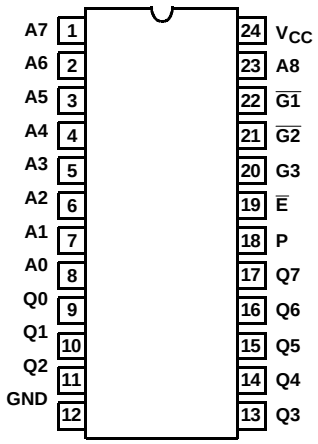
The HM-6642/883 is a 512 x 8 CMOS NiCr fusible link Programmable Read Only Memory in the popular 24 pin, byte wide pinout. Synchronous circuit design techniques combine with CMOS processing to give this device high speed performance with very low power dissipation.

On-chip address latches are provided, allowing easy interfacing with recent generation microprocessors that use multiplexed address/data bus structures, such as the 8085. The output enable controls, both active low and active high, further simplify microprocessor system interfacing by allowing output data bus control independent of the chip enable control. The data output latches allow the use of the HM-6642/883 in high speed pipelined architecture systems, and also in synchronous logic replacement functions.

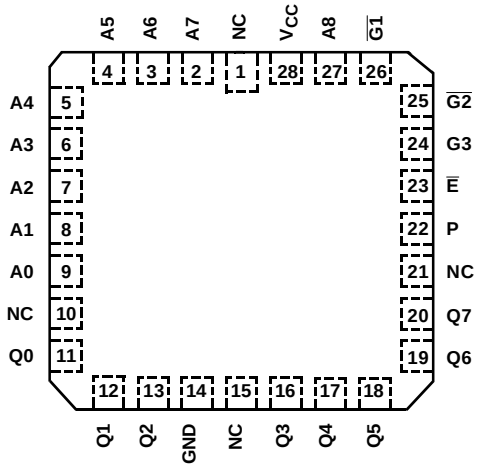
Applications for the HM-6642/883 CMOS PROM include low power hand held microprocessor based instrumentation and communications systems, remote data acquisition and processing systems, processor control store, and synchronous logic replacement.
All bits are manufactured storing a logical “0” and can be selectively programmed for a logical “1” at any bit location.

Pinouts

M-6642/883 (BDIP)
TOP VIEW



HM-6642/883 (CLCC)
TOP VIEW

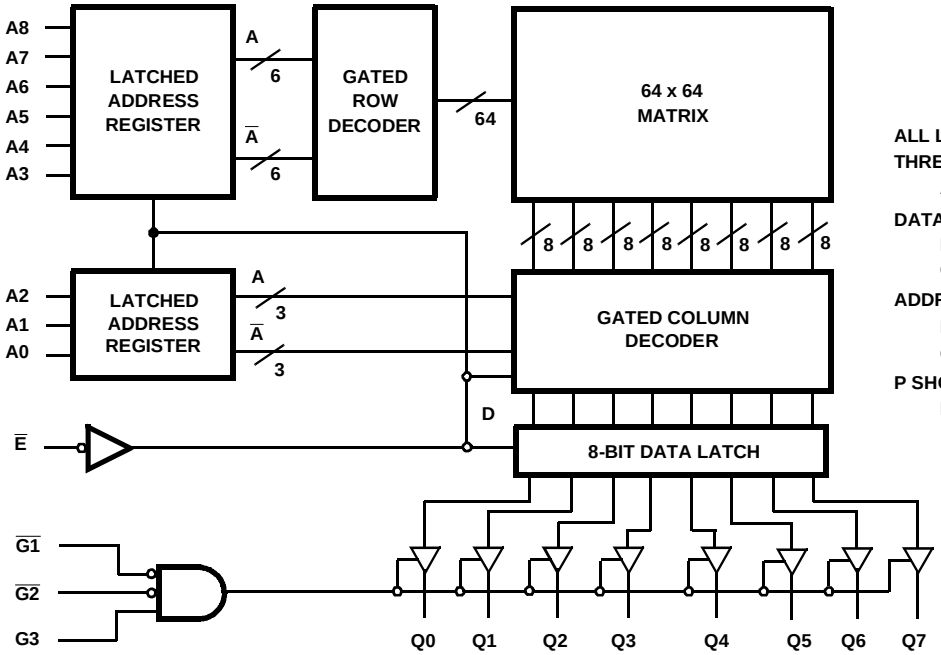


PIN DESCRIPTION

PIN	DESCRIPTION
NC	No Connect
A0-A8	Address Inputs
$\overline{E}$	Chip Enable
Q	Data Output
V_{CC}	Power (+5V)
$\overline{G1}$, $\overline{G2}$, G3	Output Enable
P (Note)	Program Enable

NOTE: P should be hardwired to GND except during programming.

Functional Diagram



ALL LINES POSITIVE LOGIC - ACTIVE HIGH

THREE STATE BUFFERS:

A HIGH → OUTPUT ACTIVE

DATA LATCHES:

L HIGH → Q = D

Q LATCHES ON RISING EDGE OF $\overline{E}$

ADDRESS LATCHES AND GATED DECODERS:

LATCH ON FALLING EDGE OF $\overline{E}$

GATE ON FALLING EDGE OF $\overline{E}$

P SHOULD BE HARDWIRED TO GND EXCEPT DURING PROGRAMMING

Absolute Maximum Ratings

Supply Voltage . . . . . +7.0V
Input, Output or I/O Voltage . . . . . GND-0.3V to VCC+0.3V
Typical Derating Factor . . . . . 5mA/MHz Increase in ICCOP
ESD Classification . . . . . Class 1

Operating Conditions

Operating Voltage Range . . . . . ±4.5V
Operating Temperature Range. . . . . -55^oC to $+125^oC$
Input Low Voltage. . . . . -0.3V to +0.8V
Input High Voltage . . . . . 2.4 to VCC+0.3V

Thermal Information

Thermal Resistance (Typical)	θ_{JA}	θ_{JC}
SBDIP Package.	$52^oC/W$	$14^oC/W$
Slim SBDIP	$70^oC/W$	$19^oC/W$
CLCC Package	$58^oC/W$	$14^oC/W$

Maximum Storage Temperature Range . . . . . -65^oC to $+150^oC$
Maximum Junction Temperature. . . . . $+175^oC$
Maximum Lead Temperature (Soldering 10s). . . . . $+300^oC$

Die Characteristics

Gate Count . . . . . 1680 Gates

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

TABLE 1. HM-6642/883 DC ELECTRICAL PERFORMANCE SPECIFICATIONS

Device Guaranteed and 100% Tested

PARAMETER	SYMBOL	(NOTES 1, 4) CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
High Level Output Voltage	VOH	VCC = 4.5V, IO = -1.0mA	1, 2, 3	$-55^oC \le T_A \le +125^oC$	2.4	-	V
Low Level Output Voltage	VOL	VCC = 4.5V, IO = +3.2mA	1, 2, 3	$-55^oC \le T_A \le +125^oC$	-	0.4	V
High Impedance Output Leakage Current	IIOZ	VCC = 5.5V, $\overline{G}$ = 5.5V, VI/O = GND or VCC	1, 2, 3	$-55^oC \le T_A \le +125^oC$	-1.0	1.0	µA
Input Leakage Current	II	VCC = 5.5V, VI = GND or VCC, P Not Tested	1, 2, 3	$-55^oC \le T_A \le +125^oC$	-1.0	1.0	µA
Standby Supply Current	ICCSB	VI = VCC or GND, VCC = 5.5V, IO = 0mA	1, 2, 3	$-55^oC \le T_A \le +125^oC$	-	100	µA
Operating Supply Current	ICCOP	VCC = 5.5V, $\overline{G}$ = GND, G = VCC, (Note 3), f = 1MHz,IO = 0mA, VI = VCC or GND	1, 2, 3	$-55^oC \le T_A \le +125^oC$	-	20	mA
Functional Test	FT	VCC = 4.5V (Note 5)	7, 8A, 8B	$-55^oC \le T_A \le +125^oC$	-	-	-

TABLE 2. HM-6642/883 AC ELECTRICAL PERFORMANCE SPECIFICATIONS

Device Guaranteed and 100% Tested

PARAMETER	SYMBOL	(NOTES 1, 2, 4) CONDITIONS	GROUP A SUB-GROUPS	TEMPERATURE	LIMITS HM-6642B/883 MIN	LIMITS HM-6642B/883 MAX	LIMITS HM-6642/883 MIN	LIMITS HM-6642/883 MAX	UNITS
Address Access Time	TAVQV	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	-	140	-	220	ns
Output Enable Access Time	TGVQV	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	-	50	-	150	ns
Chip Enable Access Time	TELQV	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	-	120	-	200	ns
Address Setup Time	TAVEL	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	20	-	20	-	ns
Address Hold Time	TELAX	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	25	-	60	-	ns
Chip Enable Low Width	TELEH	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	120	-	200	-	ns
Chip Enable High Width	TEHEL	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	40	-	150	-	ns

TABLE 2. HM-6642/883 AC ELECTRICAL PERFORMANCE SPECIFICATIONS (Continued)

Device Guaranteed and 100% Tested

PARAMETER	SYMBOL	(NOTES 1, 2, 4) CONDITIONS	GROUP A SUB-GROUPS	TEMPERATURE	LIMITS				UNITS
					HM-6642B/883		HM-6642/883		
					MIN	MAX	MIN	MAX	
Read Cycle Time	TELEL	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	160	-	350	-	ns

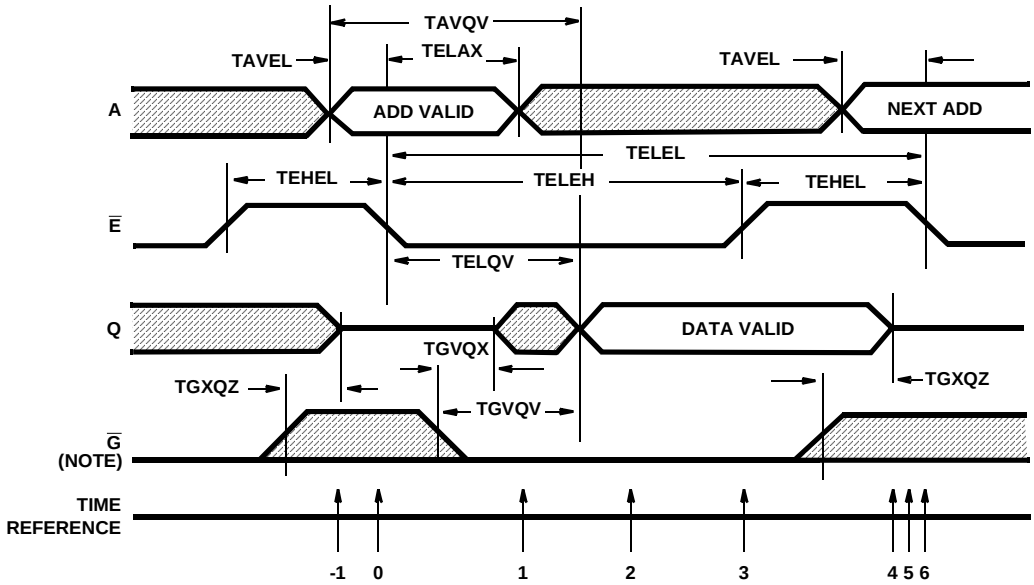
NOTES:

1. All voltages referenced to VSS.
2. A.C. measurements assume transition time < 5ns; input levels = 0.0V to 3.0V; timing reference levels = 1.5V; output load = 1TTL equivalent load and CL ≅ 50pF.
3. Typical derating = 5mA/MHz increase in ICCOP.
4. All tests performed with P hardwired to GND.
5. Tested as follows: f = 1MHz, VIH = 2.4V, VIL = 0.8V, IOH = -1mA, IOL = +1mA, VOH ≥ 1.5V, VOL ≤ 1.5V.

TABLE 3. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS	METHOD	SUBGROUPS
Initial Test	100%/5004	-
Interim Test	100%/5004	1, 7, 9
PDA	100%/5004	1
Final Test	100%/5004	2, 3, 7, 8A, 8B, 10, 11
Group A	Samples/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11
Groups C & D	Samples/5005	1, 7, 9

Switching Waveform



NOTE: G has the same timing as $\overline{G}$ except signal is inverted.

FIGURE 1. READ CYCLE

Test Load Circuit

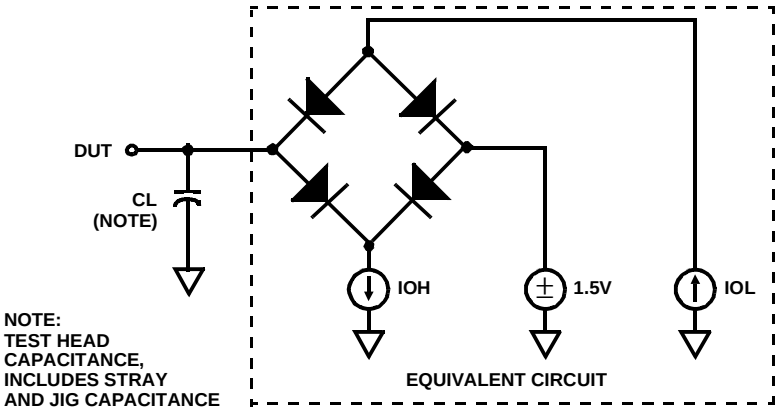
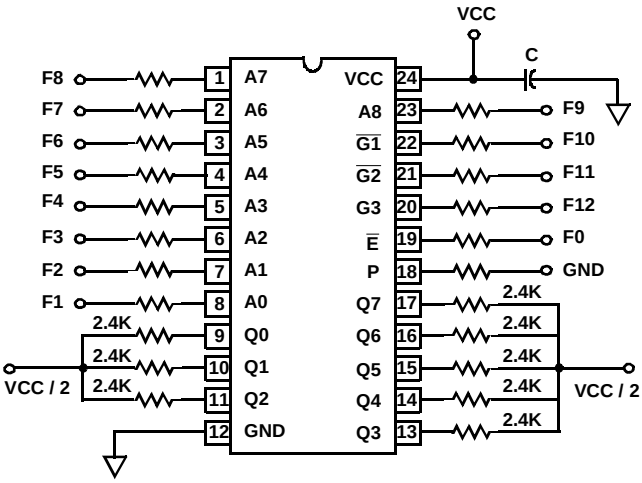


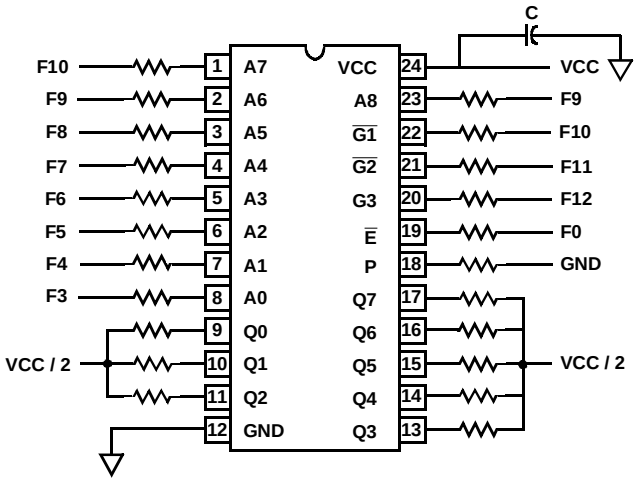
FIGURE 2. TEST LOAD CIRCUIT

Burn-In Circuits

HM-6642/883 (0.300 INCH) SBDIP

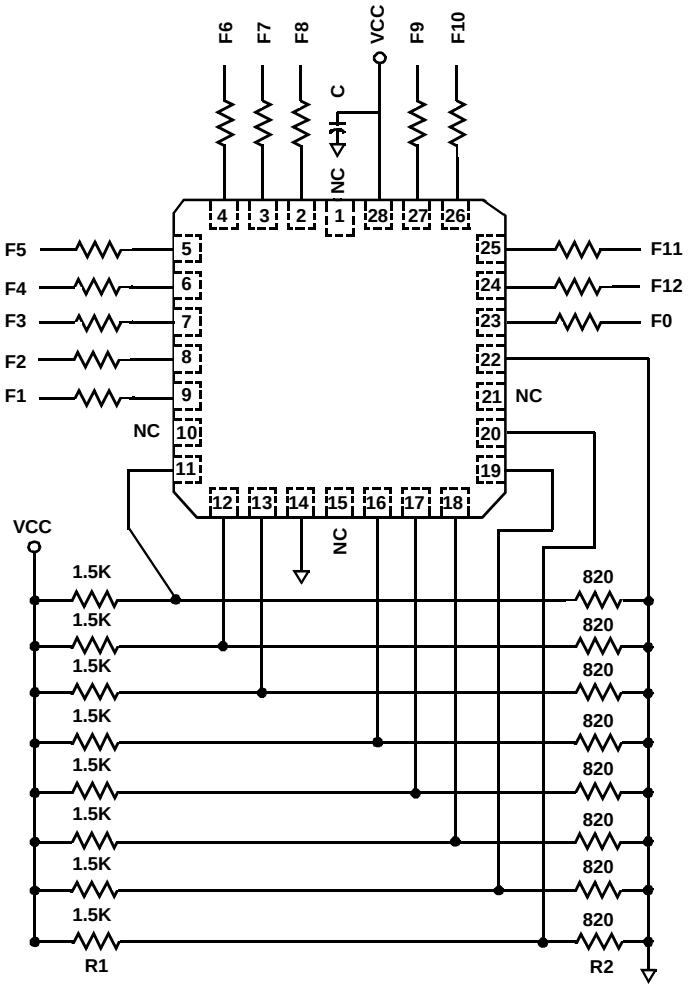


HM-6642/883 (0.600 INCH) SBDIP



Burn-In Circuits (Continued)

HM-6642/883 CLCC



NOTES:

1. F0 = 100kHz ± 10%.
2. All Resistors = 47kΩ.
3. Unless Otherwise Noted.
4. VCC = 5.5V ± 0.5V.
5. VIL = 4.5V ± 10%.
6. C = 0.01μF Min.

Die Characteristics

DIE DIMENSIONS:
136 x 168 x 19 ± 1mils

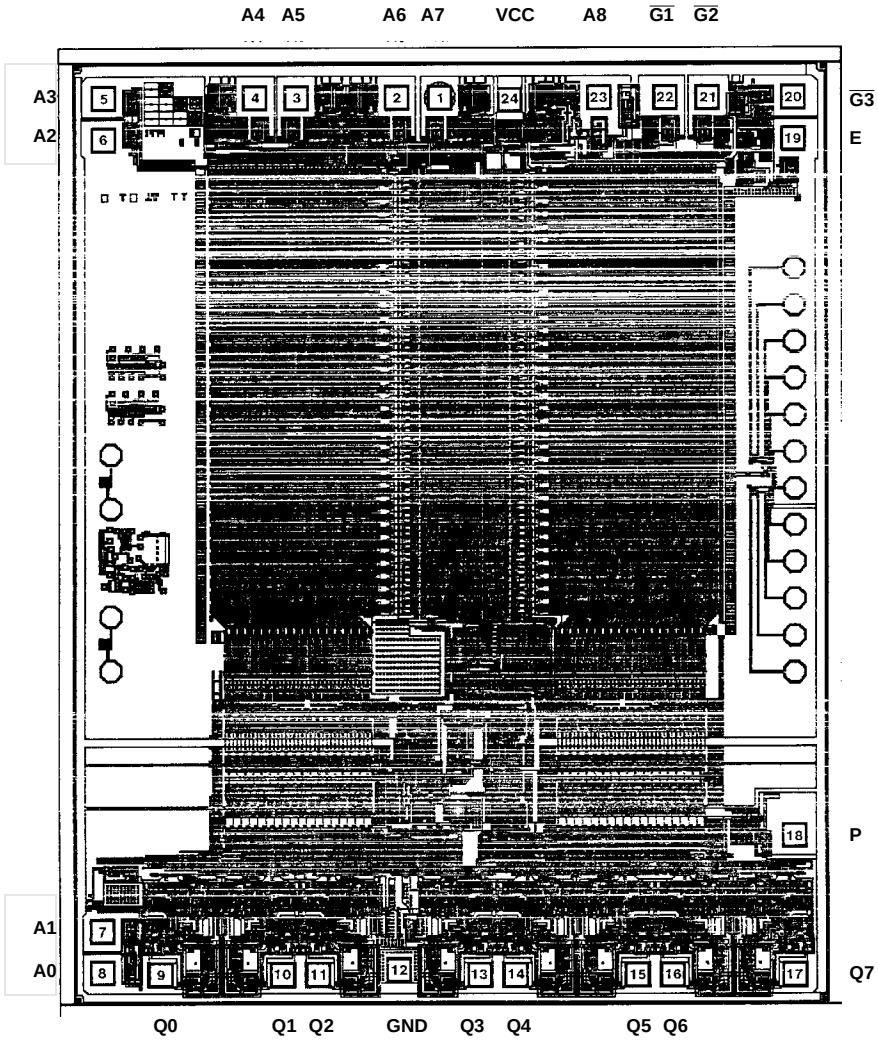
METALLIZATION:
Type: Si - Al
Thickness: 11kÅ ± 15kÅ

GLASSIVATION:
Type: SiO_2
Thickness: 8kÅ ± 1kÅ

WORST CASE CURRENT DENSITY:
1.7 x 10^5 A/cm^2

Metallization Mask Layout

HM-6642/883



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