788-144

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HN58V256A Series
HN58V257A Series

32768-word × 8-bit Electrically Erasable and Programmable CMOS ROM

HITACHI

ADE-203-357 A (Z)
Rev. 1.0
Apr. 12, 1996

Description

The Hitachi HN58V256A and HN58V257A are a electrically erasable and programmable EEPROM's organized as 32768-word × 8-bit. Employing advanced MNOS memory technology and CMOS process and circuitry technology. They also have a 64-byte page programming function to make their write operations faster.

Features

- Single 2.7 to 5.5 V supply
- On-chip latches: address, data, $\overline{CE}$, $\overline{OE}$, $\overline{WE}$
- Automatic byte write: 10 ms max
- Automatic page write (64 bytes): 10 ms max
- Fast access time: 120 ns max
- Low power dissipation: active: 20 mW/MHz, (typ)
  standby: 110 µW (max)
- Ready/$\overline{Busy}$ (only the HN58V267A series)
- $\overline{Data}$ polling and Toggle bit
- Data protection circuit on power on/off
- Conforms to JEDEC byte-wide standard
- Reliable CMOS with MNOS cell technology
- 10^5 erase/write cycles (in page mode)
- 10 years data retention
- Software data protection
- Write protection by $\overline{RES}$ pin (only the HN58V267A series)
- Industrial versions (Temperatur range: –20 to 85°C and –40 to 85°C) are also available.

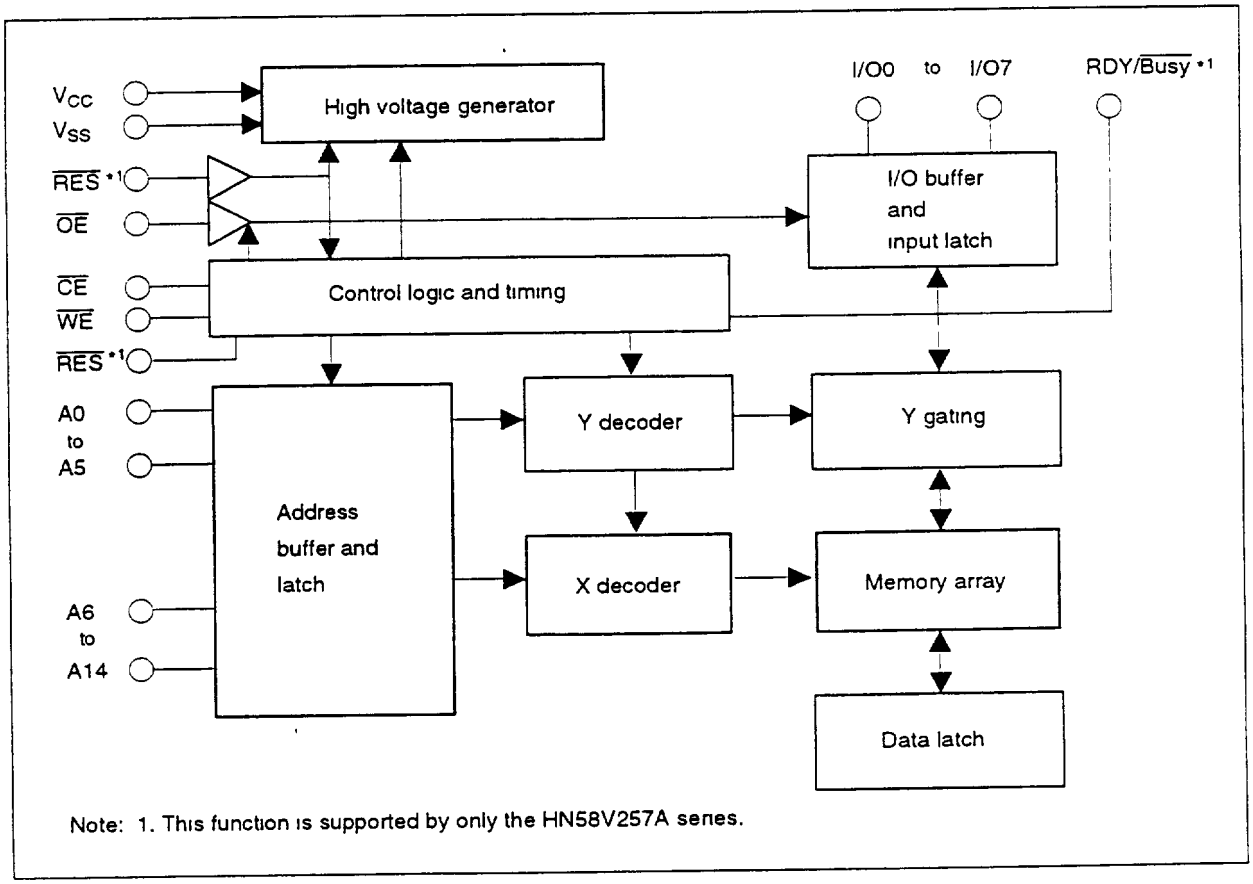
Hitachi semiconductor

Pin Description

Pin name	Function
A0 to A14	Address input
I/O0 to I/O7	Data input/output
$\overline{OE}$	Output enable
$\overline{CE}$	Chip enable
$\overline{WE}$	Write enable
V_{CC}	Power supply
V_{SS}	Ground
RDY/$\overline{Busy}$*1	Ready busy
$\overline{RES}$*1	Reset
NC	No connection

Note: 1. This function is supported by only the HN58V257A series.

Block Diagram



Note: 1. This function is supported by only the HN58V257A series.

Recommended DC Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	2.7	3.0	5.5	V
Input voltage	V_{IL}	−0.3[*1]	—	0.6	V
	V_{IH}	1.9[*2]	—	V_{CC} + 0.3[*3]	V
	V_H[*4]	V_{CC} − 0.5	—	V_{CC} + 1.0	V
Operating temperature	Topr	0	—	70	°C

Notes: 1. V_{IL} min: −1.0 V for pulse width ≤ 50 ns.
2. V_{IH} min for V_{CC} = 3.6 to 5.5 V is 2.4 V.
3. V_{IH} max: V_{CC} + 1.0 V for pulse width ≤ 50 ns.
4. This function is supported by only the HN58V257A series.

DC Characteristics (Ta = 0 to +70°C, V_{CC} = 2.7 to 5.5 V)

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Input leakage current	I_{LI}	—	—	2[*1]	µA	V_{CC} = 5.5 V, Vin = 5 5 V
Output leakage current	I_{LO}	—	—	2	µA	V_{CC} = 5.5 V, Vout = 5.5/0.4 V
V_{CC} current (standby)	I_{CC1}	—	—	20	µA	$\overline{CE}$ = V_{CC}
	I_{CC2}	—	—	1	mA	$\overline{CE}$ = V_{IH}
V_{CC} current (active)	I_{CC3}	—	—	8	mA	Iout = 0 mA, Duty = 100%, Cycle = 1 µs at V_{CC} = 3.6 V
		—	—	12	mA	Iout = 0 mA, Duty = 100%, Cycle = 1 µs at V_{CC} = 5 5 V
		—	—	12	mA	Iout = 0 mA, Duty = 100%, Cycle = 120 ns at V_{CC} = 3.6 V
		—	—	30	mA	Iout = 0 mA, Duty = 100%, Cycle = 120 ns at V_{CC} = 5.5 V
Output low voltage	V_{OL}	—	—	0.4	V	I_{OL} = 2.1 mA
Output high voltage	V_{OH}	V_{CC} × 0.8	—	—	V	I_{OH} = −400 µA

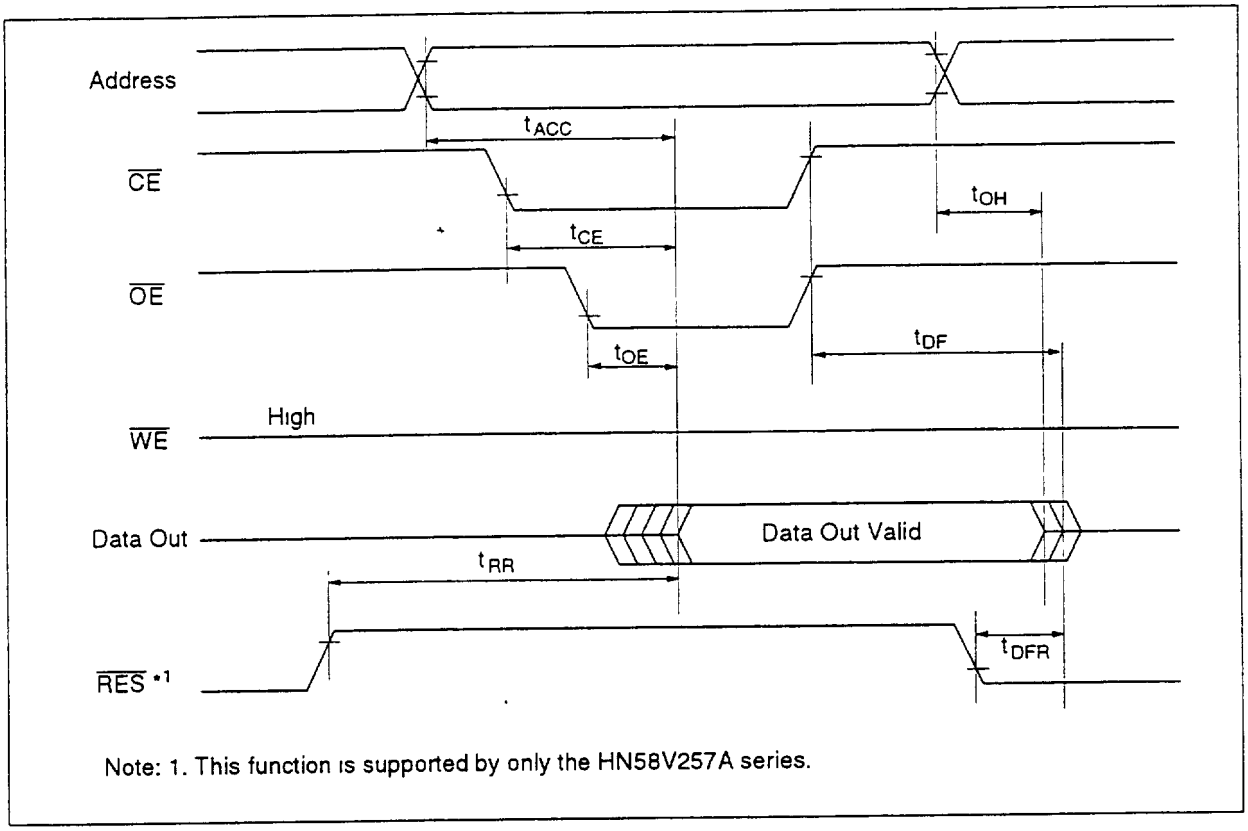
Note: 1. I_{LI} on $\overline{RES}$ = 100 µA max (only the HN58V257A series)

Capacitance (Ta = 25°C, f = 1 MHz)

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Input capacitance[*1]	Cin	—	—	6	pF	Vin = 0 V
Output capacitance[*1]	Cout	—	—	12	pF	Vout = 0 V

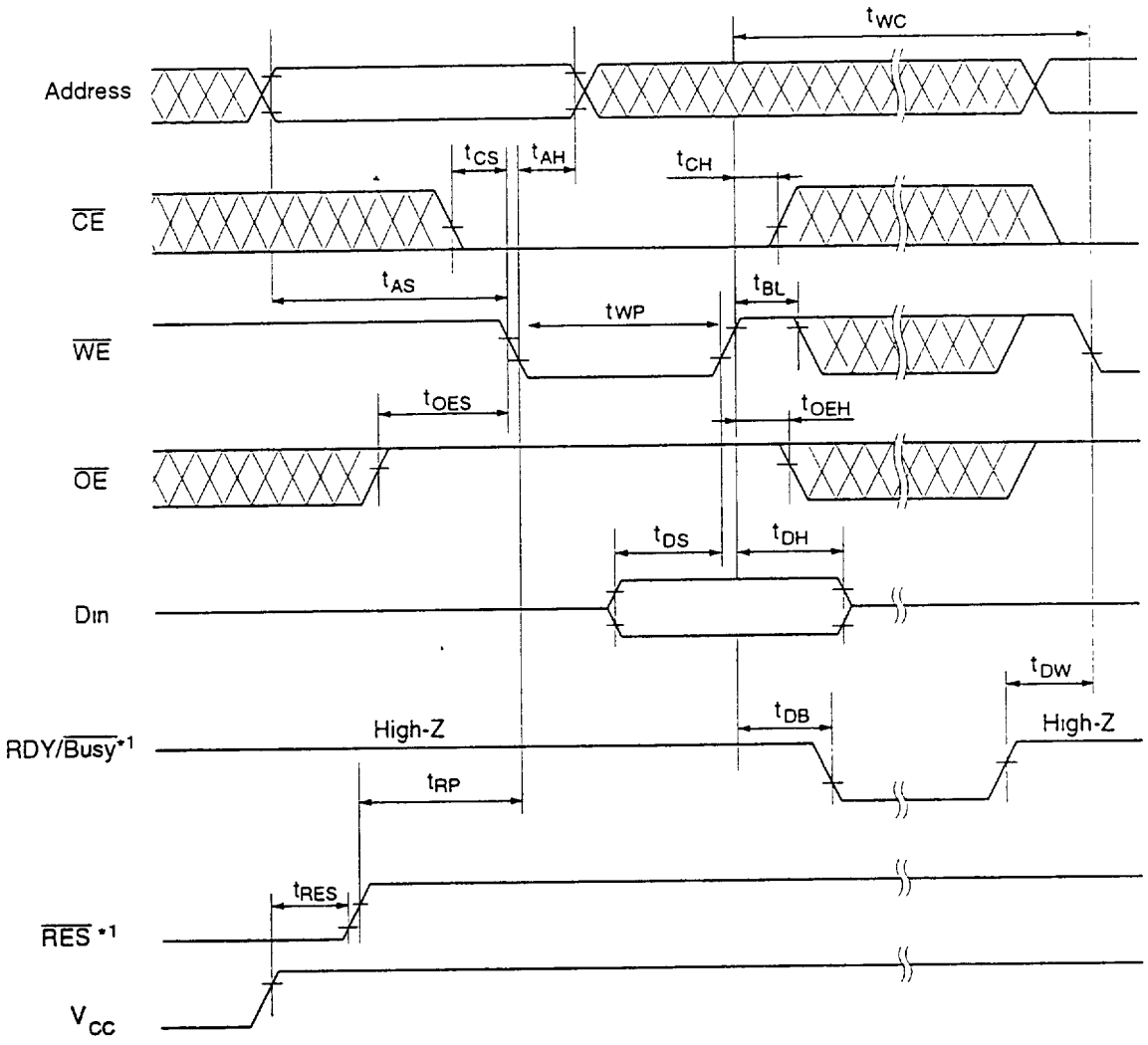
Note: 1. This parameter is periodically sampled and not 100% tested.

Read Timing Waveform



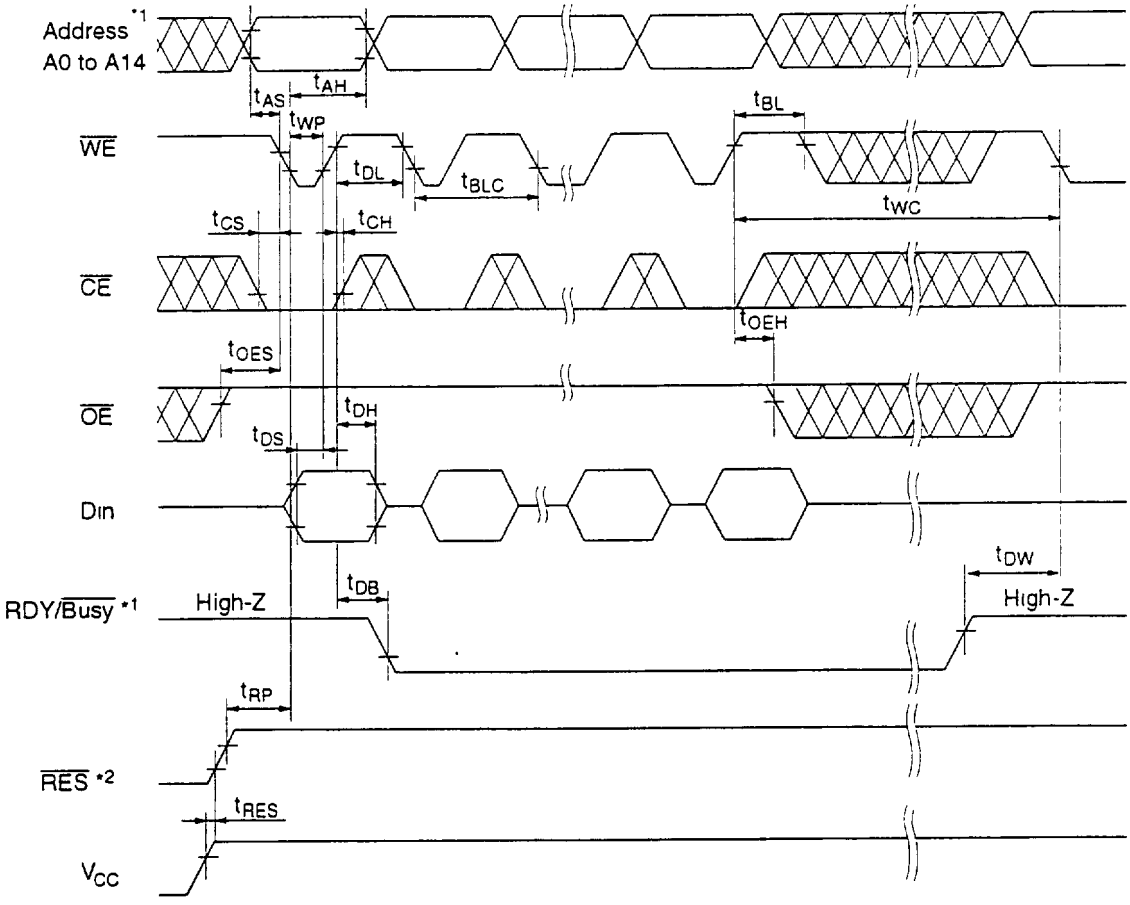
Note: 1. This function is supported by only the HN58V257A series.

Byte Write Timing Waveform (1) ($\overline{WE}$ Controlled)



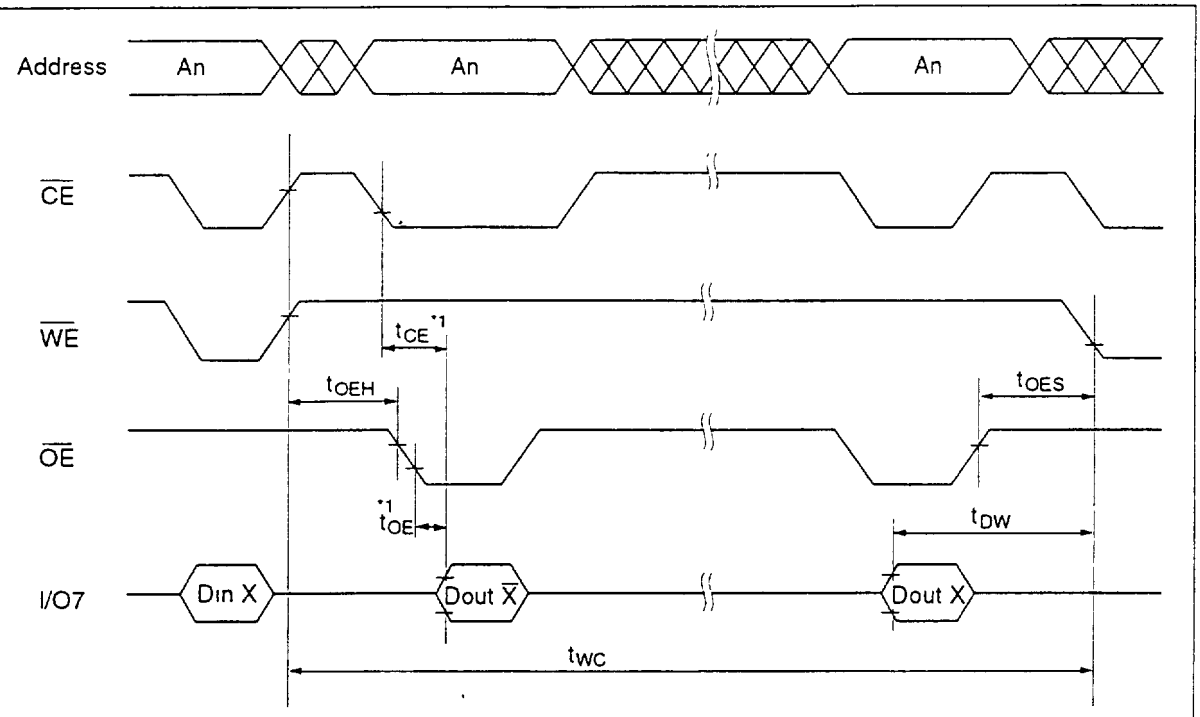
Note: 1. This function is supported by only the HN58V257A series.

Page Write Timing Waveform (1) ($\overline{WE}$ Controlled)



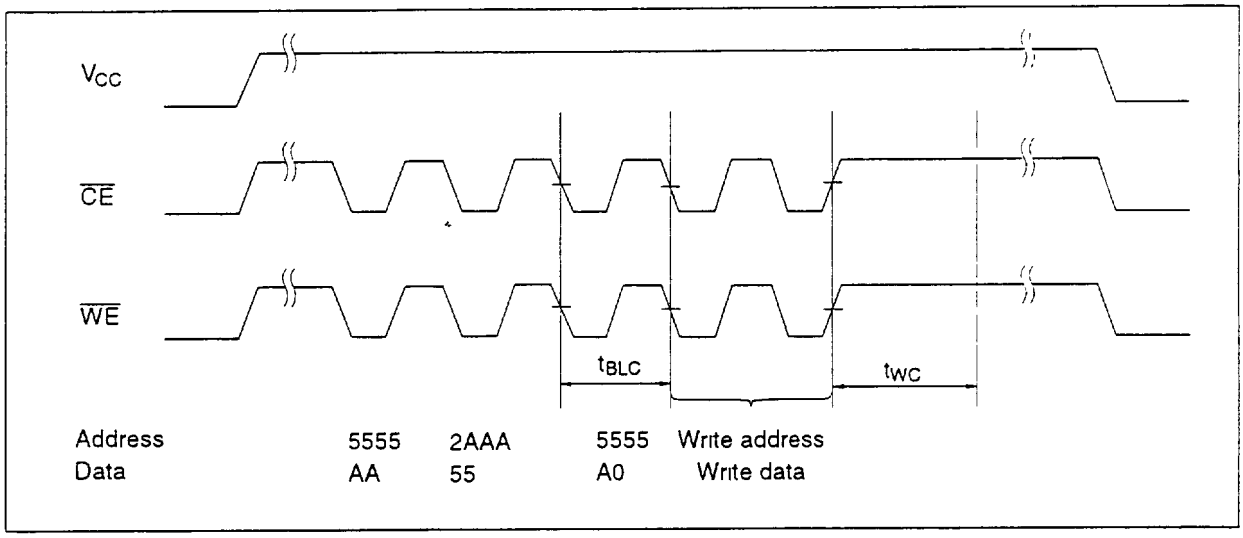
Notes: 1. A6 through A14 are page address and these address are latched at the first falling edge of $\overline{WE}$
2. This function is supported by only the HN58V257A series.

$\overline{\text{Data}}$ Polling Timing Waveform

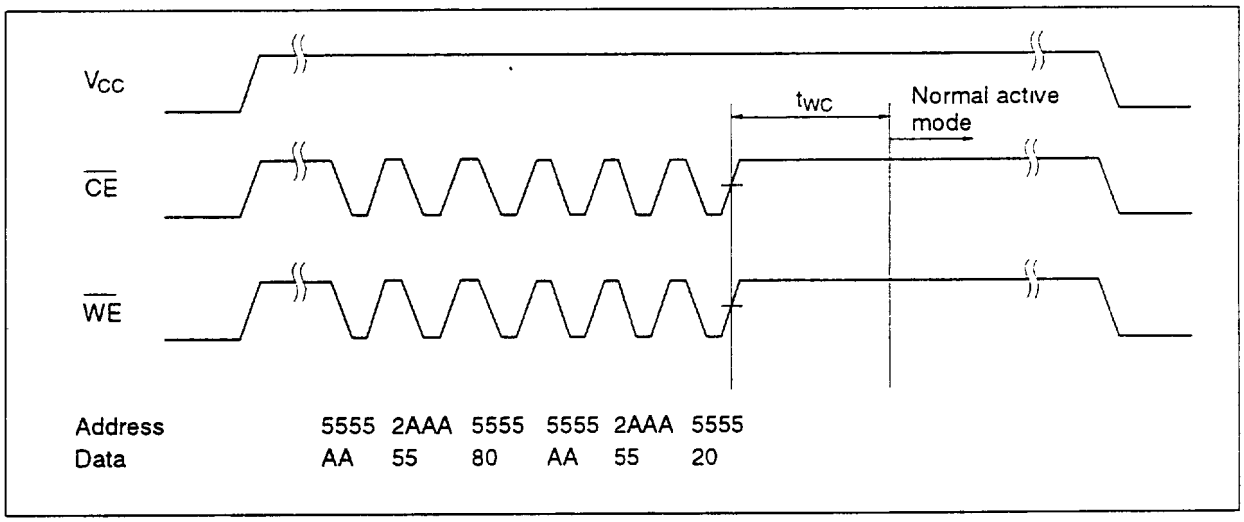


Note: 1. See AC read characteristics.

Software Data Protection Timing Waveform (1) (in protection mode)



Software Data Protection Timing Waveform (2) (in non-protection mode)



$\overline{WE}$, $\overline{CE}$ Pin Operation

During a write cycle, addresses are latched by the falling edge of $\overline{WE}$ or $\overline{CE}$, and data is latched by the rising edge of $\overline{WE}$ or $\overline{CE}$.

Write/Erase Endurance and Data Retention Time

The endurance is 10^5 cycles in case of the page programming and 10^4 cycles in case of the byte programming (1% cumulative failure rate). The data retention time is more than 10 years when a device is page-programmed less than 10^4 cycles.

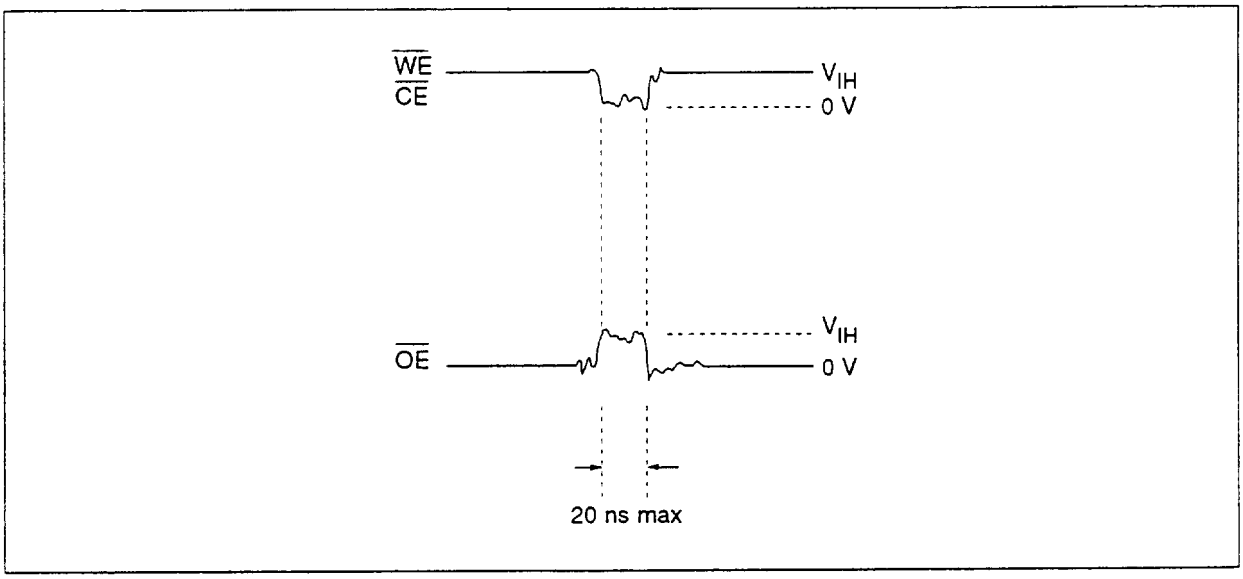
Data Protection

1. Data Protection against Noise on Control Pins ($\overline{CE}$, $\overline{OE}$, $\overline{WE}$) during Operation

During readout or standby, noise on the control pins may act as a trigger and turn the EEPROM to programming mode by mistake.

To prevent this phenomenon, this device has a noise cancelation function that cuts noise if its width is 20 ns or less in program mode.

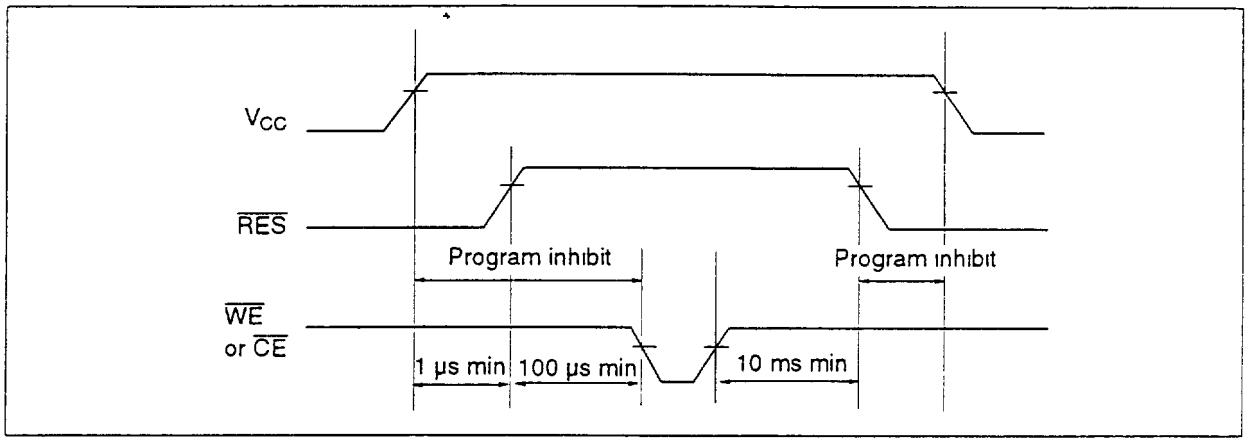
Be careful not to allow noise of a width of more than 20 ns on the control pins.



(2) Protection by $\overline{RES}$ (only the HN58V257A series)

The unprogrammable state can be realized by that the CPU's reset signal inputs directly to the EEPROM's $\overline{RES}$ pin. $\overline{RES}$ should be kept V_{SS} level during V_{CC} on/off.

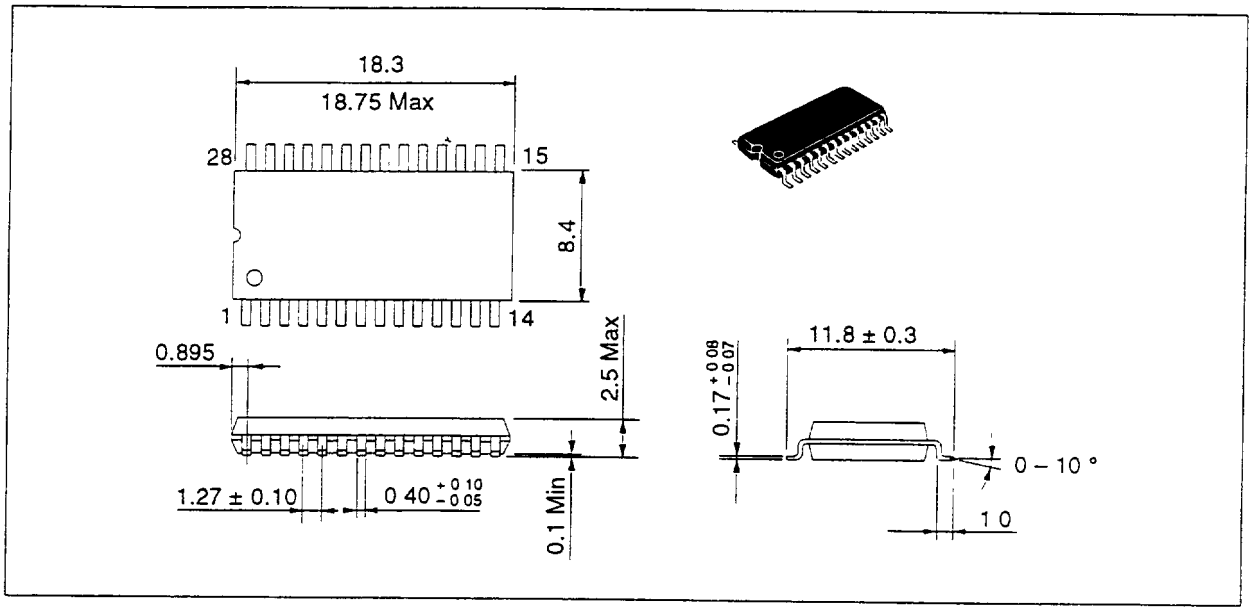
The EEPROM breaks off programming operation when $\overline{RES}$ becomes low, programming operation doesn't finish correctly in case that $\overline{RES}$ falls low during programming operation. $\overline{RES}$ should be kept high for 10 ms after the last data input.



Package Dimensions

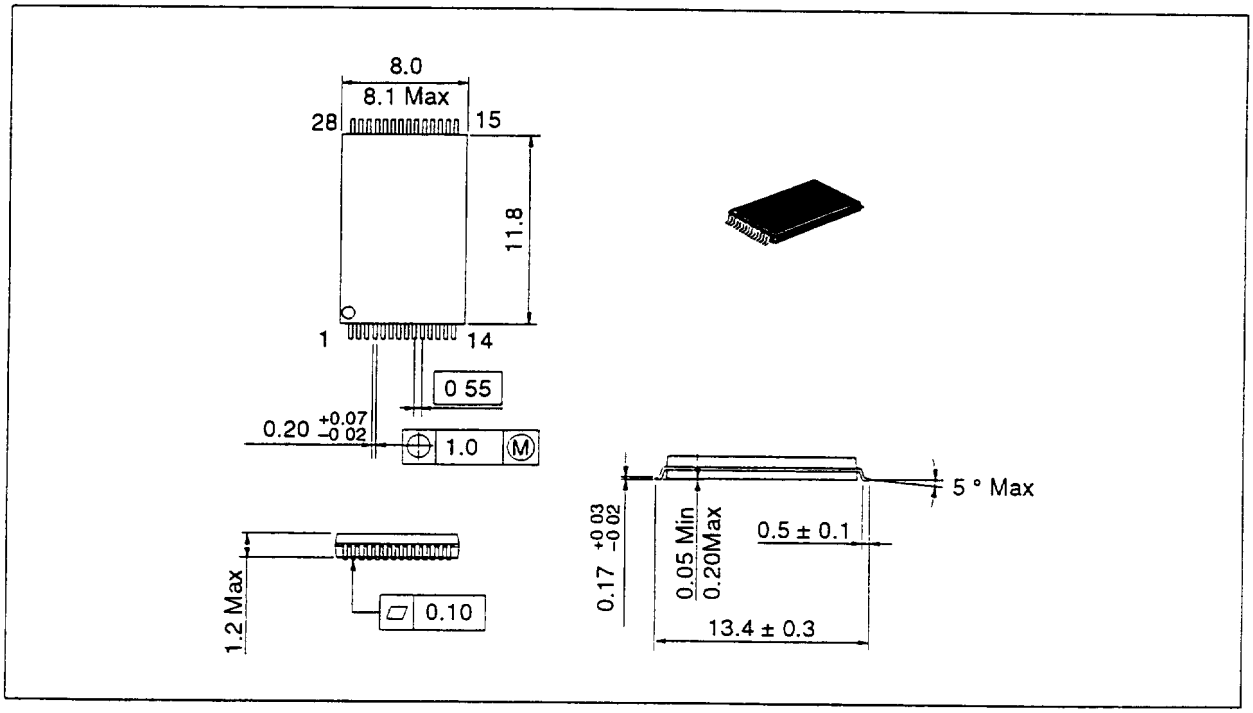
HN58V256AFP Series (FP-28D)

Unit mm



HN58V256AT Series (TFP-28DB)

Unit mm



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