

Test Circuits

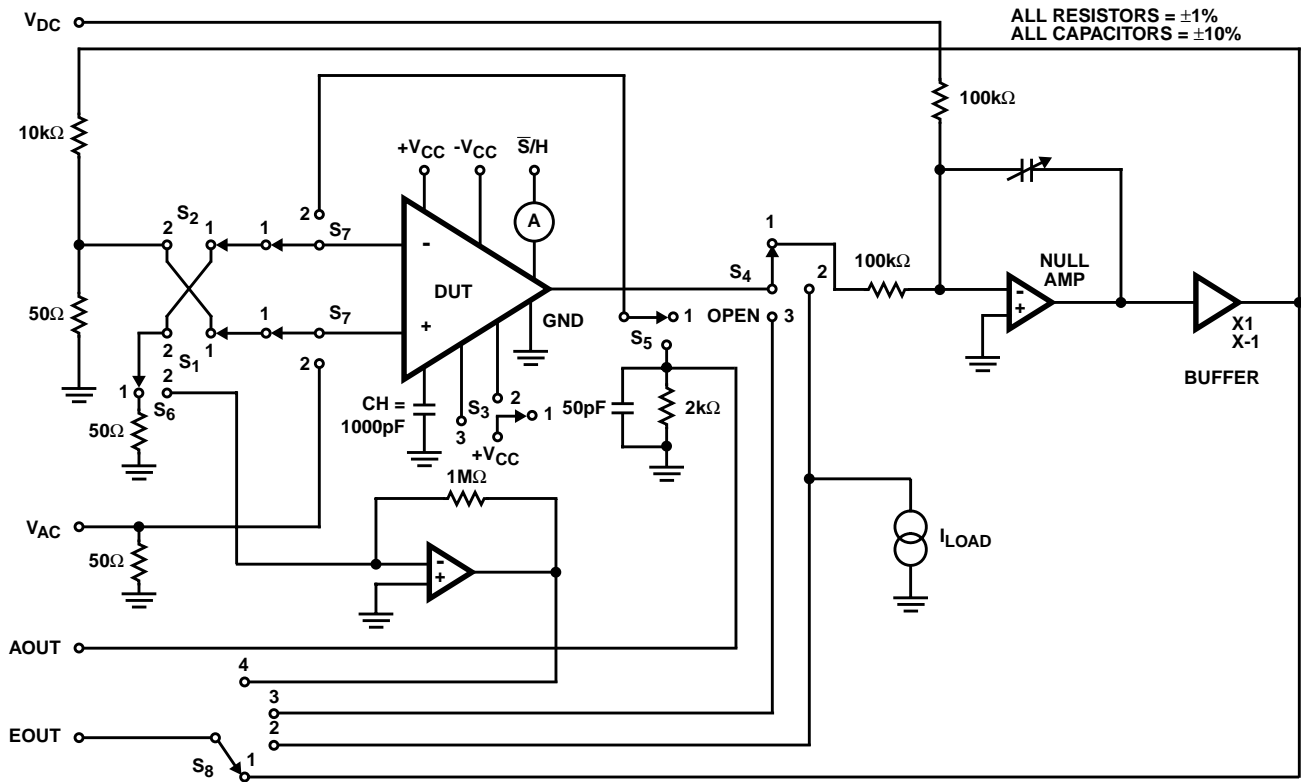
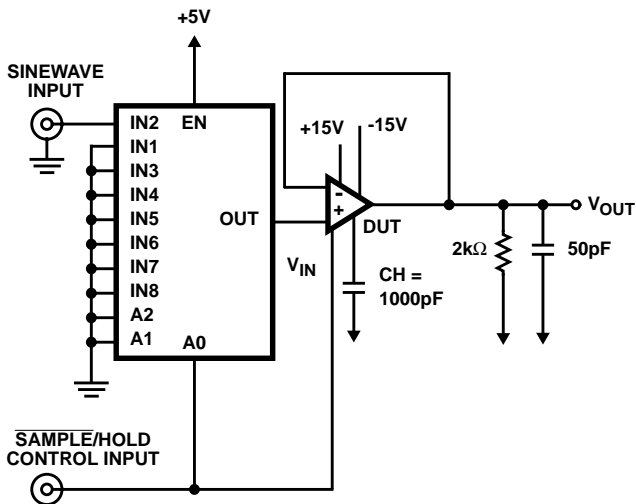


FIGURE 1. TEST FIXTURE SCHEMATIC (SWITCH POSITIONS S₁ - S₈ DETERMINE CONFIGURATION)

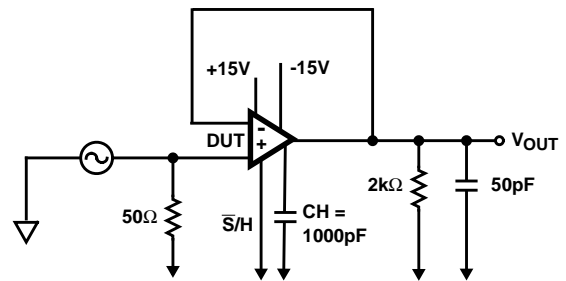


NOTE: Compute Hold Mode Feedthrough Attenuation from the Formula:

$$\text{FeedthroughAttenuation} = 20 \log \left(\frac{V_{\text{OUT HOLD}}}{V_{\text{IN HOLD}}} \right)$$

Where V_{OUT HOLD} = Peak-Peak Value of Output Sinewave during the Hold Mode.

FIGURE 2. HOLD MODE FEEDTHROUGH ATTENUATION

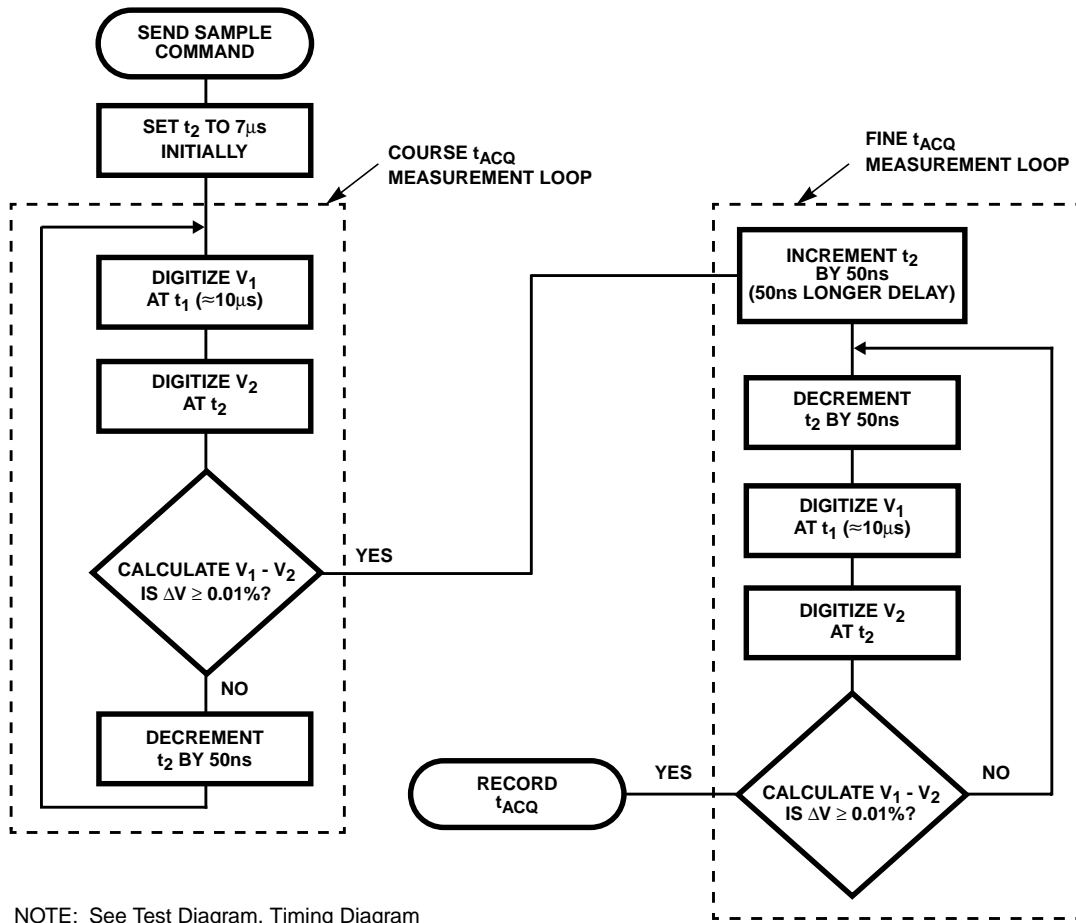


NOTE: GBWP is the Frequency of V_{INPUT} at which:

$$20 \log \left(\frac{V_{\text{OUT}}}{V_{\text{INPUT}}} \right) = -3\text{dB}$$

FIGURE 3. GAIN BANDWIDTH PRODUCT

Test Circuits (Continued)



NOTE: See Test Diagram, Timing Diagram

FIGURE 4. ACQUISITION TIME (t_{ACQ} TO 0.01% IS SHOWN, t_{ACQ} TO 0.1% IS DONE IN THE SAME MANNER)

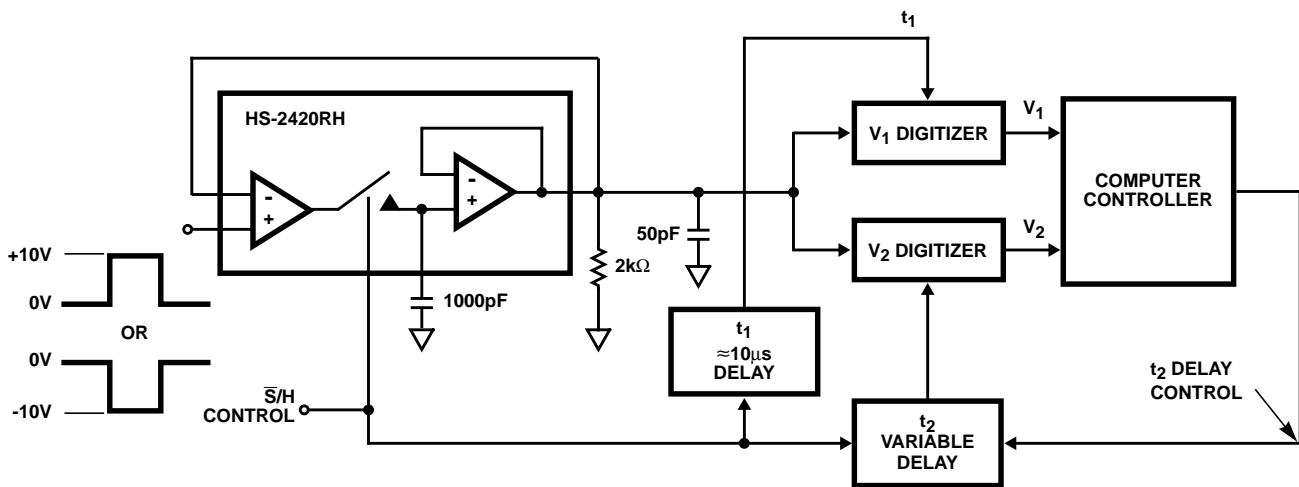


FIGURE 5.

Timing Waveforms

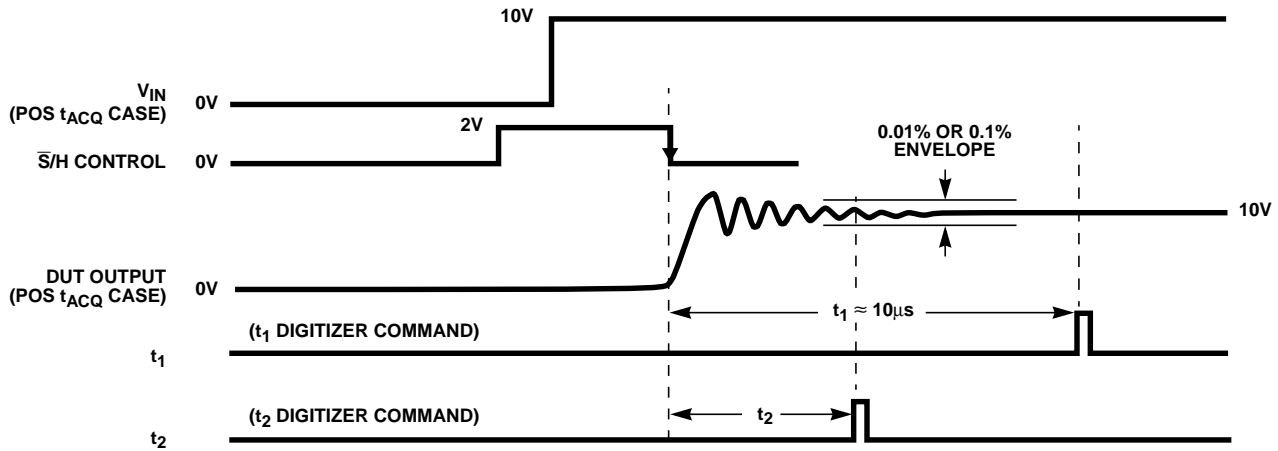


FIGURE 6. TIMING DIAGRAM FOR ACQUISITION TIME, (POSITIVE t_{ACQ} CASE)

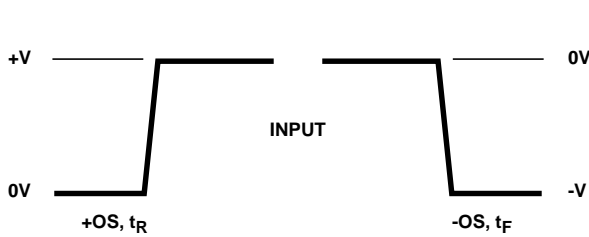


FIGURE 7A.

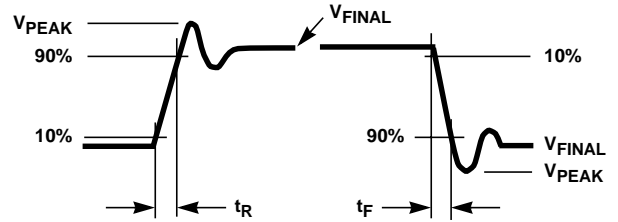


FIGURE 7B.

FIGURE 7. OVERSHOOT, RISE AND FALL TIME WAVEFORMS

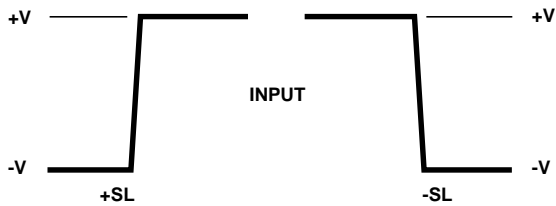


FIGURE 8A.

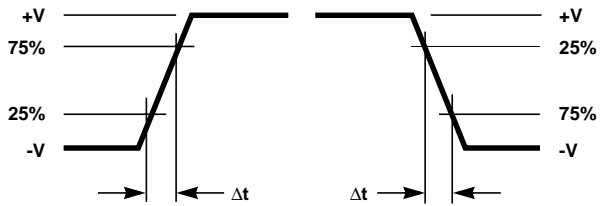


FIGURE 8B.

FIGURE 8. SLEW RATE WAVEFORMS

Typical Performance Curves $V_{SUPPLY} = \pm 15V_{DC}$, $T_A = 25^{\circ}C$, $CH = 1000pF$, Unless Otherwise Specified

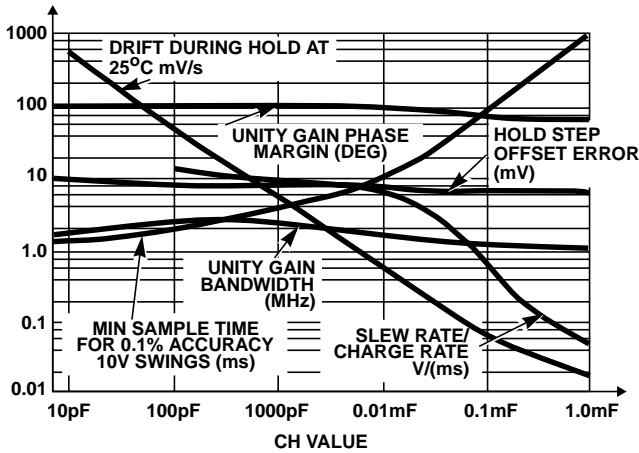


FIGURE 9. TYPICAL SAMPLE AND HOLD PERFORMANCE vs HOLDING CAPACITOR

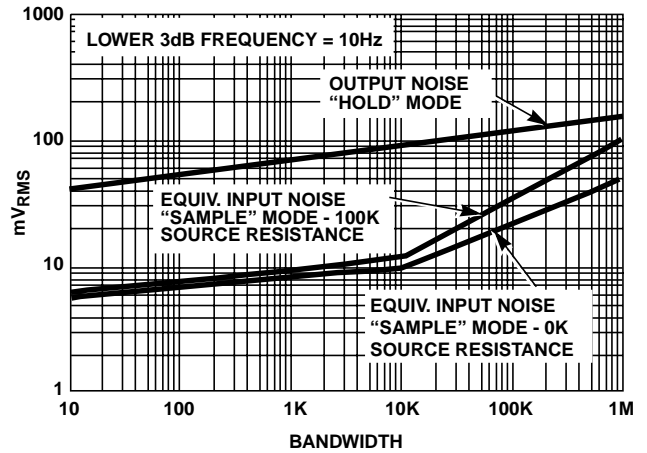


FIGURE 10. BROADBAND NOISE CHARACTERISTICS

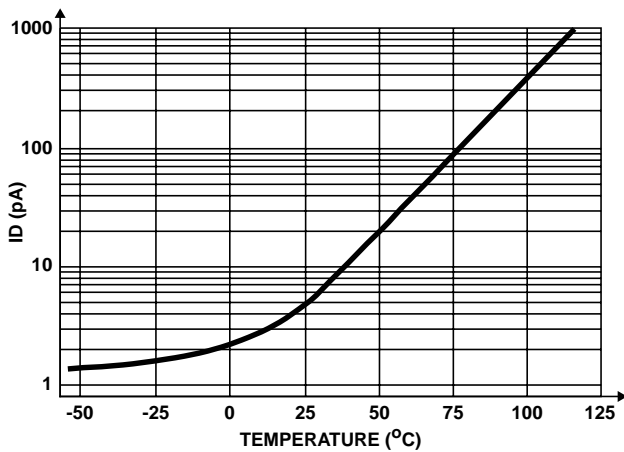


FIGURE 11. DRIFT CURRENT vs TEMPERATURE

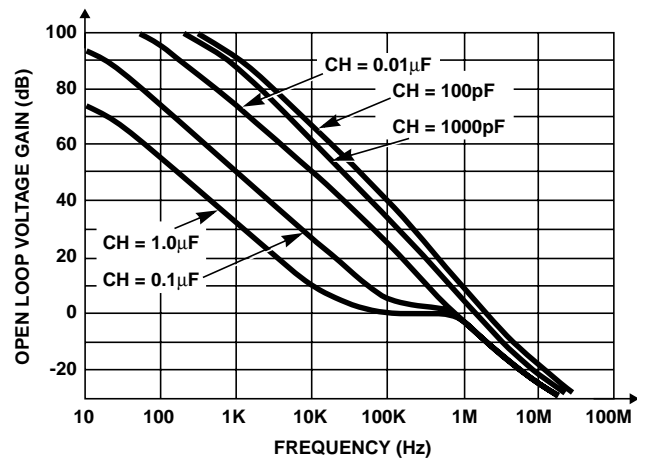


FIGURE 12. OPEN LOOP FREQUENCY RESPONSE

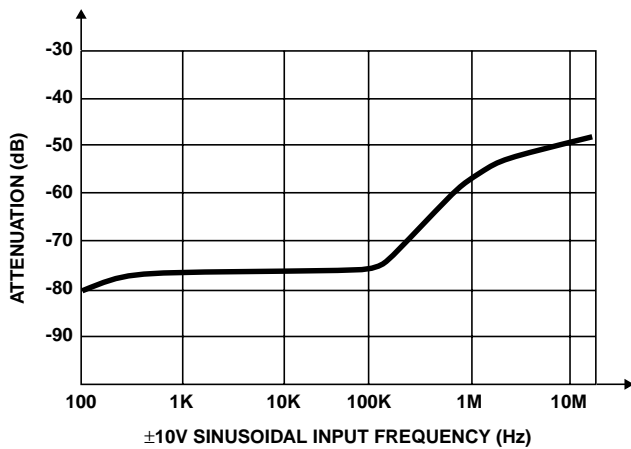


FIGURE 13. HOLD MODE FEEDTHROUGH ATTENUATION
CH = 1000pF

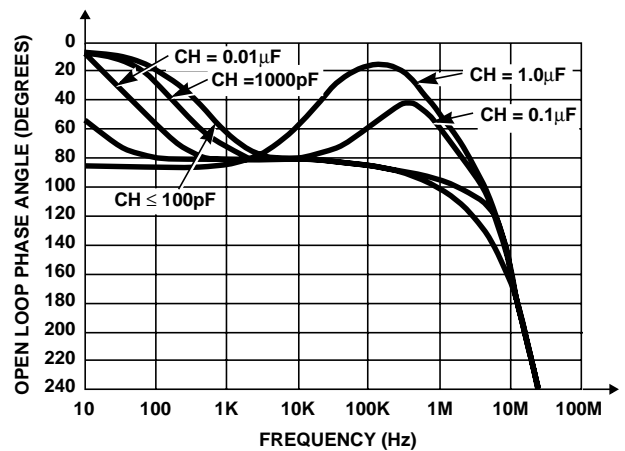
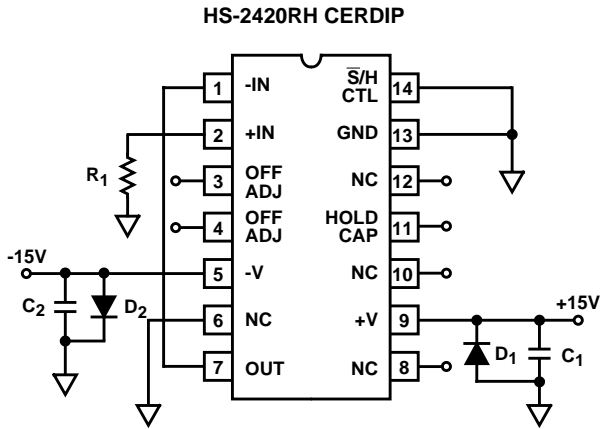


FIGURE 14. OPEN LOOP PHASE RESPONSE

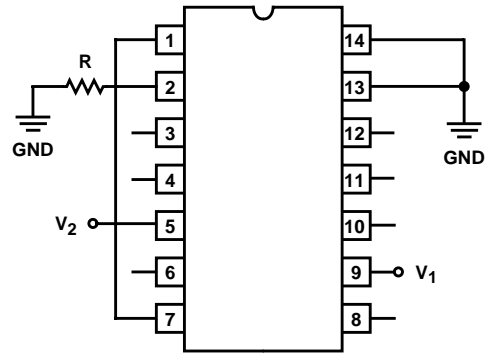
Burn-In Circuit



NOTES:

- R₁ = 100kΩ ±5% (per socket)
- C₁ = C₂ = 0.1μF (one per row) or 0.01μF (one per socket)
- D₁ = D₂ = 1N4002 or equivalent (per board)

Irradiation Circuit



NOTES:

- V₁ = +15V
- V₂ = -15V
- R = 100kΩ

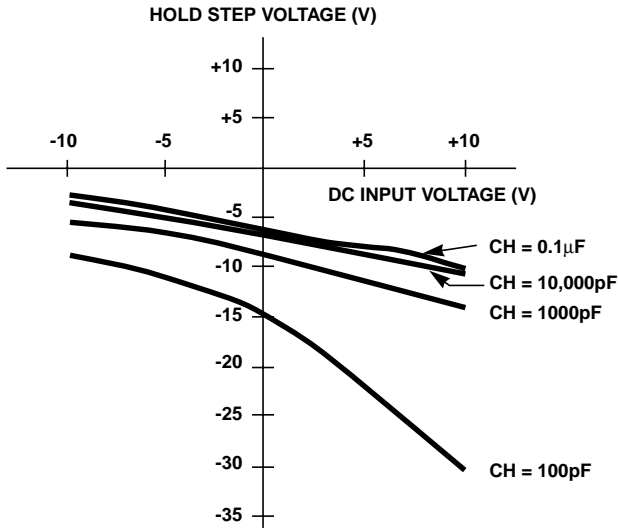


FIGURE 15. HOLD STEP vs INPUT VOLTAGE

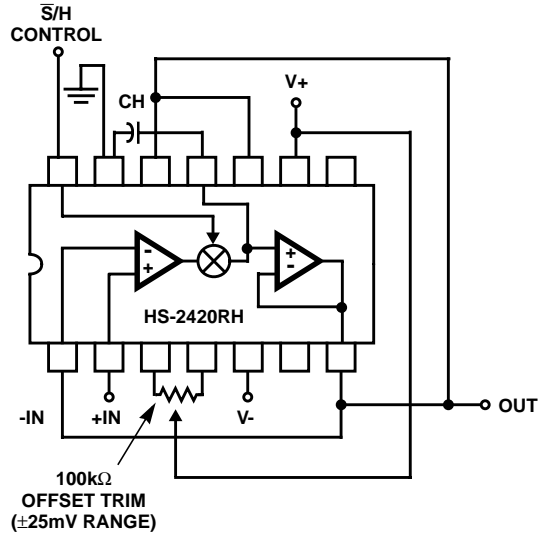


FIGURE 16. BASIC SAMPLE-AND-HOLD (TOP VIEW)

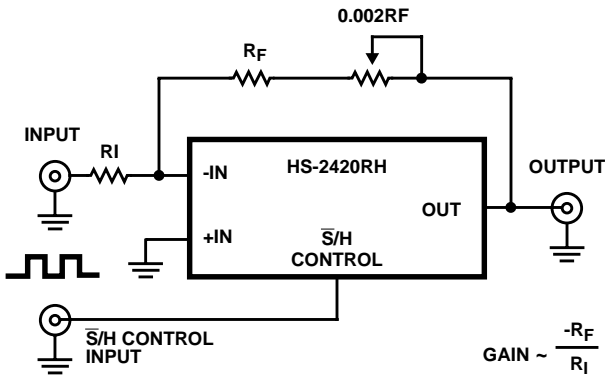


FIGURE 17. INVERTING CONFIGURATION

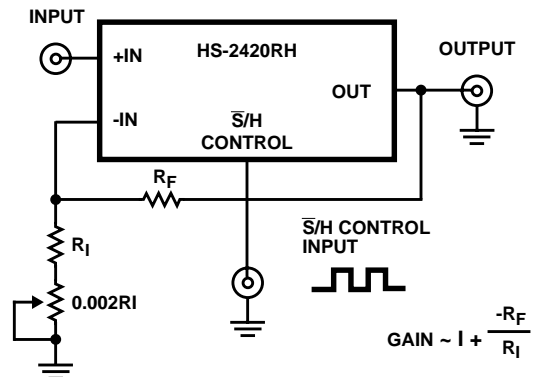


FIGURE 18. NONINVERTING CONFIGURATION

Offset and Gain Adjustment

Offset Adjustment

The offset voltage of the HS-2420RH may be adjusted using a 100k Ω trim pot, as shown in Figure 15. The recommended adjustment procedure is:

1. Apply 0V to the sample-and-hold input, and a square wave to the \overline{S}/H control.
2. Adjust the trim pot for 0V output in the hold mode.

Gain Adjustment

The linear variation in pedestal voltage with sample-and-hold input voltage causes a -0.06% gain error (CH = 1000pF). In some applications (D/A deglitcher, A/D converter) the gain error can be adjusted elsewhere in the system, while in other applications it must be adjusted at the sample-and-hold. The two circuits shown below demonstrate how to adjust gain error at the sample-and-hold.

The recommended procedure for adjusting gain error is:

1. Perform offset adjustment.
2. Apply the nominal input voltage that should produce a +10V output.
3. Adjust the trim pot for +10V output in the hold mode.
4. Apply the nominal input voltage that should produce a -10V output.
5. Measure the output hold voltage (V-10 NOMINAL). Adjust the trim pot for an output hold voltage of:

$$\frac{(V-10 \text{ NOMINAL}) + (-10V)}{2}$$

HS-2420RH

Die Characteristics

DIE DIMENSIONS:

97 mils x 61 mils x 19 mils

METALLIZATION:

Type: Al

Thickness: $16\text{k}\text{\AA} \pm 2\text{k}\text{\AA}$

GLASSIVATION:

Type: Silox

Thickness: $14\text{k}\text{\AA} \pm 2\text{k}\text{\AA}$

WORST CASE CURRENT DENSITY:

$2.0 \times 10^5 \text{A/cm}^2$

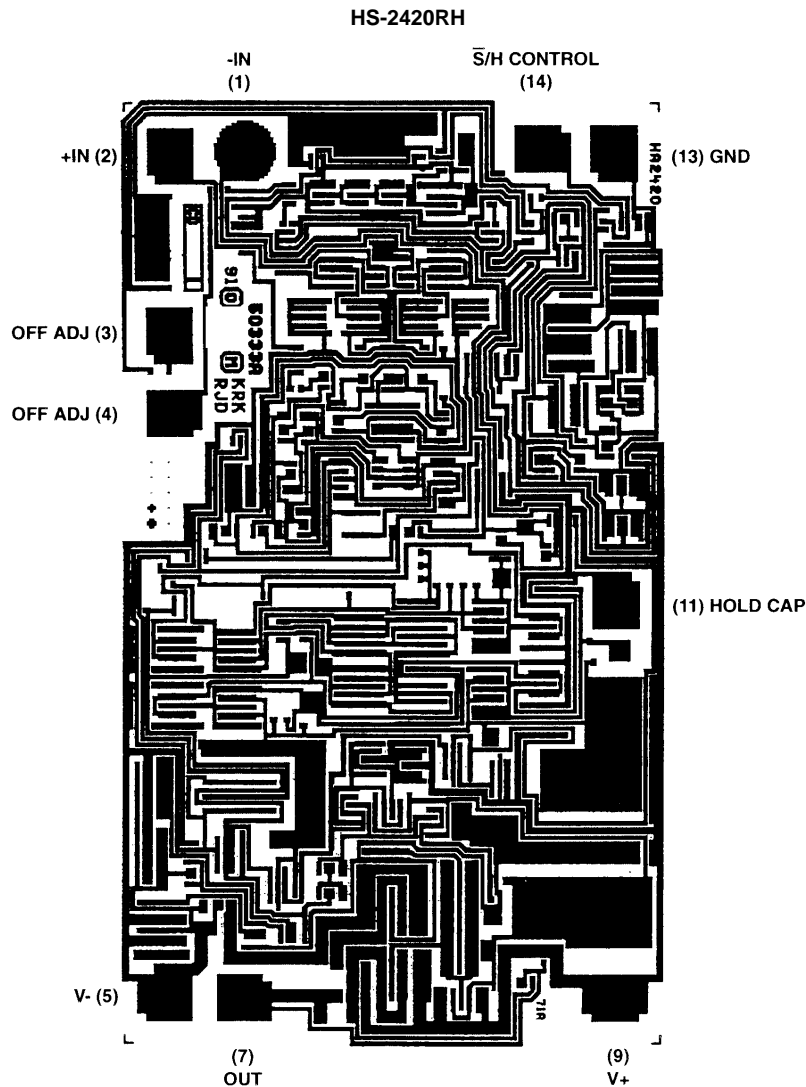
TRANSISTOR COUNT:

78

PROCESS:

Bipolar-Di

Metallization Mask Layout



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