

## High Voltage Liquid Crystal Shutter Driver

### Ordering Information

Device	HV <sub>IN</sub> Maximum Voltage	Package Options
		SO-8
HV508	45V	HV508LG

### Features

- ❑ HVCMOS® technology for high performance
- ❑ Logic-selectable output voltage
- ❑ 100nF drive capability
- ❑ Up to 90V<sub>P-P</sub>
- ❑ 25µs response time

### General Description

The Supertex HV508 is a 45V liquid crystal shutter driver in an SO-8 surface mount package. It consists of two outputs that provide square waves of opposite phase. The liquid crystal shutter is connected between the two outputs. Its equivalent load can be approximated as a resistor in parallel with a capacitor. Minimum resistance is 1.0MΩ and maximum capacitance is 0.1µF.

The HV508 has three input supply voltages, HV<sub>IN</sub>, LV<sub>IN</sub>, and V<sub>DD</sub>. The output's amplitude will be either LV<sub>IN</sub> or HV<sub>IN</sub>. A logic high on the HV<sub>EN</sub> input will set the output to operate from the HV<sub>IN</sub> supply. A logic low on the HV<sub>EN</sub> input will set the output to operate from the LV<sub>IN</sub> supply. The output frequency is set by the logic input frequency applied on the POL input.

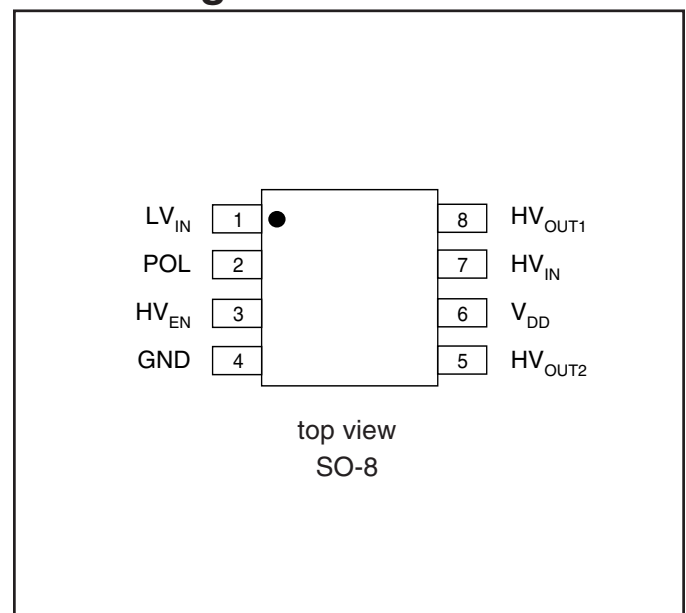
### Absolute Maximum\* Ratings

HV <sub>IN</sub> , high voltage input	+60V
LV <sub>IN</sub> , low voltage input	+7.5V
V <sub>DD</sub> , logic supply voltage	+12V
Continuous total power dissipation	700mW
Operating temperature	-5°C to +60°C
Storage temperature	-65°C to +150°C
Soldering temperature	+300°C

\* All voltages are referenced to GND.

For operation above 25°C ambient derate linearly at 6mW/°C.

### Pin Configuration



## Electrical Characteristics

**DC Electrical Characteristics** (over operating supply voltages unless otherwise specified,  $T_A = -5^{\circ}\text{C}$  to  $+60^{\circ}\text{C}$ )

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
$I_{HVQ}$	HV <sub>IN</sub> quiescent current			10	μA	
$I_{LVQ}$	LV <sub>IN</sub> quiescent current			10	μA	
$I_{DDQ}$	V <sub>DD</sub> quiescent current			10	μA	
$I_{HV}$	HV <sub>IN</sub> operating current			2.8	mA	POL = 100Hz, HV <sub>EN</sub> = high, T <sub>A</sub> = 25°C, Load = 1MΩ in parallel with 0.1μF between HV <sub>OUT1</sub> and HV <sub>OUT2</sub>
$I_{LV}$	LV <sub>IN</sub> operating current			380	μA	POL = 100Hz, HV <sub>EN</sub> = low, T <sub>A</sub> = 25°C, Load = 1MΩ in parallel with 0.1μF between HV <sub>OUT1</sub> and HV <sub>OUT2</sub>
$I_{IL}$	Logic input current low	-5			μA	
$I_{IH}$	Logic input current high			5.0	μA	
$C_{LOAD}$	Output capacitive load*	0		0.25	μF	C <sub>LOAD</sub> in parallel with a 1MΩ resistor

\*The device can operate continuously without any damage within this range. AC limits are not implemented.

**AC Electrical Characteristics** (HV<sub>IN</sub> = 45V, LV<sub>IN</sub> = 6V, V<sub>DD</sub> = 5V, T<sub>A</sub> = -5°C to +60°C)

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
$f_{POL}$	POL input frequency	0		100	Hz	
$t_{HV(ON)}$	Turn-on time when high voltage is enable			16	μs	Load = 1MΩ in parallel with 0.1μF between HV <sub>OUT1</sub> and HV <sub>OUT2</sub> . HV <sub>EN</sub> = High. Outputs rise to HV <sub>IN</sub> . See Fig. 1.
$t_{HV(OFF)}$	Turn-off time when high voltage is enabled			16	μs	
$t_{LV(ON)}$	Turn-on time when high voltage is disabled			40	μs	Load = 1MΩ in parallel with 0.1μF between HV <sub>OUT1</sub> and HV <sub>OUT2</sub> . HV <sub>EN</sub> = Low. Outputs rise to LV <sub>IN</sub> . See Fig. 1.
$t_{LV(OFF)}$	Turn-off time when high voltage is disabled			6.0	μs	
$t_{EN(ON)}$	Turn-on time from HV <sub>EN</sub> to HV <sub>OUT</sub>			25	μs	Load = 1MΩ in parallel with 0.1μF between HV <sub>OUT1</sub> and HV <sub>OUT2</sub> . See Fig. 2.

## Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit
V <sub>DD</sub>	Logic supply voltage	5.0		10.0	V
LV <sub>IN</sub>	Low output supply voltage	3.0		6.0	V
HV <sub>IN</sub>	High output supply voltage	5.0		45	V
V <sub>IL</sub>	Logic input voltage low	0		0.3V <sub>DD</sub>	V
V <sub>IH</sub>	Logic input voltage high	0.7V <sub>DD</sub>		V <sub>DD</sub>	V
T <sub>A</sub>	Ambient Temperature	-5.0		+60	°C

### Notes:

Power-up sequence should be the following:

1. Connect GND, V<sub>DD</sub>, logic inputs, HV<sub>IN</sub>, and LV<sub>IN</sub>.

Power-down sequence should be the reverse of the above.

## Truth Table

HV <sub>EN</sub>	POL	HV <sub>OUT1</sub>	HV <sub>OUT2</sub>
H	H	HV <sub>IN</sub>	GND
H	L	GND	HV <sub>IN</sub>
L	H	LV <sub>IN</sub>	GND
L	L	GND	LV <sub>IN</sub>

## Timing Diagram

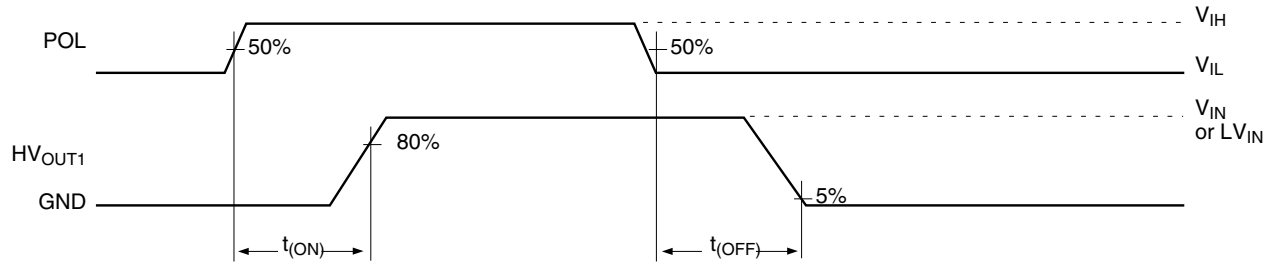


Figure 1

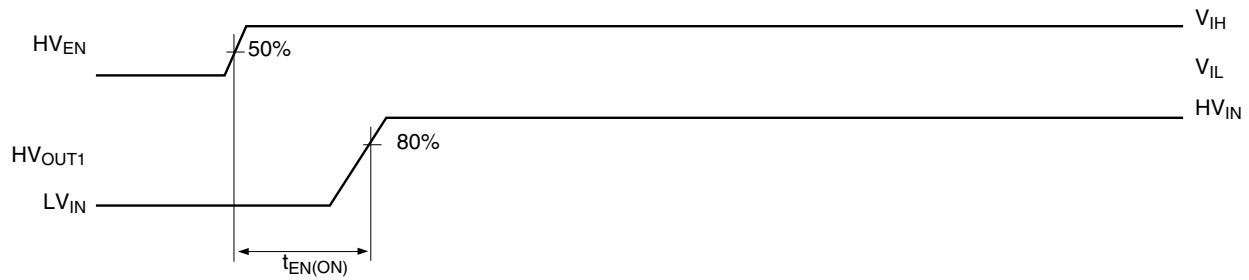


Figure 2

## Block Diagram

