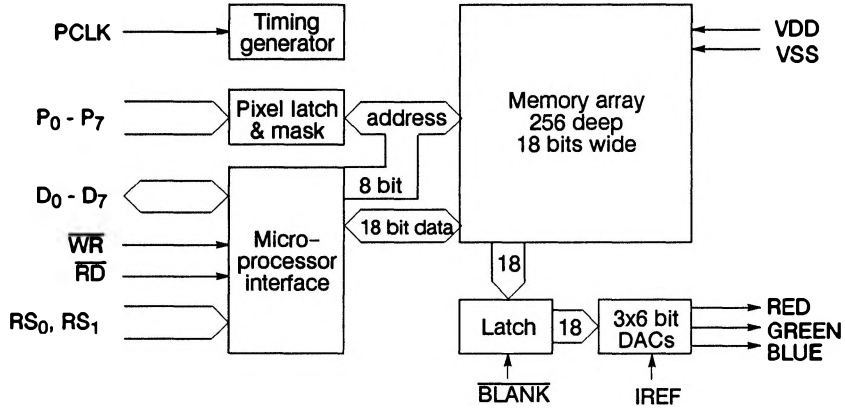
IMS G176
IMS G176L
High performance CMOS colour look-up table

Designed to be compatible with
IBM PS/2, VGA graphics systems



FEATURES

- Compatible with the RS170 video standard.
- Pixel rates up to 66MHz.
- 256K possible colours.
- Single monolithic, high performance CMOS.
- Pixel word mask.
- RGB analogue output, 6 bit DAC per gun.
- Composite blank on all three channels.
- Low DAC glitch energy.
- Video signal output into 37.5Ω.
- Up to 8 bits per pixel.
- TTL compatible inputs.
- Microprocessor compatible interface.
- Single +5V power supply.
- Low power dissipation, 950mW max. at maximum pixel rate.
- Standard 600 mil 28 pin DIL or 32 pin or 44 pin Plastic LCC.
- Pin compatible with IMS G171.
- Power down capability.

DESCRIPTION

The IMS G176/L integrates the functions of a colour look-up table (or colour palette), digital to analogue converters and bi-directional microprocessor interface into a single 28 pin DIL, 32 pin or 44 pin PLCC package. The IMS G176L is a power down version of the IMS G176.

The device is capable of driving a doubly-terminated 75Ω line with no external buffering, and composite blank signals can be generated on all three outputs.

Capable of displaying 256 colours from a total of 262,144 colours, the IMS G176 replaces TTL/ECL systems, giving reduced component cost, board area and power consumption.

The pixel word mask allows displayed colours to be changed in a single write cycle rather than by modifying the look-up table.

4.1 Pin designations

4.1.1 Pixel Interface

Signal	Pin number			I/O	Signal name	Description
	DIL	PLCC				
		32	44			
PCLK	13	14	40	I	Pixel Clock	The rising edge of the Pixel Clock signal controls the sampling of values on the Pixel Address and Blank inputs. The Pixel Clock also controls the progress of these values through the three stage pipeline of the colour look-up table to the analogue outputs.
P_0-P_7	5-12	6-13	32-39	I	Pixel Address	The byte wide value sampled on these inputs is masked by the Pixel mask register and then used as the address into the colour look-up table.
$\overline{BLANK}$	16	20	7	I	Blank	A low value on this input, when sampled, will cause a colour value of zero to be applied to the inputs of the DACs regardless of the colour value of the current pixel.

4.1.2 Analogue Interface

Signal	Pin number			I/O	Signal name	Description
	DIL	PLCC				
		32	44			
RED BLUE GREEN	1 2 3	2 3 4	25 26 27	O O O		These signals are the outputs of the 6 bit DACs. Each DAC is composed of 63 current sources whose outputs are summed. The number of current sources active is controlled by the 6 bit binary value applied.
IREF	4	5	28	I	Reference current	The reference current drawn from VDD (or AVDD) via the IREF pin determines the current sourced by each of the current sources in the DACs.

4.1.3 Microprocessor Interface

Signal	Pin number			I/O	Signal name	Description
	DIL	PLCC				
		32	44			
$\overline{WR}$	25	29	16	I	Write enable	The Read Enable and Write Enable signals control the timing of read and write operations on the microprocessor interface.
$\overline{RD}$	15	19	6	I	Read enable	Most of the operations on the microprocessor interface can take place asynchronously to the pixel stream being processed by the colour look-up table. Various minimum periods between operations are specified (in terms of Pixel Clock) to allow this asynchronous behaviour. The Read and Write Enable signals should not be asserted at the same time.
RS_0, RS_1	26,27	30,31	17,18	I	Register select	The values on these inputs are sampled on the falling edge of the active enable signal ($\overline{RD}$ or $\overline{WR}$); they specify which one of the internal registers is to be accessed. See Internal Register description for the function of these registers.
D_0–D_7	17-24	21-28	8-15	I/O	Program Data	Data is transferred between the 8 bit wide Program Data bus and the registers within the IMS G176/L under control of the active enable signal ($\overline{RD}$ or $\overline{WR}$). In a write cycle the rising edge of $\overline{WR}$ validates the data on the program data bus and causes it to be written to the register selected. The rising edge of the $\overline{RD}$ signal signifies the end of a read cycle, after which the program data bus will cease to carry the contents of the register addressed and will go to a high impedance state.

4.1.4 Power supply

Signal	Pin number			Signal name	Description
	DIL	PLCC			
		32	44		
VDD	28			Power supply	Digital and analogue supply pads are bonded out to a single pin on the DIL package. The package contains a high-frequency decoupling capacitor between VDD and VSS to ensure a high quality analogue supply.
VDD		17	4,21,22	Digital supply	Digital and analogue supply pads are bonded out separately on the PLCC package to give highest possible noise immunity. Due to package size limitations the decoupling capacitor capacitor must be provided externally (see section on 'Power supply decoupling')
AVDD		32	20	Analogue supply	
VSS	14	16	3	Ground	

4.1.5 Internal registers

RS_1	RS_0	Size (bits)	Register name	Description
				There is a single Address register within the IMS G176/L. This register can be accessed through either register select 0,0 or 1,1
0	0	8	Address (write mode)	Writing a value to register 0,0 performs the following operations which would normally precede writing one or more new colour definitions to the colour look-up table: a) Specifies an address within the colour look-up table. b) Initialises the Colour Value register.
1	1	8	Address (read mode)	Writing a value to register 1,1 performs the following operations which would normally precede reading one or more colour definitions from the colour look-up table: a) Specifies an address within the the colour look-up table. b) Loads the Colour Value register with the contents of the location in the look-up table addressed and then increments the Address register. A read from register 0,0 is functionally equivalent to a read from 1,1.
0	1	18	Colour Value	The Colour Value register is internally an 18 bit wide register used as a buffer between the microprocessor interface and the colour look-up table. A value can be read from or written to this register by a sequence of three byte transfers at this register address. When a byte is written only the least significant six bits D_0–D_5 are used. When a byte is read only the least significant six bits contain information – the most significant two bits being set to zero. The sequence of data transfer is red first, green second and blue last. After writing three values to this register its contents are written to the location in the colour look-up specified by the Address register. The Address register then increments. After reading three values from this register the contents of the location in the colour look-up table specified by the Address register are copied into the Colour Value register. The Address register then increments. Each transfer between the Colour Value register and the colour look-up table replaces the normal pixel mapping operations of the IMS G176/L for a single pixel.
1	0	8	Pixel Mask	The Pixel Mask register can be used to mask selected bits of the Pixel Address value applied to the Pixel Address inputs (P_0–P_7). A one in a position in the mask register leaves the corresponding bit in the Pixel Address unaltered, while a zero sets that bit to zero. The Pixel Mask register does not affect the Address generated by the Microprocessor Interface when the look-up table is being accessed via that interface.

4.2 Device description

The IMS G176/L is intended for use as the output stage of raster scan video systems. It contains a high speed random access store (or look-up table) of 256 × 18 bit words, three 6 bit high speed DACs, a microprocessor interface and a pixel word mask.

An 8 bit value read in on the Pixel Address inputs is used as a read address for the look-up table and results in an 18 bit data word being output from the table. This data is partitioned as three fields of 6 bits, each field being applied to the inputs of a 6 bit DAC.

Pixel rates of up to 66 MHz are achieved by pipelining the memory access over three clock periods.

An externally generated blank signal can be input to the IMS G176/L. This signal acts on all three of the analogue outputs. The $\overline{\text{BLANK}}$ signal is delayed internally so that it appears at the analogue outputs with the correct relationship to the pixel stream.

The contents of the look-up table can be accessed via an 8 bit wide microprocessor interface. The use of an internal synchronising circuit allows colour value accesses to be totally asynchronous to the video path.

A pixel word mask is included to allow the incoming pixel address to be masked. This permits rapid changes to the effective contents of the colour look-up table to facilitate such operations as animation, overlays and flashing objects. Operations on the contents of the mask register can also be totally asynchronous to the pixel stream.

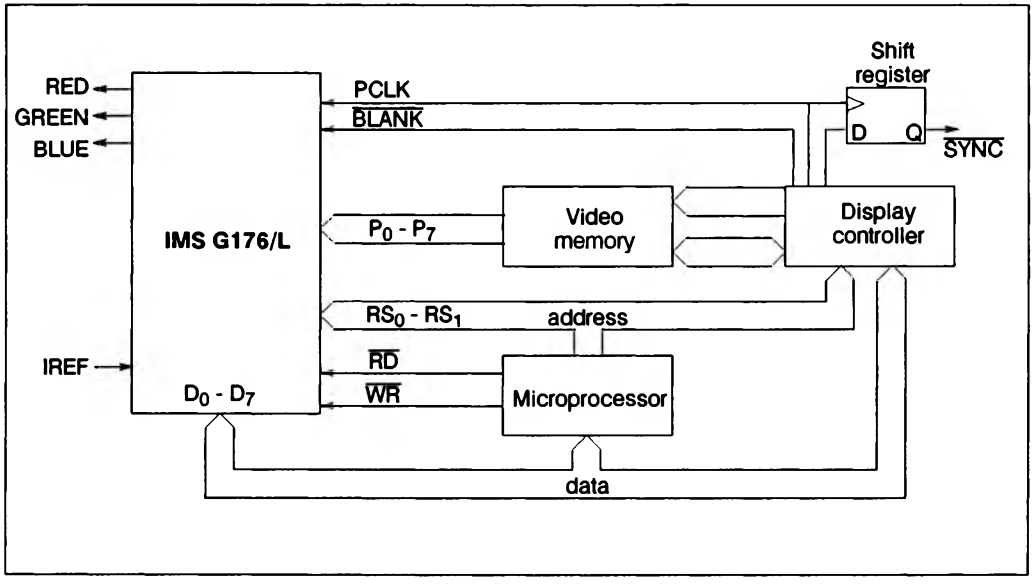


Figure 4.1Typical IMS G176/L application

4.2.1 Video path

P_0–P_7 and $\overline{\text{BLANK}}$ inputs are sampled on the rising edge of Pixel Clock, their effect appears at the analogue outputs after three further rising edges of Pixel Clock (see figure 4.2).

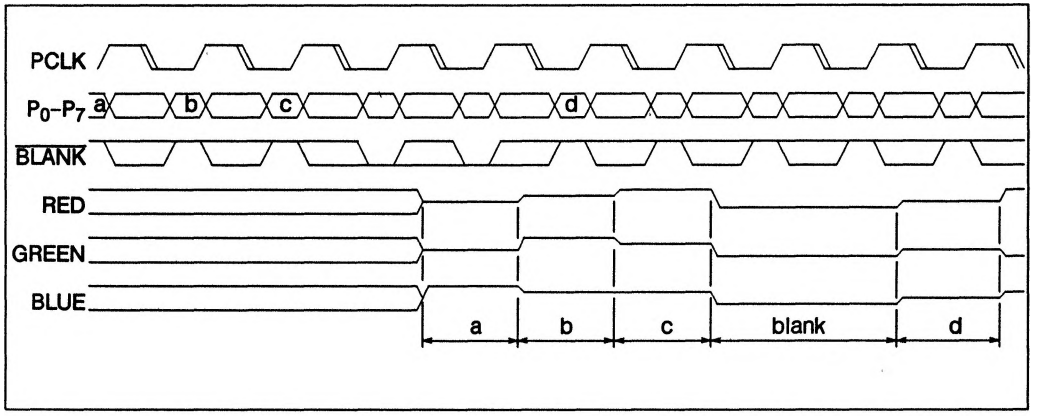


Figure 4.2

4.2.2 Analogue outputs

The outputs of the DACs are designed to be capable of producing 0.7 volt peak white amplitude with an IREF of 9.07 mA when driving a doubly terminated 75Ω load. This corresponds to an effective DAC output load ($R_{EFFECTIVE}$) of 37.5Ω.

The $\overline{BLANK}$ input to the IMS G176/L acts on all three of the analogue outputs. When the $\overline{BLANK}$ input is low a binary zero is applied to the inputs of the DACs.

The expression for calculating IREF with various peak white voltage/output loading combinations is given below:

$$IREF = \frac{V_{PEAKWHITE}}{2.058 \times R_{EFFECTIVE}}$$

Note that for all values of IREF and output loading:

$$V_{BLACK\ LEVEL} = 0$$

4.2.3 Microprocessor Interface

Below are listed the three microprocessor interface registers within the IMS G176/L and the four locations through which they can be accessed:

RS_1	RS_0	Register name
0	0	Address (write mode)
1	1	Address (read mode)
0	1	Colour Value
1	0	Pixel Mask

The contents of the colour look-up table can be accessed via the Colour Value register and the Address register.

Writing to the look-up table

To set a new colour definition a value specifying a location in the colour look-up table is first written to the write mode Address register. The values for the red, green and blue intensities are then written in succession to the Colour Value register. After the blue data is written to the Colour Value register the new colour definition is transferred to the colour look-up table and the Address register is automatically incremented.

As the Address register increments after each new colour definition has been transfered from the Colour Value register to the colour look-up table, it is simple to write a set of consecutive locations with new colour definitions. First the start address of the set of locations is written to the write mode Address register; then the colour definitions for each location are written sequentially to the Colour Value register.

Reading from the look-up table

To read a colour definition a value specifying the location in the look-up table to be read is written to the read mode Address register. After this value has been written, the contents of the location specified are copied to the Colour Value register and the Address register is then automatically incremented.

The red, green and blue intensity values can be read by a sequence of three reads from the Colour Value register. After the blue value has been read the location in the look-up table currently specified by the Address register is copied to the Colour Value register and the Address register is again incremented automatically.

Thus a set of colour definitions in consecutive locations can be read simply by writing the start address of the set to the read mode Address register and then sequentially reading the colour definitions for each location in the set.

Whenever the Address register is updated any unfinished colour definition read or write is aborted and a new one may begin.

Asynchronous microprocessor interface access

Accesses to all registers may occur without reference to the high speed timing of the pixel stream being processed by the IMS G176/L. Data transfers between the look-up table and the Colour Value register and modifications to the Pixel Mask register are synchronised to the Pixel Clock by internal logic. This is done in the period between microprocessor accesses. Thus, various minimum periods are specified between microprocessor interface accesses to allow for the appropriate transfers or modifications to take place.

The Pixel Mask register

The pixel address used to access the colour look-up table through the pixel interface is the result of the bitwise ANDing of the incoming pixel address and the contents of the Pixel Mask register. This pixel masking process can be used to alter the displayed colours without altering the video memory or the look-up table contents. Thus, by partitioning the colour definitions by one or more bits in the pixel address such effects as rapid animation, overlays and flashing objects can be produced.

The Pixel Mask register is completely independent of the Address and Colour Value registers.

4.3 Electrical specifications

4.3.1 Absolute maximum ratings *

Symbol	Parameter	Min.	Max.	Units	Notes
VDD/AVDD	DC supply voltage		7.0	V	
	Voltage on input and output pins	VSS-1.0	VDD+0.5	V	
TS	Storage temperature (ambient)	-55	,125	°C	
TA	Temperature under bias	-40	85	°C	
PDmax	Power dissipation		1.5	W	
	Reference current	-15		mA	
	Analogue output current (per output)		45	mA	
	DC digital output current		25	mA	

Notes

*Stresses greater than those listed under 'Absolute maximum ratings' may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

4.3.2 DC operating conditions

Symbol	Parameter	Min.	Typ.	Max.	Units	Notes (1)
VDD	Positive supply voltage	4.50	5.0	5.50	volts	2,3,IMS G176/L-40/50
VDD	Positive supply voltage	4.75	5.0	5.25	volts	2,3,IMS G176/L-66
VSS	Ground		0		volts	
VIH	Input logic '1' voltage	2.0		VDD+0.5	volts	3
VIL	Input logic '0' voltage	−0.5		0.8	volts	4
TA	Ambient operating temperature	0		70	°C	5
IREF	Reference current	−7.0		−10	mA	6

Notes

1 All voltages are with respect to VSS unless specified otherwise.

2 This parameter allows for a range of fixed power supply voltages to be used; it does not imply that the supply voltage should be allowed to vary dynamically within these limits.

3 These voltage ranges apply equally for AVDD and VDD when using the PLCC packaged device.

4 VIL(min) = −1.0V for a pulse width not exceeding 25% of the duty cycle (t_{CHCH}) or 10ns, whichever is the smaller value.

5 With a 400 linear ft/min transverse air flow.

6 Reference currents below the minimum specified may cause the analogue outputs to become invalid.

DC electrical characteristics

Symbol	Parameter	Min.	Max.	Units	Notes (1,2,3)
IDD	Average power supply current		190	mA	4, IMS G176/L-66
IDD	Average power supply current		160	mA	4, IMS G176/L-50
IDD	Average power supply current		155	mA	4, IMS G176/L-40
VREF	Voltage at IREF input (pin 4)	VDD−3	VDD	volts	5
IIN	Digital input current (any input)		±10	µA	6,7
IOZ	Off state digital output current		±50	µA	6,8
VOH	Output logic '1'	2.4		volts	IO = −5mA
VOL	Output logic '0'		0.4	volts	IO = 5mA

Notes

1 All voltages are with respect to VSS unless specified otherwise.

2 The Pixel Clock frequency must be stable for a period of at least 20µs after power-up (or after change in a Pixel Clock frequency) before proper device operation is guaranteed.

3 Over the range of the DC operating conditions unless specified otherwise.

4 IO = IO(max). IDD is dependent on digital loading and cycle rate, the specified values are obtained with the outputs unloaded and at the maximum rated Pixel Clock frequency.

5 These voltages apply equally for AVDD and VDD when using the PLCC packaged device.

6 VDD = max, VSS $\leq$ VIN $\leq$ VDD.

7 On digital inputs (P_0–P_7, PClk, $\overline{RD}$, $\overline{BLANK}$, $\overline{WR}$ and RS_0–RS_1).

8 On digital input/output (D_0–D_7).

4.3.3 Power down

The IMS G176L is a 'power-down' version of the IMS G176. It is designed to support the lap-top market which requires the colour look-up table to dissipate minimal power when not in use.

Symbol	Parameter	Min.	Max.	Units	Notes
IDDSB	Standby power supply current		10	mA	1-5

Notes

1 All voltages with respect to VSS unless otherwise stated.

2 Table 4.1 defines the conditions required to guarantee IDD standby.

3 PCLK should be held DC low as specified in table 4.1.

4 $\overline{RD}$ should be held high as specified in table 4.1 to prevent the data pins (D0-D7) from driving and therefore drawing supply current. If, however there is no external load resistance between D0-D7 data pins and GND or VDD, then taking $\overline{RD}$ low will have no detrimental effect on IDD standby.

5 The voltage on any pin shall not be greater than VDD or less than VSS.

Pin name	Required value	Units	Notes
RED	$\geq$0 and $\leq$VDD	V	
GREEN	$\geq$0 and $\leq$VDD	V	
BLUE	$\geq$0 and $\leq$VDD	V	
IREF	<10	µA	
P0-P7	<0.2	V	
PCLK	<0.2	V	
RD	>VDD-0.2	V	
BLANK	<0.2 or >VDD-0.2	V	
D0-D7	<0.2	V	
WR	>VDD-0.2	V	
RS0	<0.2 or >VDD-0.2	V	
RS1	<0.2 or >VDD-0.2	V	
VDD	4.5<VDD<5.5	V	

Table 4.1 Conditions to guarantee IDD standby

4.3.4 DAC characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Notes (1,2,3)
	Resolution	6			bits	
VO(max)	Output voltage			1.5	volts	IO≤10mA
IO(max)	Output current			−21	mA	VO≤1V
	Full scale error			±5	%	4
	DAC to DAC correlation error			±2	%	5
	Integral linearity error			±0.5	LSB	6
	Rise time (10% to 90%)			6	ns	7, IMS G176/L-66
	Rise time (10% to 90%)			8	ns	7, IMS G176/L-40/50
	Full scale settling time			15.3	ns	7,8,9, IMS G176/L-66
	Full scale settling time			20	ns	7,8,9, IMS G176/L-50
	Full scale settling time			25	ns	7,8,9, IMS G176/L-40
	Glitch energy		120		pVsec	7,9

Notes

1 All voltages are with respect to VSS unless specified otherwise.

2 The Pixel Clock frequency must be stable for a period of at least 20μs after power-up (or after change in a Pixel Clock frequency) before proper device operation is guaranteed.

3 Tested over the operating temperature range and at nominal supply voltage with IREF = -9.07mA.

4 Full scale error from the value predicted by the design equations.

5 About the mid point of the distribution of the three DACs measured at full scale deflection.

6 Linearity measured from the best fit line through the DAC characteristic. Monotonicity guaranteed.

7 Load = 37.5Ω + 30pF with IREF = -9.07mA.

8 From a 2% change in the output voltage until settling to within 2% of the final value.

9 This parameter is sampled, not 100% tested.

4.3.5 AC test conditions

Input pulse levels	VSS to 3V
Typical input rise and fall times (10% to 90%)	3ns
Digital input timing reference level	1.5V
Digital output timing reference level	0.8V and 2.4V
Digital output load	see figure NO TAG

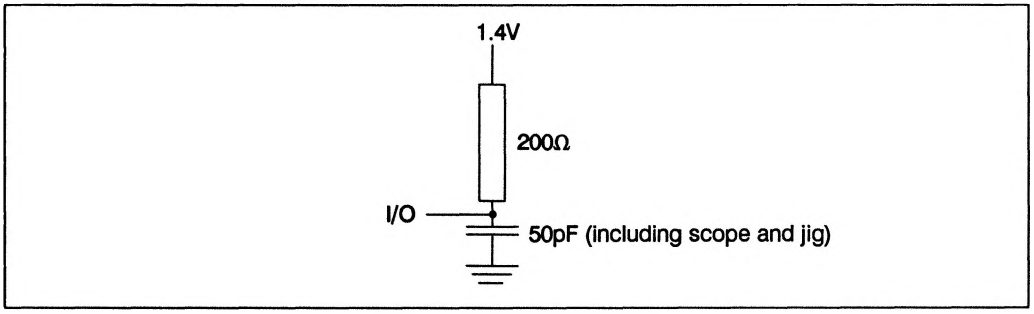


Figure 4.3Digital output load

4.3.6 Capacitance

Symbol	Parameter	Min.	Max.	Units	Notes (1,2)
CI	Digital input		7	pF	
CO	Digital output		7	pF	3
COA	Analogue output		10	pF	4

Notes

1 These parameters are sampled, not 100% tested.

2 Measured on a BOONTON METER.

3 $\overline{RD} \geq$ VIH(min) to disable D_0-D_7

4 BLANK $\leq$ VIL(max) to disable RED, GREEN and BLUE.

4.3.7 Video operation (figure 4.4)

Symbol	Parameter	All	40 MHz	50 MHz	66 MHz	Units	Notes
		Max.	Min.	Min.	Min.		
tCHCH	PCLK period	10000	25	20	15.1	ns	
ΔtCHCH	PCLK jitter	±2.5				%	1
tCLCH	PCLK width low	10000	9	6	5	ns	
tCHCL	PCLK width high	10000	7	6	5	ns	
tPVCH	Pixel address set-up time		5	4	3	ns	2
tCHPX	Pixel address hold time		5	4	3	ns	2
tBVCH	$\overline{BLANK}$ setup time		5	4	3	ns	
tCHBX	$\overline{BLANK}$ hold time		5	4	3	ns	
tCHAV	PCLK to valid DAC output	30	5	5	5	ns	3
ΔtCHAV	Differential output delay	2				ns	4
	Pixel clock transition time	50				ns	

Notes

1 This parameter allows for variation in the Pixel Clock frequency, but does not permit the Pixel Clock period to vary outside the minimum and maximum values for Pixel Clock (tCHCH) period specified above.

2 It is required that the Pixel Address input to the colour look-up table be set up as a valid logic level with the appropriate setup and hold times to each rising edge of PCLK (this requirement must be met during the blanking period).

3 A valid analogue output is defined as when the changing analogue signal is half way between its successive values. This parameter is stable with time but can vary between different devices and may vary with different DC operating conditions.

4 Between different analogue outputs on the same device.

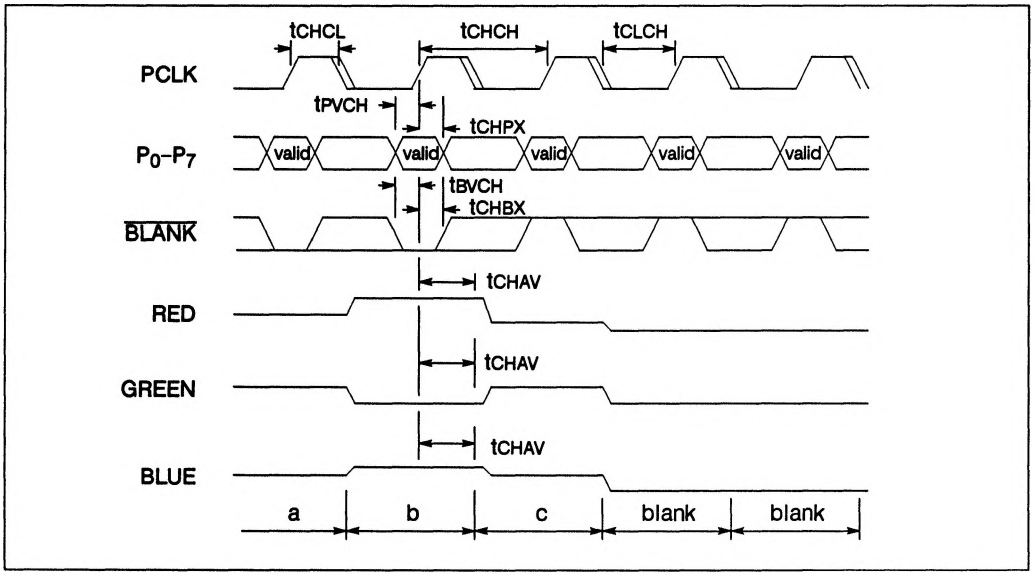


Figure 4.4 Video operation

4.3.8 Microprocessor interface operation

Symbol	Parameter	All	40 MHz	50 MHz	66 MHz	Units	Notes
		Max.	Min.	Min.	Min.		
tWLWH	$\overline{WR}$ pulse width low		50	50	50	ns	
tRLRH	$\overline{RD}$ pulse width low		50	50	50	ns	
tSVWL	Register select setup time		15	10	10	ns	
tSVRL	Register select setup time		15	10	10	ns	
tWLSX	Register select hold time		15	10	10	ns	
tRLSX	Register select hold time		15	10	10	ns	
tDVWH	Write data setup time		15	10	10	ns	
tWHDX	Write data hold time		15	10	10	ns	
tRLQX	Output turn-on delay		5	5	5	ns	
tRLQV	Read enable access time	40				ns	
tRHQX	Output hold time		5	5	5	ns	
tRHQZ	Output turn-off delay	20				ns	1
tWHWL1	Successive write interval						
tWHRL1	Write followed by read interval						
tRHRL1	Successive read interval						
tRHWL1	Read followed by write interval		4xtCHCH +30ns			ns	2
tWHWL2	Write after colour write						
tWHRL2	Read after colour write						
tRHWL2	Write after colour read						
tRHRL2	Read after colour read		6xtCHCH +40ns			ns	2
tWHRL3	Read after read address write						
tCYC	Write/Read cycle time		6xtCHCH +40ns			ns	2,3
	Write/Read enable transition time	50				ns	

Notes

1 Measured ±200mV from steady output voltage.

2 This parameter allows for synchronisation between operations on the microprocessor interface and the pixel stream being processed by the colour look-up table.

3 From the rising edge of Read or Write pulse to the rising edge of the next Read or Write pulse.

Operations on the microprocessor port are internally synchronised to the pixel clock in the periods between cycles. This is the reason for the time between cycles on the microprocessor port being specified in terms of pixel clock periods.

In the case of the IMS G176/L the minimum cycle time for all accesses (defined as the period between successive rising edges of the read or write strobe) is 6×tCHCH +40ns.

For example, in the case of a 25MHz system the pixel clock period (tCHCH) would be 40ns and the minimum cycle time for accesses on the microprocessor port is:

$$6 \times 40ns + 40ns = 280ns$$

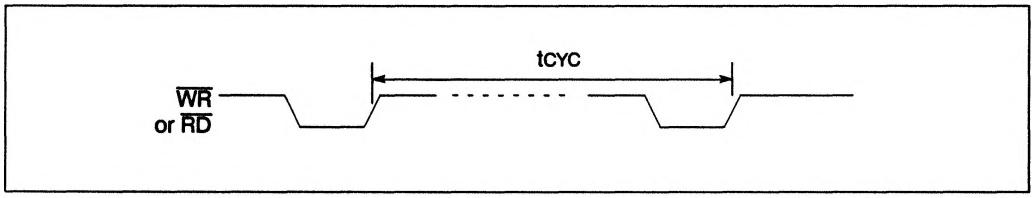


Figure 4.5 Write/Read cycle time

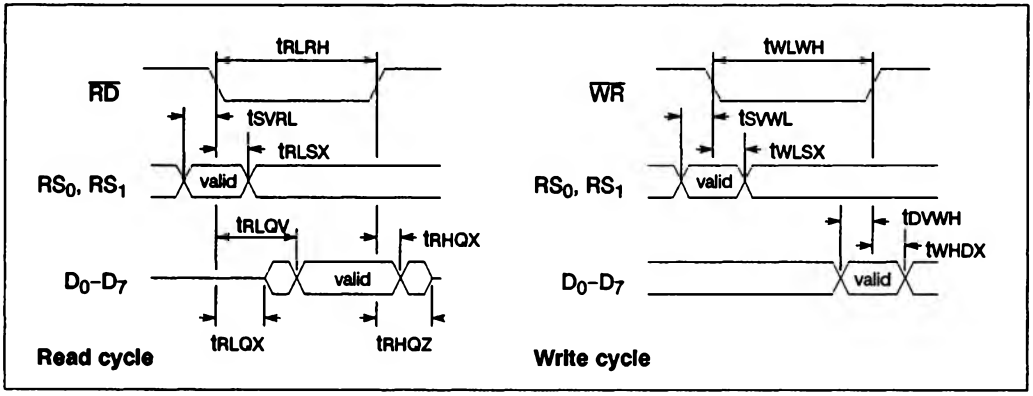


Figure 4.6 Basic read/write cycles

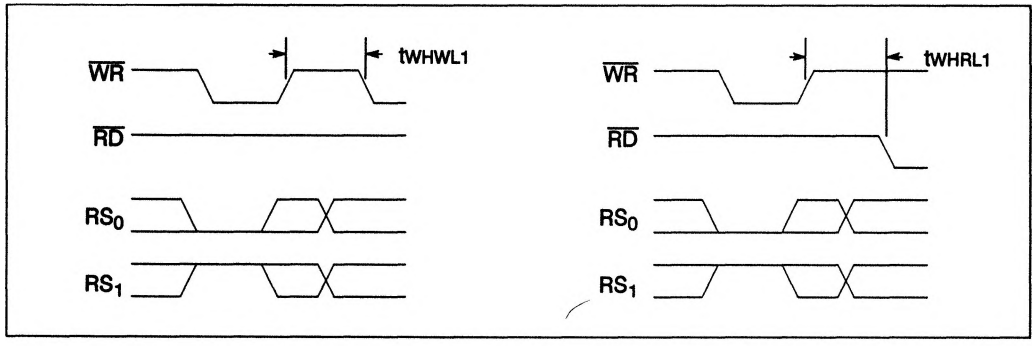


Figure 4.7 Write to pixel mask register followed by any access

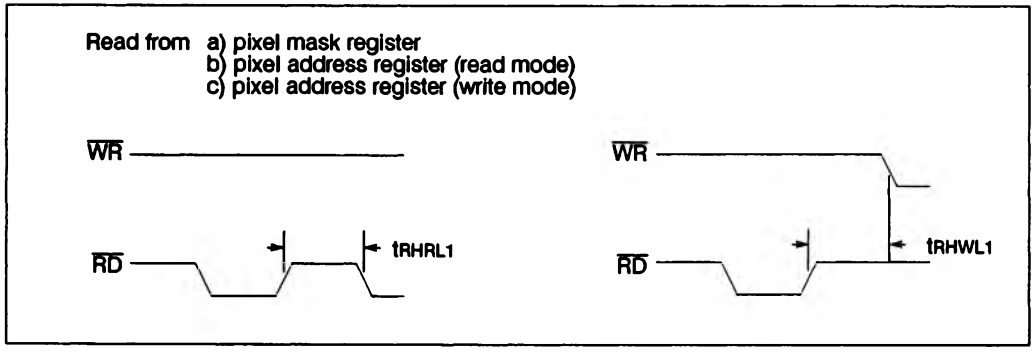


Figure 4.8 Read from register followed by any access

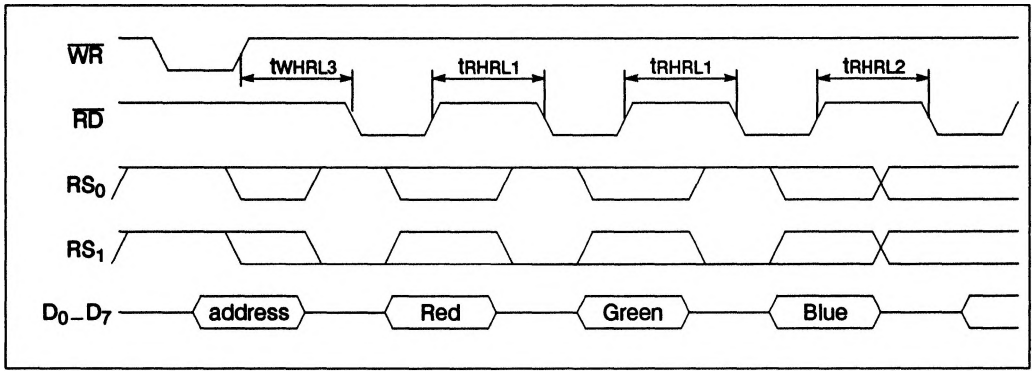


Figure 4.9 Colour value read followed by any read

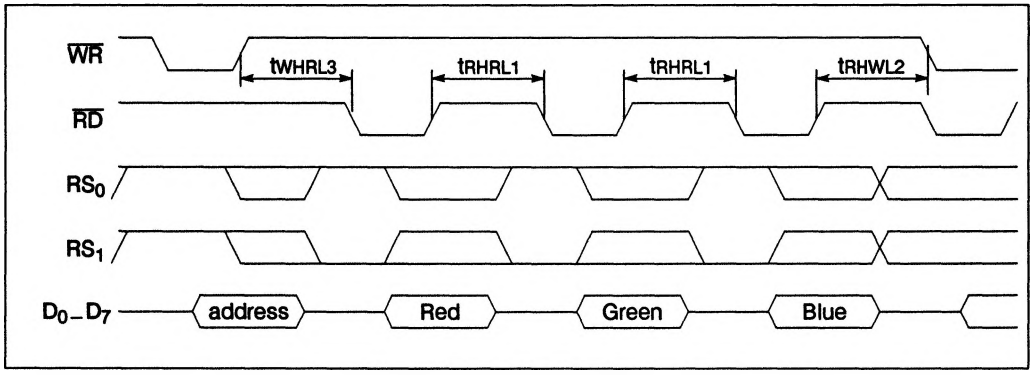


Figure 4.10 Colour value read followed by any write

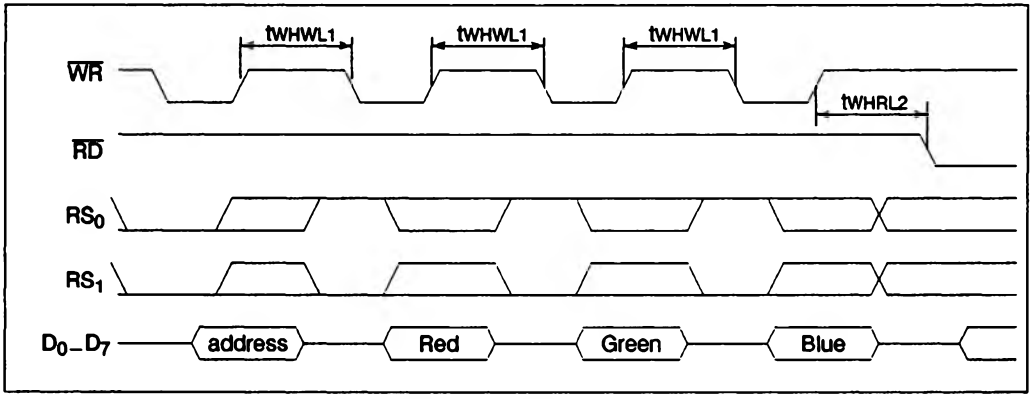


Figure 4.11 Colour value write followed by any read

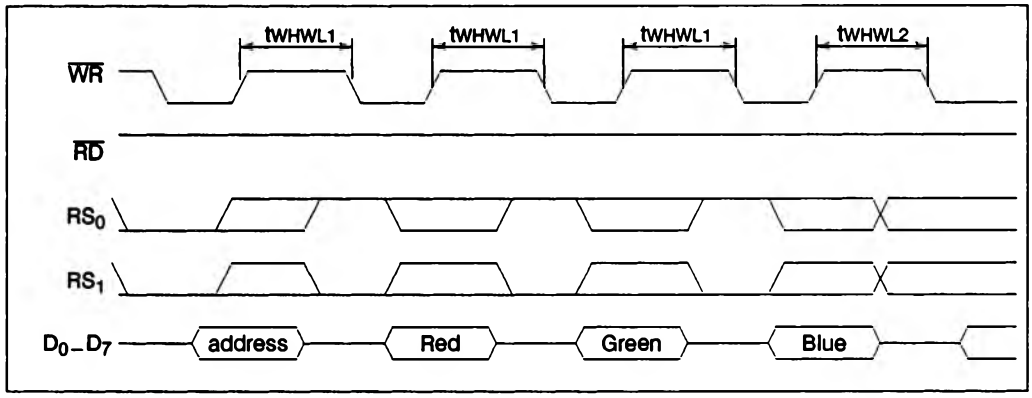


Figure 4.12 Colour value write followed by any write

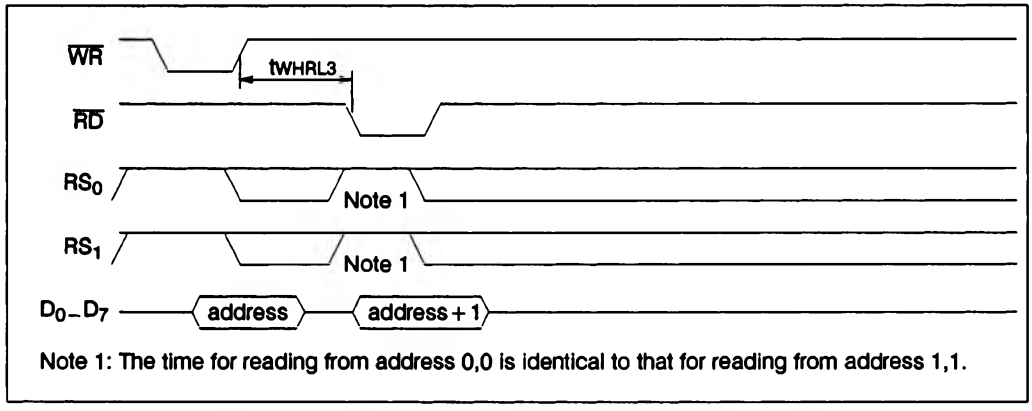


Figure 4.13 Write and read back address register (read mode)

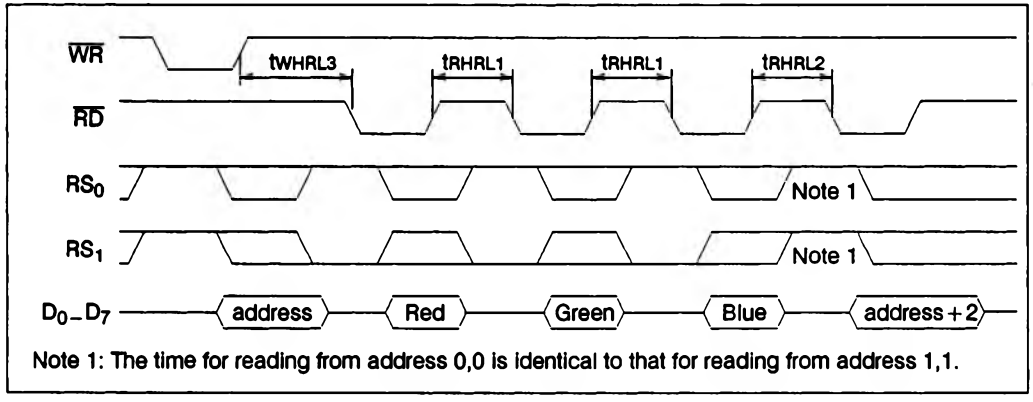


Figure 4.14 Read colour value then the address register (read mode)

4.4 Designing with the IMS G176/L

4.4.1 Board layout – general

The IMS G176/L is a high speed CMOS device. As such it has relatively low DC power requirements. However, CMOS devices may draw large transient currents from the power supply. To supply the transient currents present in high speed video circuitry it is essential that proper consideration is given to board layout and decoupling circuitry when using the IMS G176/L. A four layer board with separate power and ground planes is strongly recommended, since this will minimise differential noise and impedance in the supply.

4.4.2 Power supply decoupling

The DACs in the IMS G176/L are referenced to the positive power supply, so are fairly insensitive to ground supply noise. To ensure that switching noise generated by the digital sections of the IMS G176/L is not transmitted to the DAC circuitry, independent analogue and digital +5V supplies are provided on-chip.

When packaged in a PLCC, the analogue and digital supplies are bonded out to separate pins. It is recommended that a high frequency capacitor of around 100nF (preferably a chip capacitor) should be placed as close as possible to the package between VDD and VSS. A large tantalum capacitor (between 22μF and 47μF) should also be placed in parallel with this high-frequency capacitor. AVDD should be connected to the positive power plane by the smallest impedance path possible, e.g. a via right next to a pin (see figure 4.18).

In the DIL package both the analogue and digital supplies are bonded out to a single pin (VDD). Again it is recommended that a high-frequency 100nF capacitor in parallel with a large tantalum capacitor are provided externally to ensure a high quality analogue supply (see figure 4.19).

An inductor may also be added in series with the positive supply (AVDD and or VDD) to form a low-pass filter and so further improve the power supply local to the IMS G176/L (figure 4.18).

4.4.3 Analogue output – line driving

The DACs in the IMS G176/L are made from summed, switched current sources. IREF sets the current sourced by each current source, the digital input to each DAC determines how many current sources are active. The load resistance between the DAC output and VSS determines the voltage produced by each DAC.

The connection between the DAC outputs of the IMS G176/L and the RGB inputs of the monitor it is driving should be regarded as a transmission line. Impedance changes along the transmission line will result in the reflection of part of the video signal back along the transmission line. These reflections may result in a degradation of the picture displayed by the monitor. To ensure good signal fidelity, RF techniques should be observed. The PCB trace connecting the IMS G176/L to the offboard connector should be sized so as to form a transmission line of the correct impedance. Correctly matched RF connectors should be used to connect the PCB to the coaxial cable, and from the cable to the monitor being driven.

Two methods of DAC termination and their relative merits are described here.

Double termination

A load resistor is placed at both the DAC output and the monitor input. The resistor values should be equal to the characteristic impedance of the line.

Double termination of the DAC output allows both ends of the transmission line between the DAC outputs and the monitor inputs to be correctly matched, and thus should result in an ideal reflection free system.

This arrangement is relatively tolerant to variations in transmission line impedance (e.g. a mismatched connector) since no reflections occur from either end of the line.

Also the rise time of the DAC outputs is dependent on the RC time constant of the load it is driving. Thus, a double terminated DAC output will rise faster than any singly terminated output.

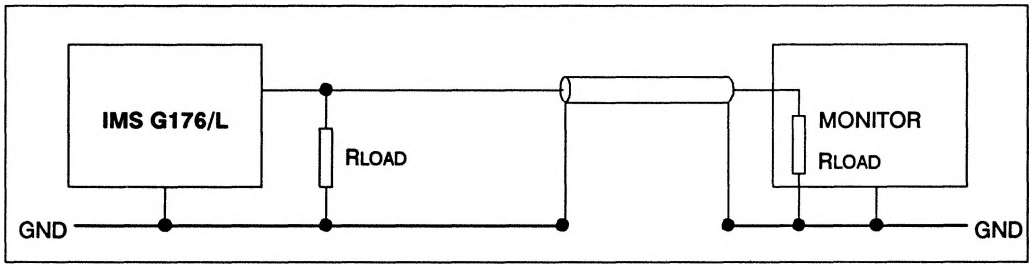


Figure 4.15 Double termination

Buffered signal

If the IMS G176/L is required to drive large capacitative loads (for instance long lossy cable runs) it may be necessary to buffer the DAC outputs. The buffer will have a relatively high input impedance. The connection between the DAC outputs and the buffer inputs should be considered as a transmission line. The buffer output will have a relatively low impedance so should be matched to the transmission line between it and the monitor with a series terminating resistor. The transmission line should be terminated at the monitor.

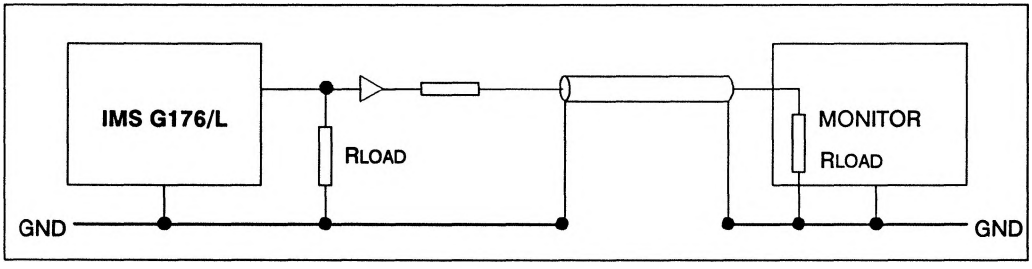


Figure 4.16 Buffered signal

4.4.4 Analogue output – protection

CMOS devices are susceptible to damage from high electrostatic voltages. Normal antistatic precautions should be observed when handling the IMS G176/L during system manufacture.

Once assembled into a system devices are much less exposed to static damage. However if the analogue outputs of the IMS G176/L are made available at connectors outside the graphic system they are still exposed to static damage and other hazardous voltages. Protection devices (e.g. IN4148 or any low cost silicon diode) should be considered at this exposed interface (see figures 4.18 and 4.19).

4.4.5 Digital input termination

The PCB trace lines between the outputs of the TTL devices driving the IMS G176/L and the input to the IMS G176/L have a low impedance source and are terminated with a high impedance. They behave like low impedance transmission lines, so signal transitions will be reflected from the high impedance input of the IMS G176/L. Similarly signal transitions will be inverted and reflected from the low impedance TTL output. To reduce or eliminate the ringing, and in particular the undershoot that reflections cause, line termination is recommended. The termination may either be series or parallel.

The recommended technique is to use series termination. Series termination has the advantage of drawing no DC current and using fewer components. Series termination is accomplished by placing a resistor in series with the signal line at the output of the TTL driver. This matches the TTL output impedance to that of the transmission line and so ensures that any signal incident on the TTL output is not reflected.

Some experimentation will have to be done to find the proper value to use for the series termination to minimise reflections, but generally a value around 100Ω will be required. because each design will result in a different signal impedance, a resistor of a predetermined value may not properly match the signal path impedance. The proper value of resistance should therefore be found empirically.

4.4.6 Current reference – design

To ensure that the output current of the DACs is predictable and stable with temperature variations, an active current reference is recommended. Figure 4.17 shows four designs of current reference.

Figure 4.17d shows the use of the LM334 precision current source as a current reference. It is shown in its temperature compensated configuration. The reference current is set by a single resistor (15Ω in this case) and is independent of the value of power supply voltage.

Figures 4.17a-c are similar circuits. Each circuit uses three resistors and the power supply voltage to set the reference current IREF through a transistor. In circuits 4.17b and 4.17c the thermal variations in the base emitter voltage of the transistor are compensated by the use of a forward biased diode (a transistor acting as a diode in the case of circuit 4.17c).

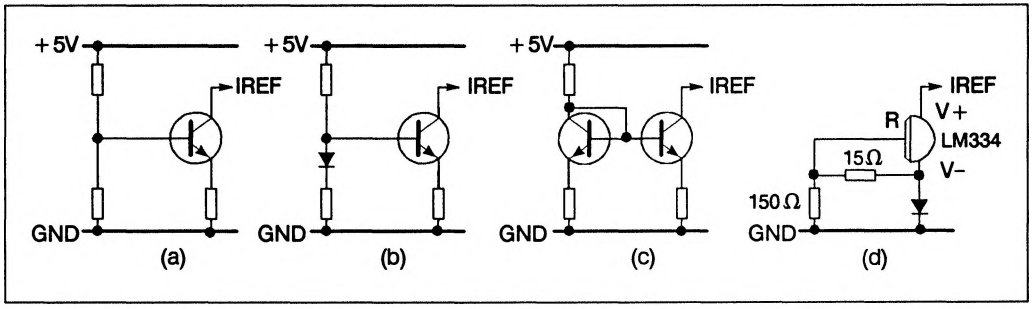


Figure 4.17

4.4.7 Current reference – decoupling

The DACs in the IMS G176/L are made from switched current sources which are based around a current mirror. The total current output by each DAC is determined by the number of active current sources and the reference current IREF.

So long as any supply variations are minor, or a suitably high quality current reference is used which tracks the variations, then no coupling capicitors need be used.

However, voltage variations on the supply not managed by the current reference circuit will result in variations in the DAC output current. If the bandwidth of the current reference circuit is not sufficient to track these supply variations it is recommended that a coupling capacitor (47μF to 100μF) in parallel with a high frequency capacitor of 100nF should be used to couple the IREF input to VDD (or to AVDD if the PLCC package is used). This will enable the current reference to track both low and high frequency variations in the supply.

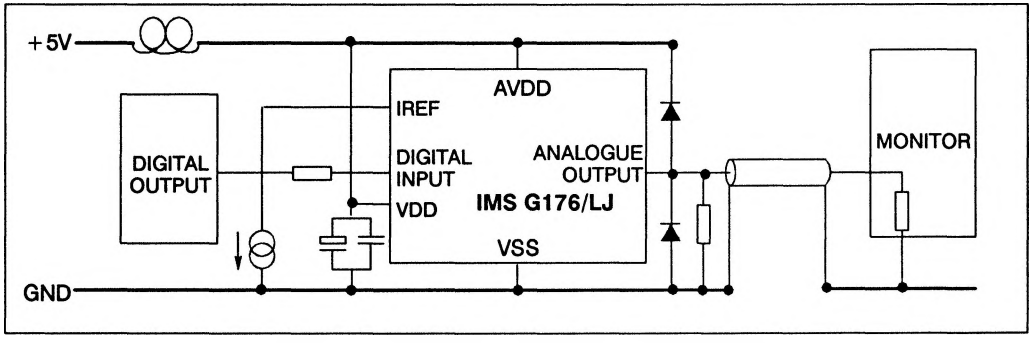


Figure 4.18 Suggested circuit using PLCC package

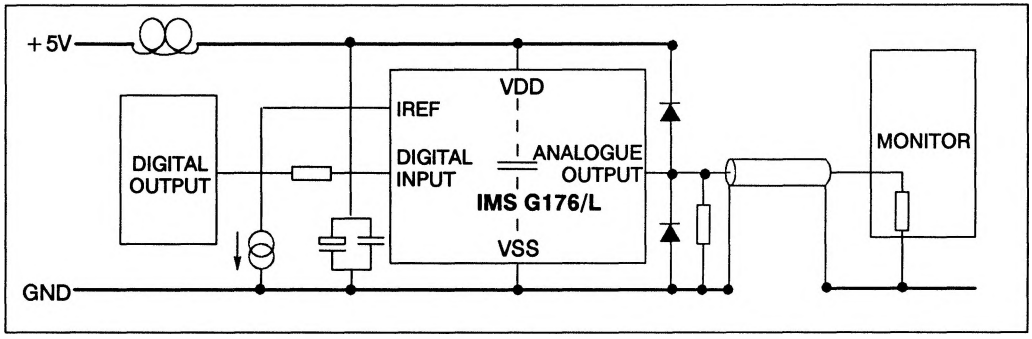


Figure 4.19 Suggested circuit using DIL package

4.5 Package specifications

4.5.1 28 pin dual-in-line package

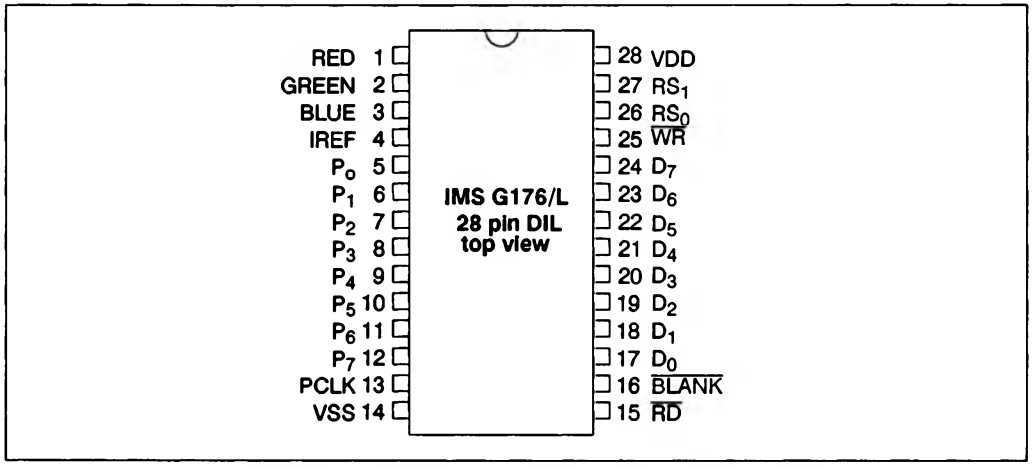


Figure 4.20 IMS G176/L 28 pin dual-in line package pinout

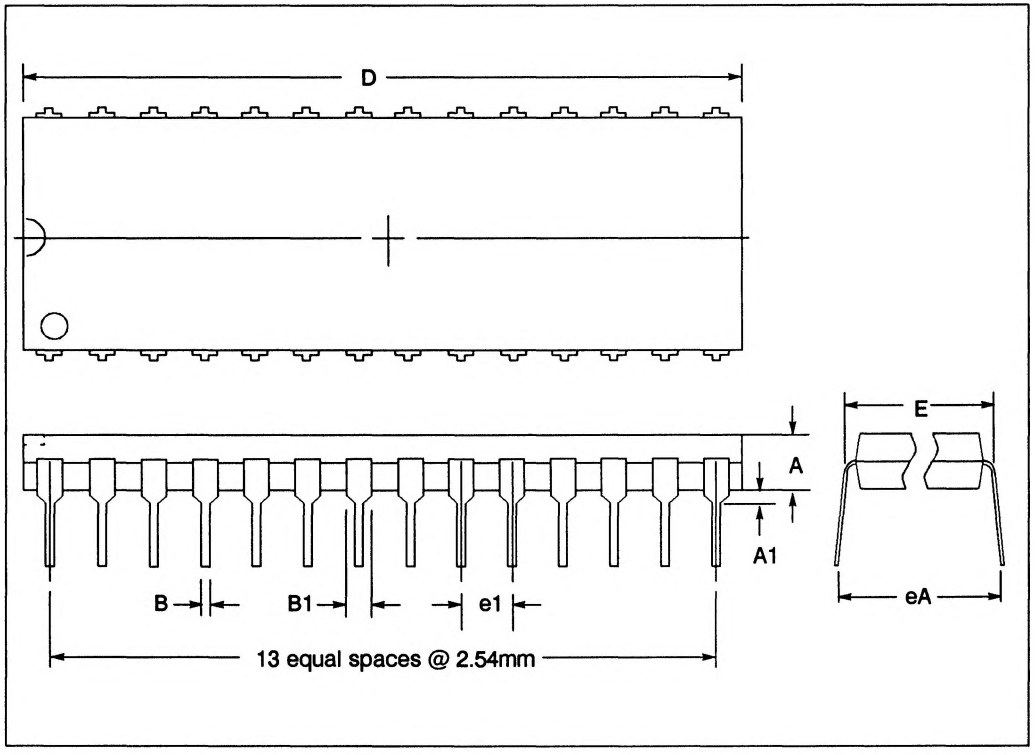


Figure 4.21 28 pin plastic dual-in-line package dimensions

DIM	Millimetres		Inches		Notes
	Min	Max	Min	Max	
A	3.556	4.064	0.140	0.160	
A1	0.508		0.020		
B	0.305		0.012		
B1	1.524		0.060		Typical
D	36.449	37.211	1.435	1.465	
E	15.164	15.316	0.597	0.603	
e1	2.286	2.794	0.090	0.110	
eA	15.848	16.644	6.240	0.655	

Table 4.2 28 pin plastic dual-in-line package dimensions

4.5.2 32 pin plastic leaded-chip-carrier package

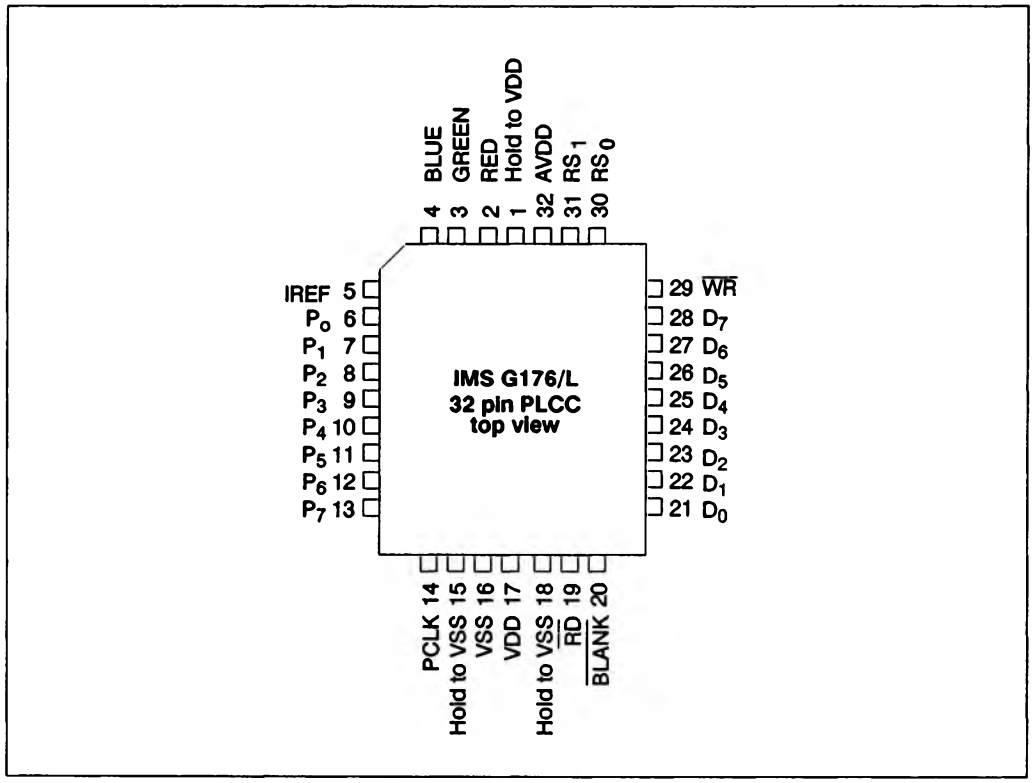


Figure 4.22 IMS G176/L 32 pin PLCC J-bend package pinout

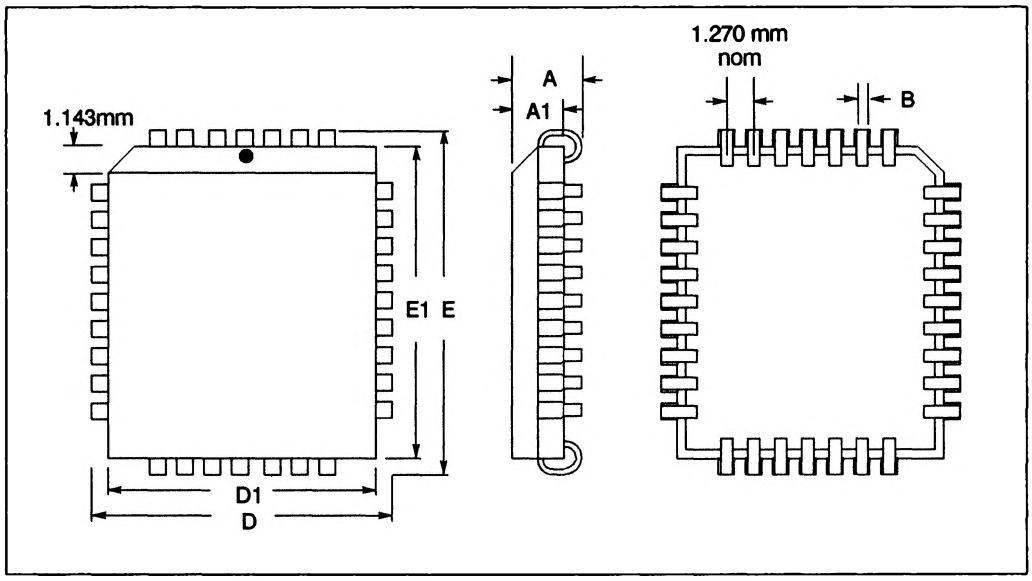


Figure 4.23 32 pin PLCC J-bend package dimensions

DIM	Millimetres		Inches		Notes
	Min	Max	Min	Max	
A	3.120	3.560	0.123	0.140	
A1	2.160		0.085		Nominal
B	0.432		0.017		Nominal
D	12.323	12.577	0.485	0.495	
D1	11.400	11.506	0.449	0.453	
E	14.859	15.113	0.585	0.595	
E1	13.940	14.046	0.549	0.553	

Table 4.3 32 pin PLCC J-bend package dimensions

4.5.3 44 pin plastic leaded-chip-carrier package

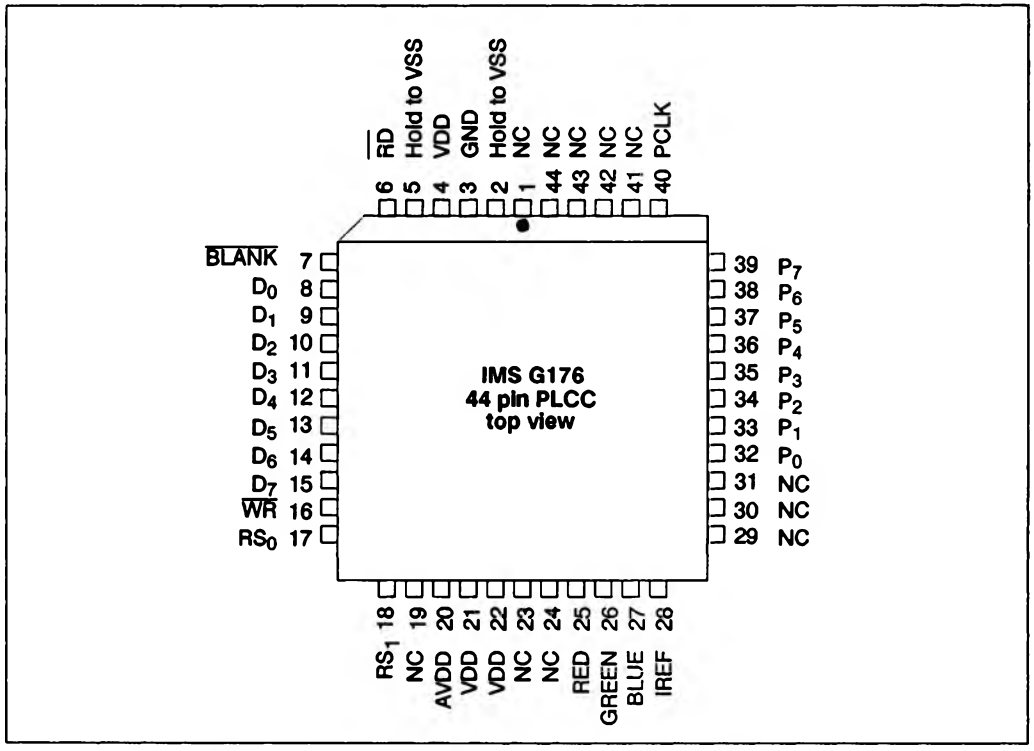


Figure 4.24 IMS G176 44 pin PLCC J-bend package pinout

Note

All **VDD** pins **must** be connected to the 5 Volt power supply.
All **GND** pins **must** be connected to ground.

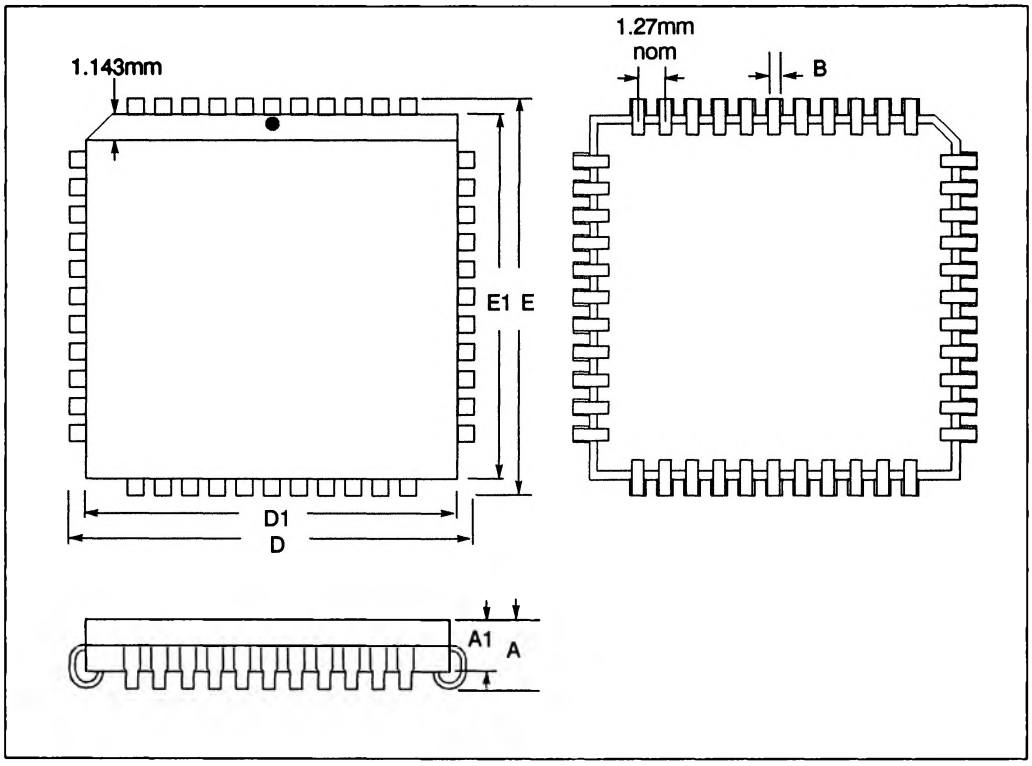


Figure 4.25 IMS G176 44 pin PLCC J-bend package dimensions

DIM	Millimetres		Inches		Notes
	Min	Max	Min	Max	
A	4.191	4.572	0.165	0.180	
A1	3.683	4.064	0.145	0.160	
B	0.457		0.018		
D	17.399	17.653	0.685	0.695	
D1	16.510	16.662	0.650	0.656	
E	17.399	17.653	0.685	0.695	
E1	16.510	16.662	0.650	0.656	

Table 4.4 44 pin PLCC J-bend package dimensions

4.5.4 Ordering Information

Device	Clock rate	Package	Part number	
			Standard	Low power
IMS G176	40 MHz	28 pin Plastic DIP	IMS G176P-40S	
IMS G176	50 MHz	28 pin Plastic DIP	IMS G176P-50S	IMS G176LP50S
IMS G176	66 MHz	28 pin Plastic DIP	IMS G176P-66S	
*IMS G176	80 MHz	28 pin Plastic DIP	IMS G176P-80S	
IMS G176	40 MHz	32 pin Plastic LCC	IMS G176J-40S	
IMS G176	50 MHz	32 pin Plastic LCC	IMS G176J-50S	IMS G176LJ50S
IMS G176	66 MHz	32 pin Plastic LCC	IMS G176J-66S	
*IMS G176	80 MHz	32 pin Plastic LCC	IMS G176J-80S	
IMS G176	40 MHz	44 pin Plastic LCC	IMS G176J-40Z	
IMS G176	50 MHz	44 pin Plastic LCC	IMS G176J-50Z	IMS G176LJ50Z
IMS G176	66 MHz	44 pin Plastic LCC	IMS G176J-66Z	
*IMS G176	80 MHz	44 pin Plastic LCC	IMS G176J-80Z	

Note: IMS G176J units can be supplied mounted on tape and reel.

* These parts will be available Q1 1991