IMS1624
CMOS
High Performance
16K x 4 Static RAM
with Output Enable

FEATURES

- INMOS' Very High Speed CMOS
- Advanced Process - 1.6 Micron Design Rules
- 16K x 4 Bit Organization with Output Enable
- 25, 30, 35, 45 and 55 nsec Address Access Times
- 25, 30, 35, 45 and 55 nsec Chip Enable Access Times
- Fully TTL Compatible
- Common Data Input & Output
- Three-state Output
- Power Down Function
- Single +5V ± 10% Operation
- 24-Pin, 300-mil DIP (JEDEC Std.)
- 28-Pin Ceramic LCC (JEDEC Std.)
- 24-Pin, 300-mil SOJ

DESCRIPTION

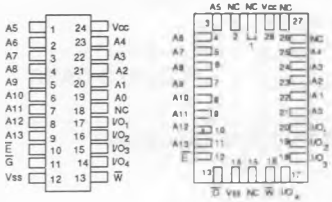
The INMOS IMS1624 is a high performance 16K x 4 CMOS Static RAM. The IMS1624 provides maximum density and speed enhancements with the additional CMOS benefits of lower power and superior reliability.

The IMS1624 features fully static operation requiring no external clocks or timing strobes, and equal address access and cycle times. The IMS1624 provides a Chip Enable (/E) function that can be used to place the device into a low-power standby mode. The IMS1624 also includes an Output Enable (/G) for fast access to data and enhanced bus contention control.

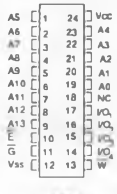
The IMS1624 is the functional equivalent of the IMS1620 with the addition of an Output Enable input.

The IMS1624M and IMS1624LM are MIL-STD-883 versions intended for military applications.

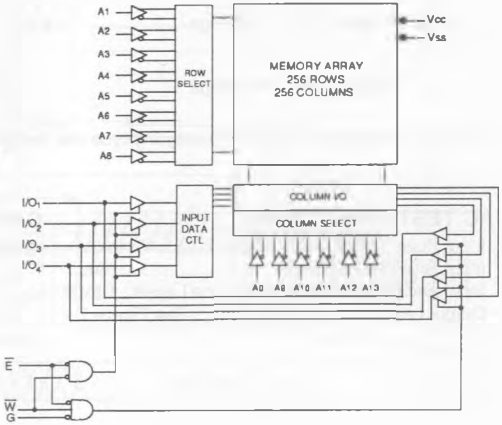
PIN CONFIGURATION



LOGIC SYMBOL



BLOCK DIAGRAM



PIN NAMES

A_0 - A_{13}	ADDRESS INPUTS	I/O	DATA IN/OUT
$\overline{W}$	WRITE ENABLE	Vcc	POWER (+5V)
$\overline{E}$	CHIP ENABLE	Vss	GROUND
$\overline{G}$	OUTPUT ENABLE		

ABSOLUTE MAXIMUM RATINGS*

Voltage on any pin relative to V_{SS}.....-2.0 to 7.0V
Voltage on I/O.....-1.0 to V_{CC}+0.5
Temperature Under Bias.....-55° C to 125°C
Storage Temperature .....-65° C to 150°C
Power Dissipation.....1W
DC Output Current.....25mA
(One output at a time, one second duration)

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	
V_{SS}	Supply Voltage	0	0	0	V	
V_{IH}	Input Logic "1" Voltage	2.0		Vcc+.5	V	All inputs
V_{IL}	Input Logic "0" Voltage	-1.0*		0.8	V	All inputs
T_A	Ambient Operating Temperature	0	25	70	°C	400 linear ft/min air flow

*V_{IL} min = -3 volts for pulse width <20ns, note b.

DC ELECTRICAL CHARACTERISTICS ($0°C \leq T_A \leq 70°C$) ($V_{CC} = 5.0V \pm 10\%$)[a]

SYMBOL	PARAMETER	MIN	MAX	UNITS	NOTES
I_{CC1}	Average Vcc Power Supply Current		110 100	mA mA	t_{AVAV} = 25ns and 30ns t_{AVAV} = 35, 45, and 55ns
I_{CC2}	Vcc Power Supply Current (Standby,Stable TTL Input Levels)		25	mA	$\overline{E} \geq V_{IH}$. All other inputs at $V_{IN} \leq V_{IL}$ or $\geq V_{IH}$
I_{CC3}	Vcc Power Supply Current (Standby, Stable CMOS Input Levels)		14	mA	$\overline{E} \geq$ (Vcc - 0.2). All other inputs at $V_{IN} \leq$ 0.2 or $\geq$ (Vcc - 0.2V)
I_{CC4}	Vcc Power Supply Current (Standby, Cycling CMOS Input Levels)		17	mA	$\overline{E} \geq$ (Vcc - 0.2). Inputs cycling at $V_{IN} \leq$ 0.2 or $\geq$ (Vcc - 0.2V)
I_{ILK}	Input Leakage Current (Any Input)		±1	µA	Vcc = max V_{IN} = Vss to Vcc
I_{OLK}	Off State Output Leakage Current		±5	µA	Vcc = max V_{IN} = Vss to Vcc
V_{OH}	Output Logic "1" Voltage	2.4		V	I_{OH} = -4mA
V_{OL}	Output Logic "0" Voltage		0.4	V	I_{OL} = 8mA

Note a: Icc is dependent on output loading and cycle rate, the specified values are obtained with the output unloaded.

AC TEST CONDITIONS

Input Pulse Levels ..... V_{SS} to 3V
Input Rise and Fall Times 5ns
Input and Output Timing Reference Levels.. 1.5V
Output Load ..... See Figure 1

CAPACITANCE[b] (T_A=25°C, f=1.0MHZ)

SYMBOL	PARAMETER	MAX	UNITS	CONDITIONS
C_{IN}	Input Capacitance	4	pF	ΔV = 0 to 3V
C_{OUT}	Output Capacitance	7	pF	ΔV = 0 to 3V

Note b: This parameter is sampled and not 100% tested

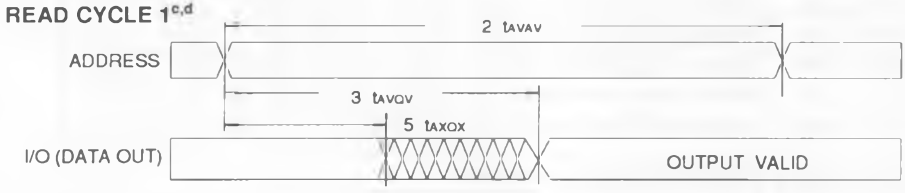
RECOMMENDED AC OPERATING CONDITIONS (0°C ≤ T_A ≤ 70°C) (V_{CC} = 5.0V ±10%)

READ CYCLE[g]

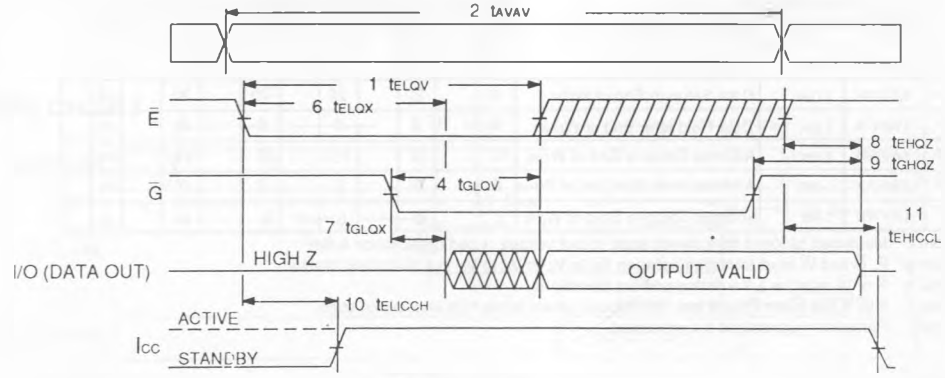
No	SYMBOL Standard	SYMBOL Alternate	PARAMETER	IMS 1624-25 MIN	IMS 1624-25 MAX	IMS 1624-30 MIN	IMS 1624-30 MAX	IMS 1624-35 MIN	IMS 1624-35 MAX	IMS 1624-45 MIN	IMS 1624-45 MAX	IMS 1624-55 MIN	IMS 1624-55 MAX	UNITS	NOTES
1	tELQV	tACS	Chip Enable Access Time		25		30		35		45		55	ns	
2	tAVAV	tRC	Read Cycle Time	25		30		35		45		55		ns	c
3	tAVQV	tAA	Address Access Time		25		30		35		45		55	ns	d
4	tGLQV	tTOE	O/P Enable Access Time		15		15		20		20		25	ns	
5	tAXQX	tOH	O/P Hold After Address Change	5		5		5		5		5		ns	j
6	tELQX	tLZ	O/P Enable to O/P Active	5		5		5		5		5		ns	j
7	tGLQX	tOLZ	O/P Enable to O/P Active	0		0		0		0		0		ns	j
8	tEHQZ	tHZ	Chip Disable to Output Inactive	0	15	0	15	0	15	0	20	0	25	ns	f, j
9	tGHQZ	tOHZ	O/P Disable to Output Inactive	0	15	0	15	0	15	0	20	0	25	ns	f, j
10	tELICCH	tPU	Chip Enable to Power Up	0		0		0		0		0		ns	j
11	tEHICCL	tPD	Chip Disable to Power Down		25		30		35		45		55	ns	j
		tT	Input Rise and Fall Times		50		50		50		50		50	ns	e, j

Note c: For READ CYCLE 1 & 2, $\overline{W}$ is high for entire cycle.
Note d: Device is continuously selected; $\overline{E}$ and $\overline{G}$ low.
Note e: Measured between V_{IL} max and V_{IH} min.
Note f: Measured ±200mV from steady state output voltage. Load capacitance is 5pF.
Note g: $\overline{E}$, $\overline{G}$ and $\overline{W}$ must transition between V_{IH} to V_{IL} or V_{IL} to V_{IH} in a monotonic fashion.
Note j: Parameter guaranteed but not tested.

READ CYCLE 1[c,d]



READ CYCLE 2[c]



RECOMMENDED AC OPERATING CONDITIONS ($0°C \leq T_A \leq 70°C$) ($V_{CC} = 5.0V \pm 10\%$)

WRITE CYCLE 1: $\overline{W}$ CONTROLLED[g,h]

No	SYMBOL Standard	SYMBOL Alternate	PARAMETER	IMS 1624-25 MIN	IMS 1624-25 MAX	IMS 1624-30 MIN	IMS 1624-30 MAX	IMS 1624-35 MIN	IMS 1624-35 MAX	IMS 1624-45 MIN	IMS 1624-45 MAX	IMS 1624-55 MIN	IMS 1624-55 MAX	UNITS	NOTES
12	tAVAV	t WC	Write Cycle Time	25		30		35		45		55		ns	
13	tWLWH	t WP	Write Pulse Width	20		20		30		30		40		ns	
14	tELWH	t CW	Chip Enable to End of Write	20		20		30		30		40		ns	
15	tDVWH	t DW	Data Setup to End of Write	13		15		15		20		25		ns	
16	tWHDX	t DH	Data Hold after End of Write	0		0		0		0		0		ns	
17	tAVWH	t AW	Address Setup to End of Write	20		25		30		30		40		ns	
18	tAVWL	t AS	Address Setup to Start of Write	0		0		0		0		0		ns	
19	tWHAX	t WR	Address Hold after End of Write	5		5		5		0		0		ns	
20	tWLQZ	t WZ	Write Enable to Output Disable	0	15	0	15	0	15	0	20	0	25	ns	f,i
21	tWHQX	t OW	O/P Active after end of Write	0		0		0		0		0		ns	j

WRITE CYCLE 2: $\overline{E}$ CONTROLLED[g,h]

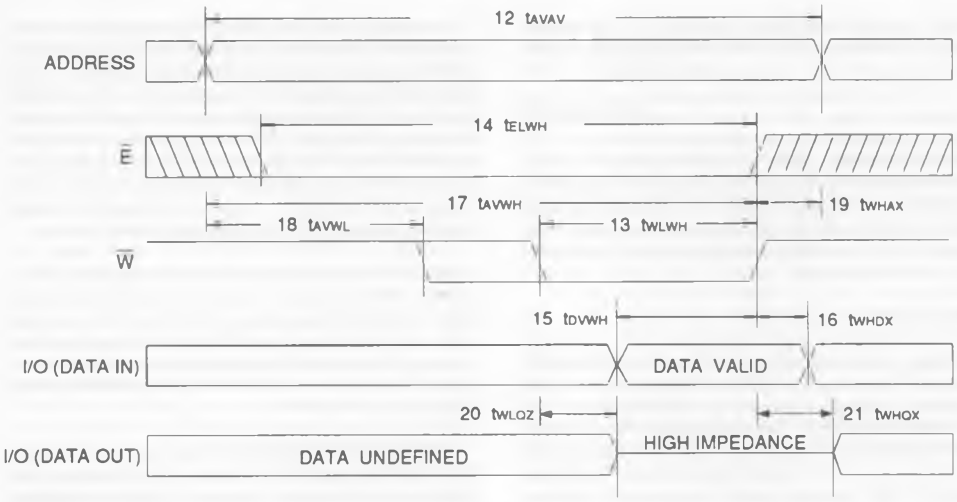
No	SYMBOL Standard	SYMBOL Alternate	PARAMETER	IMS 1624-25 MIN	IMS 1624-25 MAX	IMS 1624-30 MIN	IMS 1624-30 MAX	IMS 1624-35 MIN	IMS 1624-35 MAX	IMS 1624-45 MIN	IMS 1624-45 MAX	IMS 1624-55 MIN	IMS 1624-55 MAX	UNITS	NOTES
22	tAVAV	t WC	Write Cycle Time	25		30		35		45		55		ns	
23	tWLEH	t WP	Write Pulse Width	20		20		30		30		40		ns	
24	tELEH	t CW	Chip Enable to End of Write	20		20		30		30		40		ns	
25	tDVEH	t DW	Data Setup to End of Write	13		15		15		20		25		ns	
26	tEHDX	t DH	Data Hold after End of Write	0		0		0		0		0		ns	
27	tAVEH	t AW	Address Setup to End of Write	20		25		30		30		40		ns	
28	tEHAX	t WR	Address Hold after End of Write	5		5		5		0		0		ns	
29	tAVEL	t AS	Address Setup to Start of Write	0		0		0		0		0		ns	
30	tWLQZ	t WZ	Write Enable to Output Disable	0	15	0	15	0	15	0	20	0	25	ns	f,j

WRITE CYCLE 3: Fast Write, Outputs Disabled[g,h]

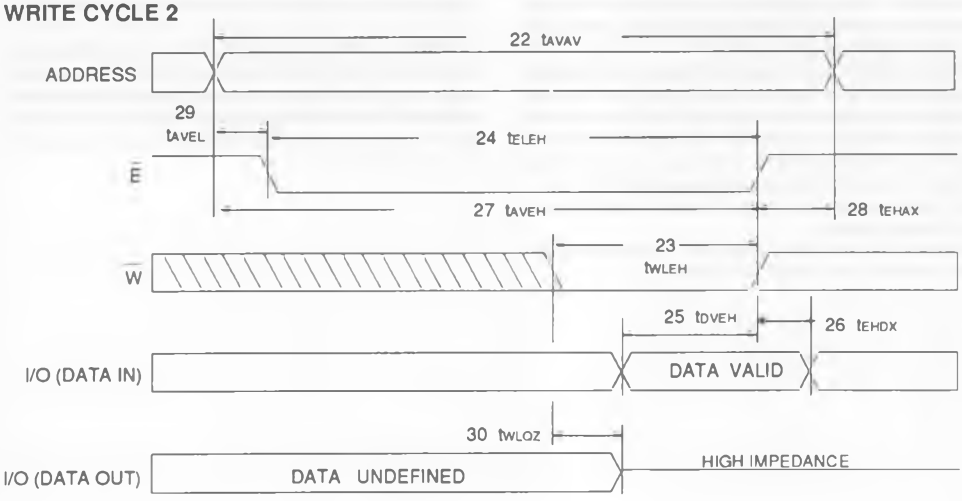
No	SYMBOL Standard	SYMBOL Alternate	PARAMETER	IMS 1624-25 MIN	IMS 1624-25 MAX	IMS 1624-30 MIN	IMS 1624-30 MAX	IMS 1624-35 MIN	IMS 1624-35 MAX	IMS 1624-45 MIN	IMS 1624-45 MAX	IMS 1624-55 MIN	IMS 1624-55 MAX	UNITS	NOTES
31	tAVAV	t WC	Write Cycle Time	18		20		20		25		30		ns	
32	tWLWH	t WP	Write Pulse Width	13		15		15		20		25		ns	
33	tDVWH	t DW	Data Setup to End of Write	18		20		20		25		30		ns	
34	tWHDX	t DH	Data Hold after End of Write	0		0		0		0		0		ns	
35	tAVWH	t AW	Address Setup to End of Write	12		15		15		20		25		ns	
36	tWHAX	t WR	Address Hold after End of Write	5		5		5		0		0		ns	
37	tAVWL	t AS	Address Setup to Start of Write	0		0		0		0		0		ns	

Note f: Measured ±200mV from steady state output voltage. Load capacitance is 5pF.
Note g: $\overline{E}$, $\overline{G}$ and $\overline{W}$ must transition between V_{IH} to V_{IL} or V_{IL} to V_{IH} in a monotonic fashion.
Note h: $\overline{E}$ or $\overline{W}$ must be $\geq V_{IH}$ during address transitions.
Note i: If $\overline{W}$ is low when $\overline{E}$ goes low, the outputs remain in the high impedance state.
Note j: Parameter guaranteed but not tested.

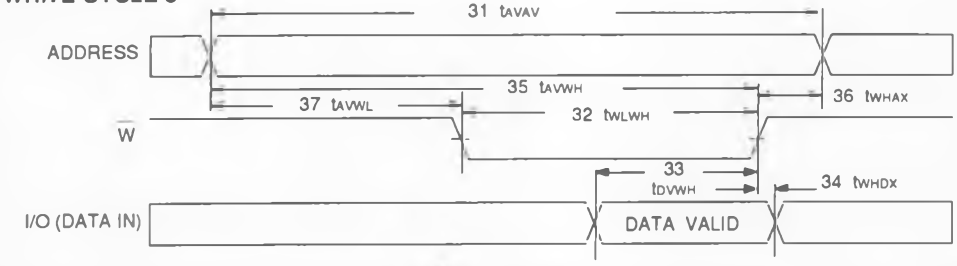
WRITE CYCLE 1



WRITE CYCLE 2



WRITE CYCLE 3



DEVICE OPERATION

The IMS1624 has three control inputs, Chip Enable (/E), Output Enable (/G) and Write Enable (/W), 14 address inputs (A0 -A13), and four Data I/O pins.

The /E input controls device selection as well as active and standby modes. With /E low, the device is selected and the 14 address inputs are decoded to select one 4-bit word out of 16,384. Read and Write operations on the memory cells are controlled by the /W and /G inputs. With /E high, the device is deselected, the outputs are disabled and the power consumption is reduced to less than one-fourth of the active mode power with TTL levels and even lower with CMOS levels.

READ CYCLE

A read cycle is defined as /W $\geq$ V_{IH} min with /E and /G $\leq$ V_{IL} max. Read access time is measured from the latter of either /E or /G going low or from valid address.

The READ CYCLE 1 waveform shows a read access that is initiated by a change in the address inputs while /E and /G are low. The outputs remain active throughout READ CYCLE 1 and are valid at the specified address access time. The address inputs may change at access time and long as /E and /G remain low, the cycle time is equal to the address access time.

The READ CYCLE 2 waveform shows a read access that is initiated bythe latter of /E or /G going low. As long as address is stable when /E goes low, valid data is at the outputs at thelatter of specified Chip Enable Access or Output Enable Access times. If address is not valid when /E goes low, the timing is as specified in READ CYCLE 1. Chip Enable access time is not affected by the duration of the deselect interval.

Since /G controls the output buffers, /G is required to be low in order for the outputs to be active.

WRITE CYCLE

The write cycle of the IMS1624 is initiated by the latter of /E or /W to transition from a high to a low. In the case of /W falling last, the output buffers are turned on t_{ELOX} after the falling edge of /E if /G is already low (just as in a read cycle). The output buffers are then turned off within t_{WLOZ} of the falling edge of /W. During this interval it is possible to have bus contention between devices with common I/O configurations. Therefore input data should not be active until t_{WLOZ}. To aviod bus contention, the /G input can be held high throughout the write operation.

WRITE CYCLE 1 waveform shows a write cycle terminated by /W going high. Data set-up and hold times are referenced to the rising edge of /W. When /W goes high at the end of the cycle with /E active, the output of the memory becomes active (if /G is low). The data from the memory will be the same as the input data unless the input data or address changes.

WRITE CYCLE 2 waveform shows a write cycle terminated by /E going high. Data set-up and hold times are referenced to the rising edge of /E. With /E high the outputs remain in the high impedance state.

WRITE CYCLE 3 waveform shows a write cycle controlled by /W, with /G high and /E low throughout the cycle. As the outputs will not become active during this operation, maximum data bandwidth is provided by allowing very short write cycles and eliminating any bus contention considerations.

POWER DISTRIBUTION

The recommended power distribution scheme combines proper power trace layout and placement of decoupling capacitors to maintain the operating margins of the IMS1624. The impedance in the decoupling path from the power pin through the decoupling capacitor to the ground pin should be kept to a minimum. The impedance of this path is determined by the series impedance of the power line inductance and the inductance and reactance of the decoupling capacitor.

Current transients associated with the operation of any high speed device have very high frequency components, so line inductance is the dominating factor. To reduce the line inductance, the power trace and ground trace should be gridded or provided by separate power planes. The decoupling capacitor supplies energy for high frequency current transients and should be located as close to the devices with as short lead length as possible. The high frequency decoupling capacitor should have a value of 0.1 microfarad and be placed between each row of devices in the array. A larger tantalum capacitor of a sufficient value to eliminate low frequency ripple, should be placed near the memory board edge connection where the power traces meet the backplane power distribution system. These larger capacitors provide bulk energy storage to prevent voltage drop due to the main supply being located off the memory board and at the end of a long inductive path. The ground grid of the memory array should extend to the TTL driver periphery circuit area This will provide a solid ground reference for the TTL drivers and prevent loss of operating margin of the drivers due to differential ground noise.

TERMINATION

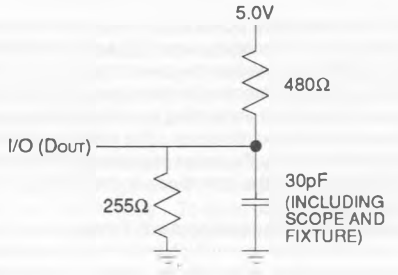
Trace lines on a memory board in the array look to TTL driver signals like low impedance, unterminated transmission lines. In order to reduce or eliminate the reflections of the TTL signals propagating down the lines, especially low going TTL signals, line termination is recommended. The termination may be either series or parallel.

The recommended technique is to use series termination. The series termination technique has the advantage of drawing no DC current and using a minimum number of components. This is accomplished by placing a series resistor in the signal line at the output of the TTL driver to dampen the reflection on the line. The resistor should be placed as close to the driver package as is practical. The line should be kept short by placing the driver-termination combination close to the memory array.

Some experimentation will have to be done to find the proper value to use for the series termination to minimize reflections, but generally a series resistor in the 10 to 33 ohm range will be required. Because each design will result in a different signal impedance, a resistor of predetermined value may not properly match the signal path impedance. The proper value of resistance should therefore be selected empirically.

Type	Package	Lead finish
A	Formed flat-pack	gold
B	Formed flat-pack	solder
C	LCC	gold
D	Cerdip	solder
E	Small outline, J-bend	solder
G	PGA	gold
H	Small outline, Gull wing	solder
J	PLCC, J-bend	solder
K	Sidebraze ceramic DIP	solder
N	Ceramic LCC	solder
P	Plastic DIP	solder
S	Sidebraze ceramic DIP	gold
T	(Skinny) Flat-pack	solder
W	Ceramic LCC	gold
Y	(Skinny) Flat-pack	gold

FIGURE 1. OUTPUT LOAD

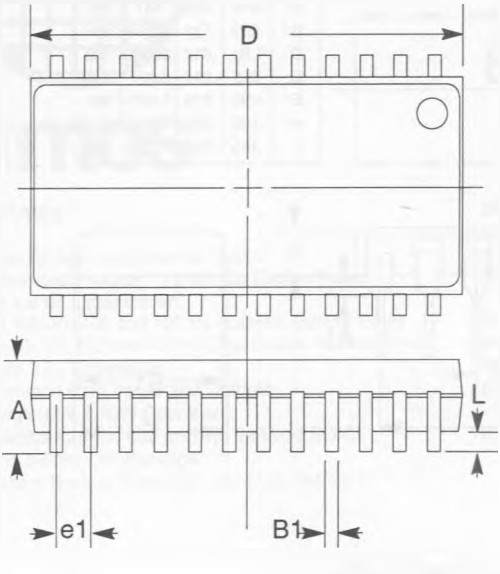


ORDERING INFORMATION

DEVICE	SPEED	PACKAGE	PART NUMBER
IMS1624	25ns	PLASTIC DIP	IMS1624P-25
	25ns	CERAMIC DIP	IMS1624S-25
	25ns	CERAMIC LCC	IMS1624W-25
	25ns	PLASTIC SOJ	IMS1624E-25
	30ns	PLASTIC DIP	IMS1624P-30
	30ns	CERAMIC DIP	IMS1624S-30
	30ns	CERAMIC LCC	IMS1624W-30
	30ns	PLASTIC SOJ	IMS1624E-30
	35ns	PLASTIC DIP	IMS1624P-35
	35ns	CERAMIC DIP	IMS1624S-35
	35ns	CERAMIC LCC	IMS1624W-35
	35ns	PLASTIC SOJ	IMS1624E-35
	45ns	PLASTIC DIP	IMS1624P-45
	45ns	CERAMIC DIP	IMS1624S-45
	45ns	CERAMIC LCC	IMS1624W-45
	45ns	PLASTIC SOJ	IMS1624E-45
	55ns	PLASTIC DIP	IMS1624P-55
	55ns	CERAMIC DIP	IMS1624S-55
	55ns	CERAMIC LCC	IMS1624W-55
	55ns	PLASTIC SOJ	IMS1624E-55

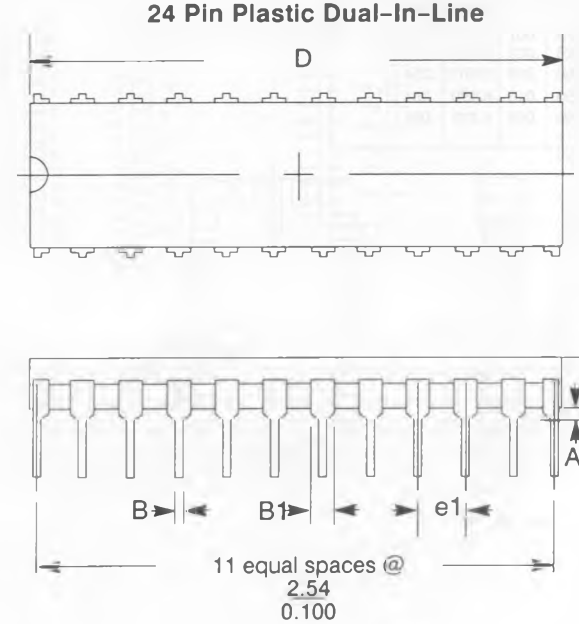
PACKAGING INFORMATION

24 Pin Plastic J Leaded SOJ



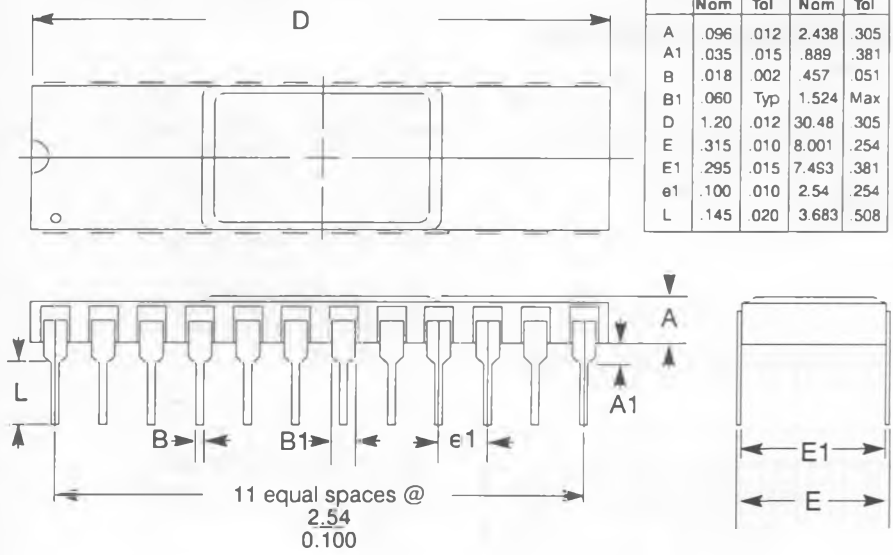
Dim	Inches		mm		Notes
	Min	Max	Min	Max	
A	.120	.140	3.048	3.556	
B1	.014	.019	.356	.483	
C	.010		.254		
D	.602	.612	15.291	15.545	
E	.335	.347	8.509	8.814	
E1	.292	.299	7.417	7.595	
e1	.050	.050	1.270	1.270	
eA	.262	.272	6.655	6.909	
L	.028	.036	.711	.914	

24 Pin Plastic Dual-In-Line



Dim	Inches		mm	
	Nom	Tol	Nom	Tol
A	.165		4.551	
A1	.045	.025	1.143	.635
B	.018	.006	0.457	.152
B1	.060	.003	1.524	127
D	1.160	.002	29.46	05
E	.300	.003	7.620	.076
e1	.100	.010	2.54	.254
eA	.325	.010	8.255	.254

24 Pin Ceramic Dual-In-Line



Dim	Inches		mm	
	Nom	Tol	Nom	Tol
A	.096	.012	2.438	.305
A1	.035	.015	.889	.381
B	.018	.002	.457	.051
B1	.060	Typ	1.524	Max
D	1.20	.012	30.48	.305
E	.315	.010	8.001	.254
E1	.295	.015	7.493	.381
e1	.100	.010	2.54	.254
L	.145	020	3.683	.508

28 Pin Leadless Chip Carrier

Dim	Inches		mm		Notes
	Nom	Tol	Nom	Tol	
A	.071	.007	1.803	.178	
B1	.025	.003	635	.076	
D	.550	.010	13.970	.254	
E	.350	.010	8.890	254	
e1	.050	.002	1.270	051