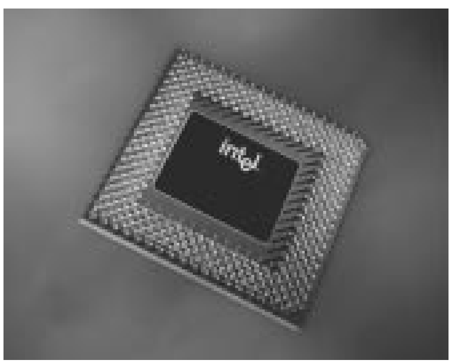
Intel® Celeron™ Processor

Datasheet

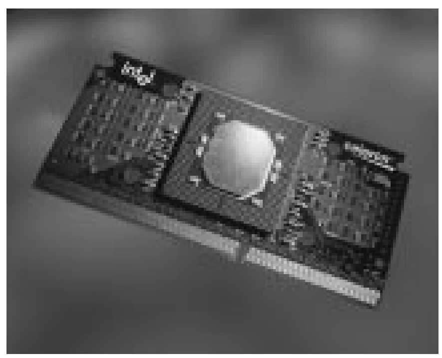
Product Features

- Available at 433 MHz, 400 MHz, 366 MHz, 333 MHz, and 300A MHz core frequencies with 128 KB level-two cache; 300 MHz and 266 MHz core frequencies without level-two cache.
- Binary compatible with applications running on previous members of the Intel microprocessor line
- Dynamic execution microarchitecture
- Operates on a 66 MHz, transaction-oriented system bus
- Intel's specifically designed processor for Value PC systems: based on the same P6 microarchitecture used in the Pentium® II processor with the capabilities of MMX™ technology
- Power Management capabilities
- Optimized for 32-bit applications running on advanced 32-bit operating systems
- Uses cost-effective packaging technology
  - —Single Edge Processor (S.E.P.) Package to maintain compatibility with SC242
  - —Plastic Pin Grid Array (PPGA) package
- Integrated high performance 32 KB instruction and data, nonblocking, level-one cache: separate 16 KB instruction and 16 KB data caches
- Integrated thermal diode

The Intel® Celeron™ processor is designed for Value PC desktops, and is binary compatible with previous generation Intel architecture processors. The Intel® Celeron processor provides good performance for applications running on advanced operating systems such as Windows* 95/98, Windows* NT, and UNIX*. This is achieved by integrating the best attributes of Intel processors—the dynamic execution performance of the P6 microarchitecture plus the capabilities of MMX™ technology—bringing a balanced level of performance to the Value PC market segment. The Intel® Celeron processor offers the dependability you expect from Intel at an exceptional value. Systems based on Intel® Celeron processors also include the latest features to simplify system management and lower the cost of ownership for small business and home environments.



PPGA Package



S.E.P. Package

Order Number: 243658-007
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1.0 Introduction

The Intel® Celeron™ processor is the next addition to the P6 microarchitecture processor product family. The Intel Celeron processor, like the Intel® Pentium® Pro and Intel® Pentium® II processor, features a Dynamic Execution microarchitecture and also executes MMX technology instructions for enhanced media and communication performance. The Intel processor also utilizes multiple low-power states such as AutoHALT, Stop-Grant, Sleep, and Deep Sleep to conserve power during idle times.

The Intel Celeron processor is capable of running today’s most common PC applications and is intended for Value PC systems. Memory is also cacheable up to 4 GB of addressable memory space. Support for multiprocessor-based systems is not provided with the Intel Celeron processor. The Pentium II processor should be used for multiprocessor system designs.

To be cost-effective at both the processor and system level, the Intel Celeron processor will utilize two cost-effective packaging technologies. They are the S.E.P. (Single-Edge Processor) Package and PPGA (Plastic Pin Grid Array) package.

The S.E.P. Package's design lacks the thermal plate, cover, and latch arms of the Single Edge Contact (S.E.C.) cartridge currently used on the Pentium II processor. Different heatsink attachment and processor retention solutions are required to support this packaging technology, with design emphasis centered on cost-effectiveness. This design and associated heatsink attachment and retention solutions provide a low-cost medium for future Intel Celeron processors targeted for cost-effective systems.

Note: This document describes the Intel® Celeron™ processor for both the PPGA package and the S.E.P. Package versions. Unless otherwise specificed, the information in this document applies to both versions.

1.1 Terminology

In this document, a ‘#’ symbol after a signal name refers to an active low signal. This means that a signal is in the active state (based on the name of the signal) when driven to a low level. For example, when FLUSH# is low, a flush has been requested. When NMI is high, a nonmaskable interrupt has occurred. In the case of signals where the name does not imply an active state but describes part of a binary sequence (such as *address* or *data*), the ‘#’ symbol implies that the signal is inverted. For example, D[3:0] = ‘HLHL’ refers to a hex ‘A’, and D#[3:0] = ‘LHLH’ also refers to a hex ‘A’ (H= High logic level, L= Low logic level).

The term “system bus” refers to the interface between the processor, system core logic (a.k.a. the AGPset components), and other bus agents. The system bus is an interface to the processor, memory, and I/O.

1.1.1 Package Terminology

The following terms are used often in this document and are explained here for clarification:

- **Intel® Celeron™ processor**—The entire product including internal components, substrate and core.
- **Processor substrate**—The structure on which components are mounted (with or without components attached).
- **Processor core**—The processor's execution engine.
- **S.E.P. Package**—Single-Edge Processor Package, differs from the S.E.C. Cartridge as this processor has no external plastic cover, thermal plate, or latch arms. The S.E.P. Package also has high frequency decoupling capacitors and AGTL+ termination resistors on its substrate, while PPGA packages do not.
- **PPGA package—**Plastic Pin Grid Array package.

Additional terms referred to in this and other related documentation:

- **SC242**—The 242-contact slot connector that the S.E.P. Package plugs into.
- **370-pin socket (PGA370)—**The zero insertion force (ZIF) socket which the PPGA package plugs into.
- **Retention mechanism**—A mechanical assembly which holds the package in the SC242 connector.

1.2 References[1,2]

The reader of this specification should also be familiar with material and concepts presented in the following documents:

- Intel® Celeron™ Processor Support Component Suppliers (http://developer.intel.com/design/celeron/componets/)
- AP-485, *Intel Processor Identification and the CPUID Instruction* (Order Number 241618)
- AP-585, *Pentium® II Processor AGTL+ Guidelines* (Order Number 243330)
- AP-586, *Pentium® II Processor Thermal Design Guidelines* (Order Number 243331)
- AP-587, *Pentium® II Processor Power Distribution Guidelines* (Order Number 243332)
- AP-589, *Design for EMI* (Order Number 243334)
- *Pentium® II Processor at 233, 266, 300, and 333 MHz Datasheet* (Order Number 243335)
- *Pentium® II Processor at 350, 400, and 450 MHz Datasheet* (Order Number 243657)
- *Intel® Celeron™ Processor Specification Update* (Order Number 243337)
- *SC242 Connector Design Guidelines* (Order Number 243397)
- *Pentium® II Processor Developer's Manual* (Order Number 243502)
- *370-Pin Socket (PGA370) Design Guidelines* (Order Number 244410)
- *Intel Architecture Software Developer's Manual* (Order Number 243193)
  - *Volume I: Basic Architecture* (Order Number 243190)
  - *Volume II: Instruction Set Reference* (Order Number 243191)
  - *Volume III: System Programming Guide* (Order Number 243192)
- *Pentium® II Processor I/O Buffer Models*, Quad XTK Format (Electronic Form)
- *Intel® 440EX AGPset Design Guide* (Order Number 290637)

- *Intel® Celeron™ Processor with the Intel® 440LX AGPset Design Guide* (Order Number 245088)
- *Intel® 440BX AGPset Design Guide* (Order Number 290634)
- *Intel® Celeron™ Processor with the Intel® 440ZX-66 AGPset Design Guide* (Order Number 245126)

Notes:

1. This reference material can be found on the Intel Developer’s Website located at: http://developer.intel.com
2. For a complete listing of the Intel® Celeron™ processor reference material, refer to the Intel Developer’s Website when this processor is formerly launched. The website is located at: http://developer.intel.com/design/celeron/

2.0 Electrical Specifications

2.1 The Intel® Celeron™ Processor System Bus and V_{REF}

Intel® Celeron processor signals use a variation of the low voltage Gunning Transceiver Logic (GTL) signaling technology. The Intel Celeron processor system bus specification is similar to the GTL specification, but has been enhanced to provide larger noise margins and reduced ringing. The improvements are accomplished by increasing the termination voltage level and controlling the edge rates. Because this specification is different from the standard GTL specification, it is referred to as Assisted Gunning Transceiver Logic (AGTL+) in this document.

The Intel® Celeron processor varies from the Pentium Pro processor in its output buffer implementation. The buffers that drive the system bus signals on the Intel® Celeron processor are actively driven to $V_{CC_{CORE}}$ for one clock cycle after the low-to-high transition. This improves rise times and reduces overshoot. These signals should still be considered open-drain and require termination to a supply that provides the logic-high signal level.

The AGTL+ inputs use differential receivers which require a reference signal (V_{REF}). V_{REF} is used by the receivers to determine if a signal is a logic-high or a logic-low, and is provided to the processor core by either the processor substrate (S.E.P. Package) or the motherboard (PPGA package). Local V_{REF} copies should be generated on the motherboard for all other devices on the AGTL+ system bus.

Termination is used to pull the bus up to the high voltage level and to control reflections on the transmission line. The processor may contain termination resistors (S.E.P. Package only) that provide termination for one end of the Intel Celeron processor system bus. Otherwise, this termination must exist on the motherboard.

Intel specifications assume a resistor resides at the ends of each signal trace (dual-ended termination) to ensure adequate AGTL+ signal quality; see Table 7 for the bus termination voltage specifications for AGTL+ and the *Pentium® II Processor Developer's Manual* (Order Number 243502) for the AGTL+ bus specification. Solutions do exist for using a single resistor at the processor end of each AGTL+ signal trace (single-ended termination) as well, though solution space is affected.

The AGTL+ bus depends on incident wave switching. Therefore timing calculations for AGTL+ signals are based on motherboard **flight time** as opposed to capacitive deratings. Analog signal simulation of the Intel Celeron processor system bus, including trace lengths, is highly recommended when designing a system. See the *Pentium® II Processor AGTL+ Layout Guidelines* and the *Pentium® II Processor I/O Buffer Models, Quad Format* (Electronic Form) for details.

2.2 Clock Control and Low Power States

Intel® Celeron processors allow the use of AutoHALT, Stop-Grant, Sleep, and Deep Sleep states to reduce power consumption by stopping the clock to internal sections of the processor, depending on each particular state. See Figure 1 for a visual representation of the Intel Celeron processor low power states.

For the processor to fully realize the low current consumption of the Stop-Grant, Sleep, and Deep Sleep states, a Model Specific Register (MSR) bit must be set. For the MSR at 02AH (Hex), bit 26 must be set to a ‘1’ (this is the power on default setting) for the processor to stop all internal clocks during these modes. For more information, see the *Pentium® II Processor Developer's Manual* (Order Number 243502).

2.2.1 Normal State—State 1

This is the normal operating state for the processor.

2.2.2 AutoHALT Power Down State—State 2

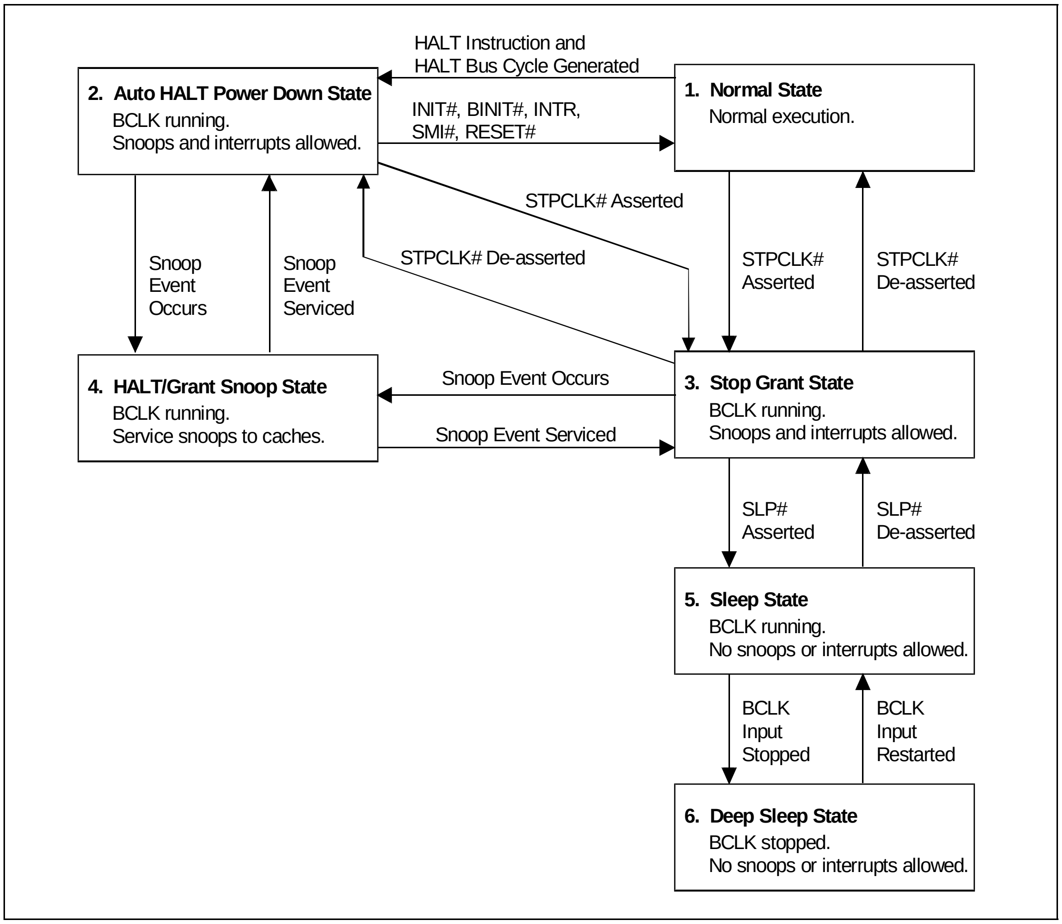
AutoHALT is a low power state entered when the processor executes the HALT instruction. The processor will transition to the Normal state upon the occurrence of SMI#, BINIT#, INIT#, or LINT[1:0] (NMI, INTR). RESET# will cause the processor to immediately initialize itself.

The return from a System Management Interrupt (SMI) handler can be to either Normal Mode or the AutoHALT Power Down state. See the *Intel Architecture Software Developer's Manual, Volume III: System Programmer's Guide* (Order Number 243192) for more information.

FLUSH# will be serviced during the AutoHALT state, and the processor will return to the AutoHALT state.

The system can generate a STPCLK# while the processor is in the AutoHALT Power Down state. When the system deasserts the STPCLK# interrupt, the processor will return execution to the HALT state.

Figure 1. Clock Control State Machine



2.2.3 Stop-Grant State—State 3

The Stop-Grant state on the processor is entered when the STPCLK# signal is asserted.

Since the AGTL+ signal pins receive power from the system bus, these pins should not be driven (allowing the level to return to V_{TT}) for minimum power drawn by the termination resistors in this state. In addition, all other input pins on the system bus should be driven to the inactive state.

BINIT# will not be serviced while the processor is in Stop-Grant state. The event will be latched and can be serviced by software upon exit from Stop-Grant state.

FLUSH# will not be serviced during Stop-Grant state.

RESET# will cause the processor to immediately initialize itself, but the processor will stay in Stop-Grant state. A transition back to the Normal state will occur with the deassertion of the STPCLK# signal.

A transition to the HALT/Grant Snoop state will occur when the processor detects a snoop on the system bus (see Section 2.2.4). A transition to the Sleep state (see Section 2.2.4) will occur with the assertion of the SLP# signal.

While in the Stop-Grant State, SMI#, INIT#, and LINT[1:0] will be latched by the processor, and only serviced when the processor returns to the Normal State. Only one occurrence of each event will be recognized upon return to the Normal state.

2.2.4 HALT/Grant Snoop State—State 4

The processor will respond to snoop transactions on the Intel® Celeron processor system bus while in Stop-Grant state or in AutoHALT Power Down state. During a snoop transaction, the processor enters the HALT/Grant Snoop state. The processor will stay in this state until the snoop on the Intel Celeron processor system bus has been serviced (whether by the processor or another agent on the Intel Celeron processor system bus). After the snoop is serviced, the processor will return to the Stop-Grant state or AutoHALT Power Down state, as appropriate.

2.2.5 Sleep State—State 5

The Sleep state is a very low power state in which the processor maintains its context, maintains the phase-locked loop (PLL), and has stopped all internal clocks. The Sleep state can only be entered from Stop-Grant state. Once in the Stop-Grant state, the SLP# pin can be asserted, causing the processor to enter the Sleep state. The SLP# pin is not recognized in the Normal or AutoHALT states.

Snoop events that occur while in Sleep State or during a transition into or out of Sleep state will cause unpredictable behavior.

In the Sleep state, the processor is incapable of responding to snoop transactions or latching interrupt signals. No transitions or assertions of signals (with the exception of SLP# or RESET#) are allowed on the system bus while the processor is in Sleep state. Any transition on an input signal before the processor has returned to Stop-Grant state will result in unpredictable behavior.

If RESET# is driven active while the processor is in the Sleep state, and held active as specified in the RESET# pin specification, then the processor will reset itself, ignoring the transition through Stop-Grant State. If RESET# is driven active while the processor is in the Sleep State, the SLP# and STPCLK# signals should be deasserted immediately after RESET# is asserted to ensure the processor correctly executes the Reset sequence.

While in the Sleep state, the processor is capable of entering its lowest power state, the Deep Sleep state, by stopping the BCLK input. (See Section 2.2.6.) Once in the Sleep state, the SLP# pin can be deasserted if another asynchronous system bus event occurs. The SLP# pin has a minimum assertion of one BCLK period.

2.2.6 Deep Sleep State—State 6

The Deep Sleep state is the lowest power state the processor can enter while maintaining context. The Deep Sleep state is entered by stopping the BCLK input (after the Sleep state was entered from the assertion of the SLP# pin). The processor is in Deep Sleep state immediately after BLCK is stopped. It is recommended that the BLCK input be held low during the Deep Sleep State. Stopping of the BCLK input lowers the overall current consumption to leakage levels.

To re-enter the Sleep state, the BLCK input must be restarted. A period of 1 ms (to allow for PLL stabilization) must occur before the processor can be considered to be in the Sleep State. Once in the Sleep state, the SLP# pin can be deasserted to re-enter the Stop-Grant state.

While in Deep Sleep state, the processor is incapable of responding to snoop transactions or latching interrupt signals. No transitions or assertions of signals are allowed on the system bus while the processor is in Deep Sleep state. Any transition on an input signal before the processor has returned to Stop-Grant state will result in unpredictable behavior.

2.2.7 Clock Control

When the processor is in the Sleep or Deep Sleep states, it will not respond to interrupts or snoop transactions. PICCLK should not be removed during the AutoHALT Power Down or Stop-Grant states. PICCLK can be removed during the Sleep or Deep Sleep states. When transitioning from the Deep Sleep state to the Sleep state, PICCLK must be restarted with BCLK.

2.3 Intel® Celeron™ Processor Power and Ground Pins

There are five pins defined on the S.E.P. Package for voltage identification (VID) and there are four pins on the PPGA package. These pins specify the voltage required by the processor core. These have been added to cleanly support voltage specification variations on current and future Intel® Celeron processors.

For clean on-chip power distribution, Intel Celeron processors in the S.E.P. Package have 27 V_{CC} (power) and 30 V_{SS} (ground) inputs. The 27 V_{CC} pins are further divided to provide the different voltage levels to the components. $V_{CC_{CORE}}$ inputs for the processor core account for 19 of the V_{CC} pins, while 4 V_{TT} inputs (1.5 V) are used to provide a AGTL+ termination voltage to the processor. For only the S.E.P. Package, one V_{CC_5} pin is provided for Voltage Transient Tools. V_{CC_5} and $V_{CC_{CORE}}$ must remain electrically separated from each other.

The PPGA package has more power (88) and ground (80) pins than the S.E.P. Package. Of the power pins, 77 are used for the processor core ($V_{CC_{CORE}}$) and 8 are used as a AGTL+ reference voltage (V_{REF}). The other 3 power pins are $V_{CC_{1.5}}$, $V_{CC_{2.5}}$ and $V_{CC_{CMOS}}$ and are used for future processor compatibility.

The $V_{CC_{CMOS}}$ pin is provided as a feature for future processor support in a flexible design. In such a design, the $V_{CC_{CMOS}}$ pin is used to provide the CMOS voltage for use by the platform. Additionally, 2.5 V must be provided to the $V_{CC_{2.5}}$ input and 1.5 V must be provided to the $V_{CC_{1.5}}$ input. The processor routes the CMOS voltage level through the package that it is compatible with. For example, future processors requiring 1.5 V CMOS voltage levels route 1.5 V to the $V_{CC_{CMOS}}$ output.

Each power signal, regardless of package, must meet the specifications stated in Table 4. In addition, all $V_{CC_{CORE}}$ pins must be connected to a voltage island while all V_{SS} pins have to connect to a system ground plane.

2.4 Intel® Celeron™ Processor Decoupling

Due to the large number of transistors and high internal clock speeds, the processor is capable of generating large average current swings between low and full power states. This causes voltages on power planes to sag below their nominal values if bulk decoupling is not adequate. Care must be taken in the board design to ensure that the voltage provided to the processor remains within the specifications listed in Table 4, failure to do so can result in timing violations or a reduced lifetime of the component.

2.4.1 Intel® Celeron™ Processor System Bus AGTL+ Decoupling

The S.E.P. Package contains high frequency decoupling capacitance on the processor substrate, where the PPGA package does not. Therefore, Intel® Celeron™ processors in the PPGA package require high frequency decoupling on the system motherboard. Bulk decoupling must be provided on the motherboard for proper AGTL+ bus operation for both packages. See AP-585, *Pentium® II Processor AGTL+ Guidelines* (Order Number 243330), AP-587, *Pentium® II Processor Power Distribution Guidelines* (Order Number 243332), and the *Pentium® II Processor Developer's Manual* (Order Number 243502) for more information.

2.5 Voltage Identification

The processor's voltage identification (VID) pins can be used to automatically select the $V_{CC_{CORE}}$ voltage from a compatible voltage regulator. There are five VID pins (VID[4:0]) on the S.E.P. Package, while there are only four (VID[3:0]) on the PPGA package. This is because there are no Intel® Celeron™ processors in the PPGA package that require more than 2.05 V (see Table 1).

VID pins are not signals, but rather are an open or short circuit to V_{SS} on the processor. The combination of opens and shorts defines the processor core's required voltage. The VID pins also allow for compatibility with current and future Intel Celeron processors.

Note that the '11111' (all opens) ID can be used to detect the absence of a processor core in a given slot (S.E.P. Package only), as long as the power supply used does not affect the VID signals. Detection logic and pull-ups should not affect VID inputs at the power source (see Section 7.0).

External logic monitoring the VID signals or the voltage regulator may require the VID pins to be pulled-up. If this is the case, the VID pins should be pulled up to a TTL-compatible level with external resistors to the power source of the regulator.

The power source chosen must be guaranteed to be stable whenever the voltage regulator's supply is stable. This will prevent the possibility of the processor supply going above the specified $V_{CC_{CORE}}$ in the event of a failure in the supply for the VID lines. In the case of a DC-to-DC converter, this can be accomplished by using the input voltage to the converter for the VID line pull-ups. In addition, the power supply must supply the requested voltage or disable itself.

Table 1. Voltage Identification Definition [1, 2, 3, 5]

Processor Pins					
VID4 (S.E.P.P. Only)	VID3	VID2	VID1	VID0	$V_{CC_{CORE}}$
0	0	0	1	1	1.90
0	0	0	1	0	1.95
0	0	0	0	1	2.00[3]
0	0	0	0	0	2.05
1	1	1	1	1	No Core
1	1	1	1	0	2.1

NOTES:
1. 0 = Processor pin connected to V_{SS}.
2. 1 = Open on processor; may be pulled up to TTL V_{IH} on motherboard.
3. The Intel® Celeron™ processor core will be powered off 2.0 V.
4. VID4 applies only to the S.E.P. Package. VID[3:0] applies to both S.E.P. and PPGA packages.
5. For PPGA, only the shaded area applies.

2.6 Intel® Celeron™ Processor System Bus Unused Pins

All RESERVED pins must remain unconnected. Connection of these pins to $V_{CC_{CORE}}$, V_{SS}, or to any other signal (including each other) can result in component malfunction or incompatibility with future Intel® Celeron™ processor products. See Section 5.0 for a pin listing of the processor and the location of each RESERVED pin.

For Intel Celeron processors in the S.E.P. Package, the TESTHI pin must be at a logic-high level when the core power supply comes up. For more information, please refer to erratum C26 of the *Intel® Celeron™ Processor Specification Update* (Order Number 243748). Also note that the TESTHI signal is not available on Intel Celeron processors in the PPGA package.

PICCLK must be driven with a valid clock input and the PICD[1:0] lines must be pulled-up to 2.5 V even when the APIC will not be used. A separate pull-up resistor must be provided for each PICD line.

For reliable operation, always connect unused inputs or bi-directional signals to their deasserted signal level. The pull-up or pull-down resistor value is system dependent and should be chosen such that the logic-high (V_{IH}) and logic-low (V_{IL}) requirements are met.

For the S.E.P. Package, unused AGTL+ inputs should not be connected as the package substrate has termination resistors. On the other hand, PPGA does not have AGTL+ termination in its package and must have any unused AGTL+ inputs terminated through a pull-up resistor.

For unused CMOS inputs, active-low signals should be connected through a pull-up resistor to meet V_{IH} requirements and active-high signals should be connected through a pull-down resistor to meet V_{IL} requirements. Unused CMOS outputs can be left unconnected. A resistor must be used when tying bi-directional signals to power or ground. For any signal pulled to either power or ground, a resistor will allow for system testability.

2.7 Intel® Celeron™ Processor System Bus Signal Groups

To simplify the following discussion, the Intel® Celeron™ processor system bus signals have been combined into groups by buffer type. **All Intel® Celeron™ processor system bus outputs are open drain** and require a high-level source provided externally by the termination or pull-up resistor.

AGTL+ input signals have differential input buffers, which use V_{REF} as a reference signal. AGTL+ output signals require termination to 1.5 V. In this document, the term "AGTL+ Input" refers to the AGTL+ input group as well as the AGTL+ I/O group when receiving. Similarly, "AGTL+ Output" refers to the AGTL+ output group as well as the AGTL+ I/O group when driving.

EMI pins (S.E.P. Package only) should be connected to motherboard ground and/or to chassis ground through zero ohm (0 Ω) resistors. The zero ohm resistors should be placed in close proximity to the SC242 connector. The path to chassis ground should be short in length and have a low impedance.

The CMOS, Clock, APIC, and TAP inputs can each be driven from ground to 2.5 V. The CMOS, APIC, and TAP outputs are open drain and should be pulled high to 2.5 V. This ensures not only correct operation for current Intel Celeron processors, but compatibility for future Intel Celeron processor products as well.

The groups and the signals contained within each group are shown in Table 2. Refer to Section 7.0 for descriptions of these signals.

Table 2. Intel® Celeron™ Processor System Bus Signal Groups

Group Name	Signals
AGTL+ Input	BPRI#, DEFER#, RESET#, RS[2:0]#, TRDY#
AGTL+ Output	PRDY#
AGTL+ I/O	A[31:3]#, ADS#, BNR#, BP[3:2]#, BPM[1:0]#, BR0#, D[63:0]#, DBSY#, DRDY#, HIT#, HITM#, LOCK#, REQ[4:0]#,
CMOS Input[4]	A20M#, FLUSH#, IGNNE#, INIT#, LINT0/INTR, LINT1/NMI, PREQ#, PWRGOOD[1], SMI#, SLP#[2], STPCLK#
CMOS Output[4]	BSEL[7], FERR#, IERR#, THERMTRIP#[3]
System Bus Clock	BCLK
APIC Clock	PICCLK
APIC I/O[4]	PICD[1:0]
TAP Input[4]	TCK, TDI, TMS, TRST#
TAP Output[4]	TDO
Power/Other[5]	BSEL[6], CPUPRES#[7], EDGTRL[7], EMI[6], PLL[2:1][7], SLOTOCC#[6], THERMDP, THERMDN, $V_{CC1.5}$[7], $V_{CC2.5}$[7], V_{CCL2}[5], V_{CC5}[6], V_{CCCMOS}[7], V_{CCCORE}, $V_{COREDET}$[7], VID[3:0][7], VID[4:0][6], V_{REF}[7:0][7], V_{SS}, V_{TT}[6]

NOTES:
1. See Section 7.0 for information on the PWRGOOD signal.
2. See Section 7.0 for information on the SLP# signal.
3. See Section 7.0 for information on the THERMTRIP# signal.
4. These signals are specified for 2.5 V operation.
5. V_{CCCORE} is the power supply for the processor core.
   VID[4:0] and VID[3:0] are described in Section 2.0.
   V_{TT} is used to terminate the system bus and generate V_{REF} on the processor substrate.
   V_{SS} is system ground.
   V_{CC5} is not connected to the Intel® Celeron™ processor. This supply is used for Voltage Transient Tools.
   SLOTOCC# is described in Section 7.0.
   BSEL is described in Section 2.7.2 and Section 7.0.
   EMI pins are described in Section 7.0.
   V_{CCL2} is a Pentium® II processor reserved signal provided to maintain compatibility with the Pentium® II processor and may be left as a no contect for Intel Celeron processor only designs.
6. Only applies to Intel Celeron processors in the S.E.P. Package.
7. Only applies to Intel Celeron processors in the PPGA package.

2.7.1 Asynchronous Vs. Synchronous for System Bus Signals

All AGTL+ signals are synchronous to BCLK. All of the CMOS, APIC, and TAP signals can be applied asynchronously to BCLK. All APIC signals are synchronous to PICCLK. All TAP signals are synchronous to TCK.

2.7.2 Host Bus Frequency Select Signal (BSEL)

This signal will be asserted a logic low by the Intel® Celeron™ processor to denote 66 MHz system bus operation. On motherboards which support operation at either 66 or 100 MHz, this signal should force the clock synthesizer into 66 MHz operation.

2.8 Test Access Port (TAP) Connection

Due to the voltage levels supported by other components in the Test Access Port (TAP) logic, it is recommended that the Intel® Celeron™ processor be first in the TAP chain and followed by any other components within the system. A translation buffer should be used to connect to the rest of the chain unless one of the other components is capable of accepting a 2.5 V input. Similar considerations must be made for TCK, TMS, and TRST#. Two copies of each signal may be required with each driving a different voltage level.

A Debug Port may be placed at the start and end of the TAP chain with the TDI of the first component coming from the Debug Port and the TDO from the last component going to the Debug Port.

2.9 Maximum Ratings

Table 3 contains the Intel® Celeron™ processor stress ratings only. Functional operation at the absolute maximum and minimum is not implied nor guaranteed. The processor should not receive a clock while subjected to these conditions. Functional operating conditions are given in the AC and DC tables. Extended exposure to the maximum ratings may affect device reliability. Furthermore, although the processor contains protective circuitry to resist damage from static electric discharge, one should always take precautions to avoid high static voltages or electric fields.

Table 3. Intel® Celeron™ Processor Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit	Notes
$T_{STORAGE}$	Processor storage temperature	–40	85	°C	
T_{CASE}	Processor case temperature	5.0	85	°C	
$V_{CC(All)}$	Any processor supply voltage with respect to V_{SS}	–0.5	Operating voltage + 1.0	V	1, 2
$V_{inAGTL+}$	AGTL+ buffer DC input voltage with respect to V_{SS}	–0.3	$V_{CC_{CORE}}$ + 0.7	V	
V_{inCMOS}	CMOS buffer DC input voltage with respect to V_{SS}	–0.3	3.3	V	3
I_{VID}	Max VID pin current		5	mA	
$I_{SLOTOCC}$	Max SLOTOCC# pin current		5	mA	5
Mech Max Edge Fingers[5]	Mechanical integrity of processor edge fingers		50	Insertions/ Extractions	4, 5

NOTES:
1. Operating voltage is the voltage to which the component is designed to operate. See Table 4.
2. This rating applies to the $V_{CC_{CORE}}$, V_{CC_5}, and any input (except as noted below) to the processor.
3. Parameter applies to CMOS, APIC, and TAP bus signal groups only.
4. The electrical and mechanical integrity of the processor edge fingers are specified to last for 50 insertion/extraction cycles.
5. S.E.P. Package Only

2.10 Processor DC Specifications

The processor DC specifications in this section are defined for the Intel® Celeron™ processor. See Section 7.0 for signal definitions and Section 5.0 for signal listings.

Most of the signals on the Intel Celeron processor system bus are in the AGTL+ signal group. These signals are specified to be terminated to 1.5 V. The DC specifications for these signals are listed in Table 5.

To allow connection with other devices, the Clock, CMOS, APIC, and TAP signals are designed to interface at non-AGTL+ levels. The DC specifications for these pins are listed in Table 6.

Table 4 through Table 7 list the DC specifications for Intel Celeron processors operating at 66 MHz Intel Celeron processor system bus frequencies. Specifications are valid only while meeting specifications for case temperature, clock frequency, and input voltages. Care should be taken to read all notes associated with each parameter.

Table 4. Intel® Celeron™ Processor Voltage and Current Specifications [1]

Symbol	Parameter	Core Freq	Min	Typ	Max	Unit	Notes
$V_{CC_{CORE}}$	V_{CC} for processor core			2.00		V	2, 3, 4
V_{REF}	AGTL+ input reference voltage		$^2/_3 V_{TT} - 2\%$		$^2/_3 V_{TT} + 2\%$	V	±2%, 11
$V_{CC_{1.5}}$	V_{CC} for future $V_{CC_{CMOS}}$		1.365	1.50	1.635	V	1.5 ±9%
$V_{CC_{2.5}}$	V_{CC} for $V_{CC_{CMOS}}$		2.375	2.5	2.625	V	2.5 ± 5%
V_{TT}	AGTL+ bus termination voltage		1.365	1.50	1.635	V	1.5 ±9% [5]
Baseboard Tolerance, Static	Processor core voltage static tolerance level at SC242 pins		–0.070		0.100	V	6
Baseboard Tolerance, Transient	Processor core voltage transient tolerance level at SC242 pins		–0.120		0.120	V	6
$V_{CC_{CORE}}$ Tolerance, Static	Processor core voltage static tolerance level at edge fingers		–0.085		0.100	V	7
$V_{CC_{CORE}}$ Tolerance, Transient	Processor core voltage transient tolerance level at edge fingers		–0.140		0.140	V	7
$V_{CC_{CORE}}$ Tolerance, Static	Processor core voltage static tolerance level at processor pins		-0.089		0.100	V	8
$V_{CC_{CORE}}$ Tolerance, Transient	Processor core voltage transient tolerance level at processor pins		-0.144		0.144	V	8
$I_{CC_{CORE}}$	I_{CC} for processor core	266 MHz 300 MHz 300A MHz 333 MHz 366 MHz 400 MHz 433 MHz			8.2 9.3 9.3 10.1 11.2 12.2 12.6	A	9, 10

Table 4. Intel® Celeron™ Processor Voltage and Current Specifications [1]

Symbol	Parameter	Core Freq	Min	Typ	Max	Unit	Notes
I_{VTT}	Termination voltage supply current				2.7	A	11
I_{SGnt}	I_{CC} Stop-Grant for processor core	266 MHz 300 MHz 300A MHz 333 MHz 366 MHz 400 MHz 433 MHz			1.12 1.15 1.15 1.18 1.21 1.25 1.30	A	12
I_{SLP}	I_{CC} Sleep for processor core	266 MHz 300 MHz 300A MHz 333 MHz 366 MHz 400 MHz 433 MHz			0.90 0.94 0.94 0.96 0.97 0.99 1.01	A	
I_{DSLP}	I_{CC} Deep Sleep for processor core				0.80	A	
$dI_{CC_{CORE}}/dt$	Power supply current slew rate				20	A/µs	13, 14, 15
$dI_{CC_{CORE}}/dt$	Power supply current slew rate				240	A/µs	13, 14, 17
$dI_{CC_{VTT}}/dt$	Termination current slew rate				8	A/µs	See Table 7, Table 16, Table 17
V_{CC_5}	5 V supply voltage		4.75	5.00	5.25	V	5 V ±5%, 16
I_{CC_5}	I_{CC} for 5 V supply voltage			1.0		A	16

NOTES:
1. Unless otherwise noted, all specifications in this table apply to all processor frequencies.
2. $V_{CC_{CORE}}$ and $I_{CC_{CORE}}$ supply the processor core.
3. These voltages are targets only. A variable voltage source should exist on systems in the event that a different voltage is required.
4. Use the Typical Voltage specification with the Tolerance specifications to provide correct voltage regulation to the processor.
5. V_{TT} must be held to 1.5 V ± 9%. It is recommended that V_{TT} be held to 1.5 V ± 3% while the Intel® Celeron™ processor system bus is idle. This is measured at the processor edge fingers.
6. These are the tolerance requirements, across a 20 MHz bandwidth, **at the SC242 connector pin on the bottom side of the baseboard.** The requirements at the SC242 connector pins account for voltage drops (and impedance discontinuities) across the connector, processor edge fingers, and to the processor core. $V_{CC_{CORE}}$ must return to within the static voltage specification within 100 µs after a transient event.
7. These are the tolerance requirements, across a 20 MHz bandwidth, **at the processor edge fingers.** The requirements at the processor edge fingers account for voltage drops (and impedance discontinuities) at the processor edge fingers and to the processor core. $V_{CC_{CORE}}$ must return to within the static voltage specification within 100 µs after a transient event.
8. These are the tolerance requirements, across a 20 MHz bandwidth, **at the top of the PPGA package.** $V_{CC_{CORE}}$ must return to within the static voltage specification within 100 µs after a transient event.
9. Max $I_{CC_{CORE}}$ measurements are measured at $V_{CC_{CORE}}$ max voltage ($V_{CC_{CORE\_TYP}}$ + maximum static tolerance), under maximum signal loading conditions.
10. Voltage regulators may be designed with a minimum equivalent internal resistance to ensure that the output voltage, at maximum current output, is no greater than the nominal (i.e., typical) voltage level of $V_{CC_{CORE}}$

(Vcc_{CORE_TYP}). In this case, the maximum current level for the regulator, Icc_{CORE_REG}, can be reduced from the specified maximum current Icc_{CORE_MAX} and is calculated by the equation:
$Icc_{CORE\_REG} = Icc_{CORE\_MAX} \times Vcc_{CORE\_TYP} / (Vcc_{CORE\_TYP} + Vcc_{CORE}$ Tolerance, Transient)

11. The current specified is the current required for a single Intel Celeron processor. A similar amount of current is drawn through the termination resistors on the opposite end of the AGTL+ bus, unless single-ended termination is used (see Section 2.1).
12. The current specified is also for AutoHALT state.
13. Maximum values are specified by design/characterization at nominal Vcc_{CORE}.
14. Based on simulation and averaged over the duration of any change in current. Use to compute the maximum inductance tolerable and reaction time of the voltage regulator. This parameter is not tested.
15. dIcc/dt specifications are measured and specified at the SC242 connector pins.
16. Vcc_5 and Icc_5 are not used by the Intel Celeron processor. This supply is used for the Voltage Transient Tools.
17. dIcc/dt specifications are measured and specified at the PPGA package's processor pins.

Table 5. AGTL+ Signal Groups DC Specifications [1]

Symbol	Parameter	Min	Max	Unit	Notes
V_{IL}	Input Low Voltage	–0.3	0.82	V	
V_{IH}	Input High Voltage	1.22	V_{TT}	V	2, 3
Ron	Buffer On Resistance		16.67	Ω	8
I_L	Leakage Current		±100	µA	6
I_{LO}	Output Leakage Current		±15	µA	7

NOTES:
1. Unless otherwise noted, all specifications in this table apply to all Intel® Celeron™ processor frequencies and cache sizes.
2. V_{IH} and V_{OH} for the Intel Celeron processor may experience excursions of up to 200 mV above V_{TT} for a single system bus clock. However, input signal drivers must comply with the signal quality specifications in Section 3.0.
3. Minimum and maximum V_{TT} are given in Table 7.
4. Parameter correlated to measurement into a 25 Ω resistor terminated to 1.5 V.
5. I_{OH} for the Intel Celeron processor may experience excursions of up to 12 mA for a single system bus clock.
6. ($0 \le V_{IN} \le 2.0$ V +5%).
7. ($0 \le V_{OUT} \le 2.0$ V +5%).
8. Refer to the I/O Buffer Models for IV characteristics.

Table 6. Non-AGTL+ Signal Group DC Specifications [1]

Symbol	Parameter	Min	Max	Unit	Notes
V_{IL}	Input Low Voltage	–0.3	0.7	V	
V_{IH}	Input High Voltage	1.7	2.625	V	2.5 V +5% maximum
V_{OL}	Output Low Voltage		0.4	V	2
V_{OH}	Output High Voltage	N/A	2.625	V	All outputs are open-drain to 2.5 V +5%
I_{OL}	Output Low Current	14		mA	
I_{LI}	Input Leakage Current		±100	µA	3
I_{LO}	Output Leakage Current		±30	µA	4

NOTES:
1. Unless otherwise noted, all specifications in this table apply to all Intel® Celeron™ processor frequencies.
2. Parameter measured at 14 mA (for use with TTL inputs).
3. ($0 \le V_{IN} \le 2.5$ V +5%).
4. ($0 \le V_{OUT} \le 2.5$ V +5%).

2.11 AGTL+ System Bus Specifications

It is recommended that the AGTL+ bus be routed in a daisy-chain fashion with termination resistors to V_{TT} at each end of the signal trace. These termination resistors are placed electrically between the ends of the signal traces and the V_{TT} voltage supply and generally are chosen to approximate the substrate impedance. The valid high and low levels are determined by the input buffers using a reference voltage called V_{REF}. Single ended termination may be possible if trace lengths are tightly controlled, see the *Intel® 440EX AGPset Design Guide* (Order Number 290637) or the *Intel® Celeron™ Processor (PPGA) with the Intel® 440LX AGPset Design Guide* (Order Number 245088) for more information.

Table 7 below lists the nominal specification for the AGTL+ termination voltage (V_{TT}). The AGTL+ reference voltage (V_{REF}) is generated on the processor substrate (S.E.P. Package only) for the processor core, but should be set to $^2/_3$ V_{TT} for other AGTL+ logic using a voltage divider on the motherboard. It is important that the motherboard impedance be specified and held to a ±20% tolerance, and that the intrinsic trace capacitance for the AGTL+ signal group traces is known and well-controlled. For more details on AGTL+, see the *Pentium® II Processor Developer's Manual* (Order Number 243502) and AP-585, *Pentium® II Processor AGTL+ Guidelines* (Order Number 243330).

Table 7. Intel® Celeron™ Processor AGTL+ Bus Specifications

Symbol	Parameter	Min	Typ	Max	Units	Notes
V_{TT}	Bus Termination Voltage	1.365	1.50	1.635	V	1.5 V ±9% [3]
R_{TT}	Termination Resistor		56		Ohms	±5%
V_{REF}	Bus Reference Voltage		2/3 V_{TT}		V	±2% [4]

NOTES:
1. Unless otherwise noted, all specifications in this table apply to all Intel® Celeron™ processor frequencies.
2. V_{TT} must be held to 1.5 V ±9%; $dIcc_{VTT}/dt$ is specified in Table 4. It is recommended that V_{TT} be held to 1.5 V ±3% while the Intel Celeron processor system bus is idle. This is measured at the processor edge fingers.
3. V_{REF} is generated on the processor substrate to be 2/3 V_{TT} nominally (S.E.P. package only).

2.12 Intel® Celeron™ Processor System Bus AC Specifications

The Intel® Celeron™ processor system bus timings specified in this section are defined at the Intel Celeron processor edge fingers and the processor core pads. Timings specified at the processor edge fingers only apply to the S.E.P. Package and timings given at the processor core pads apply to both the S.E.P. Package and the PPGA package. Unless otherwise specified, timings are tested at the processor core during manufacturing. Timings at the processor edge fingers are specified by design characterization. See Section 7.0 for the Intel Celeron processor signal definitions. **Note that at 66 MHz system bus operation, the Intel Celeron processor timings at the processor edge fingers are identical to the Pentium II processor processor timings at the edge fingers.** See the *Pentium® II Processor at 233, 266, 300, and 333 MHz* (Order Number 243335) for more detail.

Table 8 through Table 20 list the AC specifications associated with the Intel Celeron processor system bus. These specifications are broken into the following categories: Table 8 through Table 10 contain the system bus clock specifications, Table 11 and Table 12 contain the AGTL+ specifications, Table 14 and Table 15 are the CMOS signal group specifications, Table 16 contains timings for the Reset conditions, Table 17 and Table 18 cover APIC bus timing, and Table 19 and

Table 20 cover TAP timing. For each pair of tables, the first table contains timing specifications for measurement or simulation at the processor edge fingers. The second table contains specifications for simulation at the processor core pads.

All Intel Celeron processor system bus AC specifications for the AGTL+ signal group are relative to the rising edge of the BCLK input. All AGTL+ timings are referenced to V_{REF} for both ‘0’ and ‘1’ logic levels unless otherwise specified.

The timings specified in this section should be used in conjunction with the I/O buffer models provided by Intel. These I/O buffer models, which include package information, are available for the Pentium II processor in Quad format as the *Pentium® II Processor I/O Buffer Models*, Quad XTK Format (Electronic Form). AGTL+ layout guidelines are also available in AP-585, *Pentium® II Processor AGTL+ Guidelines* (Order Number 243330).

Care should be taken to read all notes associated with a particular timing parameter.

Table 8. Intel® Celeron™ Processor System Bus AC Specifications (Clock) at the Processor Edge Fingers For the S.E.P. Package [1, 2, 3]

T# Parameter	Min	Nom	Max	Unit	Figure	Notes
System Bus Frequency		66.67		MHz		
T1’: BCLK Period	15.0			ns	6	4, 5, 6
T1B’: SC242 to Core Logic BCLK Offset		0.78		ns	6	Absolute Value [7,8]
T2’: BCLK Period Stability				±300ps		See Table 9
T3’: BCLK High Time	4.44			ns	6	@>2.0 V [6]
T4’: BCLK Low Time	4.44			ns	6	@<0.5 V [6]
T5’: BCLK Rise Time	0.84		2.31	ns	6	(0.5 V–2.0 V) [6, 9]
T6’: BCLK Fall Time	0.84		2.31	ns	6	(2.0 V–0.5 V) [6, 9]

NOTES:
1. Unless otherwise noted, all specifications in this table apply to all Intel® Celeron™ processor frequencies.
2. All AC timings for the AGTL+ signals are referenced to the BCLK rising edge at 0.70 V at the processor edge fingers. This reference is to account for trace length and capacitance on the processor substrate, allowing the processor core to receive the signal with a reference at 1.25 V. All AGTL+ signal timings (address bus, data bus, etc.) are referenced at 1.00 V at the processor edge fingers.
3. All AC timings for the CMOS signals are referenced to the BCLK rising edge at 0.70 V at the processor edge fingers. This reference is to account for trace length and capacitance on the processor substrate, allowing the processor core to receive the signal with a reference at 1.25 V. All CMOS signal timings (compatibility signals, etc.) are referenced at 1.25 V at the processor edge fingers.
4. The internal core clock frequency is derived from the Intel Celeron processor system bus clock. The system bus clock to core clock ratio is determined during initialization. Table 10 shows the supported ratios for each processor.
5. The BCLK period allows a +0.5 ns tolerance for clock driver variation.
6. This specification applies to Intel Celeron processors when operating at a system bus frequency of 66 MHz.
7. The BCLK offset time is the absolute difference needed between the BCLK signal arriving at the Intel Celeron processor edge finger at 0.5 V vs. arriving at the core logic at 1.25 V. The positive offset is needed to account for the delay between the SC242 connector and processor core. The positive offset ensures both the processor core and the core logic receive the BCLK edge concurrently.
8. See Section 3.1 for Intel Celeron processor system bus clock signal quality specifications.
9. Not 100% tested. Specified by design characterization as a clock driver requirement.

Table 9. Intel® Celeron™ Processor System Bus AC Specifications (Clock) at the Processor Core Pins For Both S.E.P. and PPGA Packages [1, 2, 3]

T# Parameter	Min	Nom	Max	Unit	Figure	Notes
System Bus Frequency		66.67		MHz		
T1: BCLK Period	15.0			ns	6	4, 5, 6
T2: BCLK Period Stability			±300	ps	6	6, 8, 9
T3: BCLK High Time	4.94			ns	6	@>2.0 V [6]
T4: BCLK Low Time	4.94			ns	6	@<0.5 V [6]
T5: BCLK Rise Time	0.34		1.36	ns	6	(0.5 V–2.0 V) [6, 10]
T6: BCLK Fall Time	0.34		1.36	ns	6	(2.0 V–0.5 V) [6, 10]

NOTES:
1. Unless otherwise noted, all specifications in this table apply to all Intel® Celeron™ processor frequencies.
2. All AC timings for the AGTL+ signals are referenced to the BCLK rising edge at 1.25 V at the processor core pin. All AGTL+ signal timings (address bus, data bus, etc.) are referenced at 1.00 V at the processor core pins.
3. All AC timings for the CMOS signals are referenced to the BCLK rising edge at 1.25 V at the processor core pin. All CMOS signal timings (compatibility signals, etc.) are referenced at 1.25 V at the processor core pins.
4. The internal core clock frequency is derived from the Intel Celeron processor system bus clock. The system bus clock to core clock ratio is determined during initialization. Table 10 shows the supported ratios for each processor.
5. The BCLK period allows a +0.5 ns tolerance for clock driver variation.
6. This specification applies to the Intel Celeron processor when operating at a system bus frequency of 66 MHz.
7. See Section 3.1 for Intel Celeron processor system bus clock signal quality specifications.
8. Due to the difficulty of accurately measuring clock jitter in a system, it is recommended that a clock driver be used that is designed to meet the period stability specification into a test load of 10 to 20 pF. This should be measured on the **rising edges of adjacent BCLKs crossing 1.25 V at the processor core pin**. The jitter present must be accounted for as a component of BCLK timing skew between devices.
9. The clock driver's closed loop jitter bandwidth must be set low to allow any PLL-based device to track the jitter created by the clock driver. The –20 dB attenuation point, as measured into a 10 to 20 pF load, should be less than 500 kHz. This specification may be ensured by design characterization and/or measured with a spectrum analyzer.
10. Not 100% tested. Specified by design characterization as a clock driver requirement.

Table 10. Valid Intel® Celeron™ Processor System Bus, Core Frequency [1, 2]

Core Frequency (MHz)	BCLK Frequency (MHz)	Frequency Multiplier
266	66	4
300	66	4.5
333	66	5
366	66	5.5
400	66	6
433	66	6.5

NOTES:
1. Contact your local Intel representative for the latest information on processor frequencies and/or frequency multipliers.
2. While other bus ratios are defined, operation at frequencies other than those listed are not supported.

Table 11. Intel® Celeron™ Processor System Bus AC Specifications (AGTL+ Signal Group) at the Processor Edge Fingers For the S.E.P. Package [1, 2, 3, 4]

T# Parameter	Min	Max	Unit	Figure	Notes
T7’: AGTL+ Output Valid Delay	1.07	6.37	ns	7	4, 5
T8’: AGTL+ Input Setup Time	1.96		ns	8	4, 6, 7, 8
T9’: AGTL+ Input Hold Time	1.53		ns	8	4, 9
T10’: RESET# Pulse Width	1.00		ms	10	10

NOTES:

1. Unless otherwise noted, all specifications in this table apply to all Intel® Celeron™ processor frequencies.
2. Not 100% tested. Specified by design characterization.
3. All AC timings for the AGTL+ signals are referenced to the BCLK rising edge at 0.50 V at the processor edge fingers. All AGTL+ signal timings (compatibility signals, etc.) are referenced at 1.00 V at the processor edge fingers.
4. This specification applies to Intel Celeron processors operating with a 66 MHz Intel Celeron processor system bus only.
5. Valid delay timings for these signals are specified into 50 Ω to 1.5 V and with V_{REF} at 1.0 V.
6. A minimum of 3 clocks must be guaranteed between two active-to-inactive transitions of TRDY#.
7. RESET# can be asserted (active) asynchronously, but must be deasserted synchronously.
8. Specification is for a minimum 0.40 V swing.
9. Specification is for a maximum 1.0 V swing.
10. After $V_{CC_{CORE}}$, and BCLK become stable.

Table 12. Intel® Celeron™ Processor System Bus AC Specifications (AGTL+ Signal Group) at the Processor Core Pins For the S.E.P. Package [1, 2, 3, 4]

T# Parameter	Min	Max	Unit	Figure	Notes
T7: AGTL+ Output Valid Delay	0.17	5.16	ns	7	5
T8: AGTL+ Input Setup Time	2.10		ns	8	5, 6, 7, 8
T9: AGTL+ Input Hold Time	0.77		ns	8	9
T10: RESET# Pulse Width	1.00		ms	10	7, 10

NOTES:

1. Unless otherwise noted, all specifications in this table apply to all Intel® Celeron™ processor frequencies.
2. These specifications are tested during manufacturing.
3. All AC timings for the AGTL+ signals are referenced to the BCLK rising edge at 1.25 V at the processor core pin. All AGTL+ signal timings (compatibility signals, etc.) are referenced at 1.00 V at the processor core pins.
4. This specification applies to the Intel Celeron processor operating with a 66 MHz Intel Celeron processor system bus only.
5. Valid delay timings for these signals are specified into 25 Ω to 1.5 V and with V_{REF} at 1.0 V.
6. A minimum of 3 clocks must be guaranteed between two active-to-inactive transitions of TRDY#.
7. RESET# can be asserted (active) asynchronously, but must be deasserted synchronously.
8. Specification is for a minimum 0.40 V swing.
9. Specification is for a maximum 1.0 V swing.
10. After $V_{CC_{CORE}}$ and BCLK become stable.

Table 13. Processor System Bus AC Specifications (AGTL+ Signal Group) at the Processor Core Pins for the PPGA Package [1, 2, 3, 4]

T# Parameter	Min	Max	Unit	Figure	Notes
T7: AGTL+ Output Valid Delay	0.30	4.43	ns		5
T8: AGTL+ Input Setup Time	2.10		ns		5, 6, 7
T9: AGTL+ Input Hold Time	0.85		ns		
T10: RESET# Pulse Width	1.00		ms		7, 8

NOTES:
1. Unless otherwise noted, all specifications in this table apply to all processor frequencies.
2. These specifications are tested during manufacturing.
3. All AC timings for the AGTL+ signals are referenced to the BCLK rising edge at 1.25 V at the processor pin. All GTL+ signal timings (compatibility signals, etc.) are referenced at 1.00 V at the processor pins.
4. This specification applies to the processor operating with a 66 MHz system bus only.
5. Valid delay timings for these signals are specified into 25 Ω to 1.5 V and with V_{REF} at 1.0 V.
6. A minimum of 3 clocks must be guaranteed between two active-to-inactive transitions of TRDY#.
7. RESET# can be asserted (active) asynchronously, but must be deasserted synchronously.
8. After $V_{CC_{CORE}}$ and BCLK become stable.

Table 14. Intel® Celeron™ Processor System Bus AC Specifications (CMOS Signal Group) at the Processor Edge Fingers For S.E.P. Package [1, 2, 3, 4]

T# Parameter	Min	Max	Unit	Figure	Notes
T11’: CMOS Output Valid Delay	1.00	10.5	ns	7	5
T12’: CMOS Input Setup Time	4.50		ns	8	6, 7, 8
T13’: CMOS Input Hold Time	1.50		ns	8	6, 7
T14’: CMOS Input Pulse Width, except PWRGOOD	2		BCLKs	7	Active and Inactive states
T14B: LINT[1:0] Input Pulse Width	6		BCLKs	7	9
T15’: PWRGOOD Inactive Pulse Width	10		BCLKs	7, 10	10, 11

NOTES:
1. Unless otherwise noted, all specifications in this table apply to all Intel® Celeron™ processor frequencies.
2. Not 100% tested. Specified by design characterization.
3. All AC timings for the CMOS signals are referenced to the BCLK rising edge at 0.50 V at the processor edge fingers. All CMOS signal timings (address bus, data bus, etc.) are referenced at 1.25 V.
4. These signals may be driven asynchronously.
5. Valid delay timings for these signals are specified to 2.5 V +5%.
6. This specification applies to Intel Celeron processors operating with a 66 MHz Intel Celeron processor system bus only.
7. To ensure recognition on a specific clock, the setup and hold times with respect to BCLK must be met.
8. INTR and NMI are only valid when the local APIC is disabled. LINT[1:0] are only valid when the local APIC is enabled.
9. This specification only applies when the APIC is enabled and the LINT1 or LINT0 pin is configured as an edge-triggered interrupt with fixed delivery; otherwise, specification T14 applies.

   PWRGOOD must remain below $V_{IL,max}$ (Table 5) until all the voltage planes meet the voltage tolerance specifications in Table 4 and BCLK has met the BCLK AC specifications in Table 9 for at least 10 clock cycles. PWRGOOD must rise glitch-free and monotonically to 2.5 V.
10. When driven inactive or after $V_{CC_{CORE}}$, and BCLK become stable.
11. If the BCLK signal meets its AC specification within 150 ns of turning on, then the PWRGOOD inactive pulse width specification (T15) is waived and BCLK may start after PWRGOOD is asserted. PWRGOOD must still remain below $V_{IL,max}$ until all the voltage planes meet the voltage tolerance specifications.

Table 15. Intel® Celeron™ Processor System Bus AC Specifications (CMOS Signal Group) at the Processor Core Pins For Both S.E.P. and PPGA Packages [1, 2, 3, 4]

T# Parameter	Min	Max	Unit	Figure	Notes
T11: CMOS Output Valid Delay	0.00	8.00	ns	7	5
T12: CMOS Input Setup Time	4.00		ns	8	6, 7, 8
T13: CMOS Input Hold Time	1.30		ns	8	6, 7
T14: CMOS Input Pulse Width, except PWRGOOD	2		BCLKs	7	Active and Inactive states
T14B: LINT[1:0] Input Pulse Width (S.E.P.P. Only)	6		BCLKs	7	9
T15: PWRGOOD Inactive Pulse Width	10		BCLKs	7,10	10, 11

NOTES:
1. Unless otherwise noted, all specifications in this table apply to all Intel® Celeron™ processor frequencies.
2. These specifications are tested during manufacturing.
3. All AC timings for the CMOS signals are referenced to the BCLK rising edge at 1.25 V at the processor core pins. All CMOS signal timings (address bus, data bus, etc.) are referenced at 1.25 V.
4. These signals may be driven asynchronously.
5. Valid delay timings for these signals are specified to 2.5 V +5%.
6. This specification applies to Intel Celeron processors operating with a 66 MHz Intel Celeron processor system bus only.
7. To ensure recognition on a specific clock, the setup and hold times with respect to BCLK must be met.
8. INTR and NMI are only valid when the local APIC is disabled. LINT[1:0] are only valid when the local APIC is enabled.
9. This specification only applies when the APIC is enabled and the LINT1 or LINT0 pin is configured as an edge-triggered interrupt with fixed delivery; otherwise, specification T14 applies.
10. When driven inactive or after $V_{CC_{CORE}}$, and BCLK become stable.
11. If the BCLK signal meets its AC specification within 150 ns of turning on, then the PWRGOOD inactive pulse width specification (T15) is waived and BCLK may start after PWRGOOD is asserted. PWRGOOD must still remain below $V_{IL,max}$ until all the voltage planes meet the voltage tolerance specifications.

    PWRGOOD must remain below $V_{IL,max}$ (Table 5) until all the voltage planes meet the voltage tolerance specifications in Table 4 and BCLK has met the BCLK AC specifications in Table 9 for at least 10 clock cycles. PWRGOOD must rise glitch-free and monotonically to 2.5 V.

Table 16. Intel® Celeron™ Processor System Bus AC Specifications (Reset Conditions) [1]

T# Parameter	Min	Max	Unit	Figure	Notes
T16: Reset Configuration Signals (A[14:5]#, BR0#, FLUSH#, INIT#) Setup Time	4		BCLKs	9	Before deassertion of RESET#
T17: Reset Configuration Signals (A[14:5]#, BR0#, FLUSH#, INIT#) Hold Time	2	20	BCLKs	9	After clock that deasserts RESET#

NOTES:
1. Unless otherwise noted, all specifications in this table apply to all Intel® Celeron™ processor frequencies.

Table 17. Intel® Celeron™ Processor System Bus AC Specifications (APIC Clock and APIC I/O) at the Processor Edge Fingers For S.E.P. Package [1, 2, 3, 4]

T# Parameter	Min	Max	Unit	Figure	Notes
T21’: PICCLK Frequency	2.0	33.3	MHz		
T22’: PICCLK Period	30.0	500.0	ns	6	
T23’: PICCLK High Time	12.0		ns	6	
T24’: PICCLK Low Time	12.0		ns	6	
T25’: PICCLK Rise Time	0.25	3.0	ns	6	
T26’: PICCLK Fall Time	0.25	3.0	ns	6	
T27’: PICD[1:0] Setup Time	8.5		ns	8	5
T28’: PICD[1:0] Hold Time	3.0		ns	8	5
T29’: PICD[1:0] Valid Delay	3.0	12.0	ns	7	5, 6, 7

NOTES:
1. Unless otherwise noted, all specifications in this table apply to all Intel® Celeron™ processor frequencies.
2. Not 100% tested. Specified by design characterization.
3. All AC timings for the APIC I/O signals are referenced to the PICCLK rising edge at 0.7 V at the processor edge fingers. All APIC I/O signal timings are referenced at 1.25 V at the processor edge fingers.
4. This specification applies to Intel Celeron processors operating with a 66 MHz Intel Celeron processor system bus only.
5. Referenced to PICCLK rising edge.
6. For open drain signals, valid delay is synonymous with float delay.
7. Valid delay timings for these signals are specified to 2.5 V +5%.

Table 18. Intel® Celeron™ Processor System Bus AC Specifications (APIC Clock and APIC I/O) at the Processor Core Pins For S.E.P. and PPGA Packages [1, 2, 3, 4]

T# Parameter	Min	Max	Unit	Figure	Notes
T21: PICCLK Frequency	2.0	33.3	MHz		
T22: PICCLK Period	30.0	500.0	ns	6	
T23: PICCLK High Time	12.0		ns	6	
T24: PICCLK Low Time	12.0		ns	6	
T25: PICCLK Rise Time	0.25	3.0	ns	6	
T26: PICCLK Fall Time	0.25	3.0	ns	6	
T27: PICD[1:0] Setup Time	8.0		ns	8	5
T28: PICD[1:0] Hold Time	2.5		ns	8	5
T29: PICD[1:0] Valid Delay	1.5	10.0	ns	7	5, 6, 7

NOTES:
1. Unless otherwise noted, all specifications in this table apply to all Intel® Celeron™ processor frequencies.
2. These specifications are tested during manufacturing.
3. All AC timings for the APIC I/O signals are referenced to the PICCLK rising edge at 1.25 V at the processor core pins. All APIC I/O signal timings are referenced at 1.25 V at the processor core pins.
4. This specification applies to Intel Celeron processors operating with a 66 MHz Intel Celeron processor system bus only.
5. Referenced to PICCLK rising edge.
6. For open drain signals, valid delay is synonymous with float delay.
7. Valid delay timings for these signals are specified to 2.5 V +5%.

Table 19. Intel® Celeron™ Processor System Bus AC Specifications (TAP Connection) at the Processor Edge Fingers For S.E.P. Package [1, 2, 3]

T# Parameter	Min	Max	Unit	Figure	Notes
T30’: TCK Frequency		16.667	MHz		
T31’: TCK Period	60.0		ns	6	
T32’: TCK High Time	25.0		ns	6	@1.7 V
T33’: TCK Low Time	25.0		ns	6	@0.7 V
T34’: TCK Rise Time		5.0	ns	6	(0.7 V–1.7 V) [4]
T35’: TCK Fall Time		5.0	ns	6	(1.7 V–0.7 V) [4]
T36’: TRST# Pulse Width	40.0		ns	12	Asynchronous
T37’: TDI, TMS Setup Time	5.5		ns	11	5
T38’: TDI, TMS Hold Time	14.5		ns	11	5
T39’: TDO Valid Delay	2.0	13.5	ns	11	6, 7
T40’: TDO Float Delay		28.5	ns	11	6, 7
T41’: All Non-Test Outputs Valid Delay	2.0	27.5	ns	11	6, 8, 9
T42’: All Non-Test Inputs Setup Time		27.5	ns	11	6, 8, 9
T43’: All Non-Test Inputs Setup Time	5.5		ns	11	5, 8, 9
T44’: All Non-Test Inputs Hold Time	14.5		ns	11	5, 8, 9

NOTES:
1. Unless otherwise noted, all specifications in this table apply to all Intel® Celeron™ processor frequencies.
2. All AC timings for the TAP signals are referenced to the TCK rising edge at 0.70 V at the processor edge fingers. All TAP signal timings (TMS, TDI, etc.) are referenced at 1.25 V at the processor edge fingers.
3. Not 100% tested. Specified by design characterization.
4. 1 ns can be added to the maximum TCK rise and fall times for every 1 MHz below 16.667 MHz.
5. Referenced to TCK rising edge.
6. Referenced to TCK falling edge.
7. Valid delay timing for this signal is specified to 2.5 V +5%.
8. Non-Test Outputs and Inputs are the normal output or input signals (besides TCK, TRST#, TDI, TDO, and TMS). These timings correspond to the response of these signals due to TAP operations.
9. During Debug Port operation, use the normal specified timings rather than the TAP signal timings.

Table 20. Intel® Celeron™ Processor System Bus AC Specifications (TAP Connection) at the Processor Core Pins For Both S.E.P. and PPGA Packages [1, 2, 3]

T# Parameter	Min	Max	Unit	Figure	Notes
T30: TCK Frequency		16.667	MHz		
T31: TCK Period	60.0		ns	6	
T32: TCK High Time	25.0		ns	6	@1.7 V [10]
T33: TCK Low Time	25.0		ns	6	@0.7 V [10]
T34: TCK Rise Time		5.0	ns	6	(0.7 V–1.7 V) [4, 10]
T35: TCK Fall Time		5.0	ns	6	(1.7 V–0.7 V) [4, 10]
T36: TRST# Pulse Width	40.0		ns	12	Asynchronous [10]
T37: TDI, TMS Setup Time	5.0		ns	11	5
T38: TDI, TMS Hold Time	14.0		ns	11	5
T39: TDO Valid Delay	1.0	10.0	ns	11	6, 7
T40: TDO Float Delay		25.0	ns	11	6, 7, 10
T41: All Non-Test Outputs Valid Delay	2.0	25.0	ns	11	6, 8, 9
T42: All Non-Test Inputs Setup Time		25.0	ns	11	6, 8, 9, 10
T43: All Non-Test Inputs Setup Time	5.0		ns	11	5, 8, 9
T44: All Non-Test Inputs Hold Time	13.0		ns	11	5, 8, 9

NOTES:
1. Unless otherwise noted, all specifications in this table apply to all Intel® Celeron™ processor frequencies.
2. All AC timings for the TAP signals are referenced to the TCK rising edge at 1.25 V at the processor core pins. All TAP signal timings (TMS, TDI, etc.) are referenced at 1.25 V at the processor core pins.
3. These specifications are tested during manufacturing, unless otherwise noted.
4. 1 ns can be added to the maximum TCK rise and fall times for every 1 MHz below 16.667 MHz.
5. Referenced to TCK rising edge.
6. Referenced to TCK falling edge.
7. Valid delay timing for this signal is specified to 2.5 V +5%.
8. Non-Test Outputs and Inputs are the normal output or input signals (besides TCK, TRST#, TDI, TDO, and TMS). These timings correspond to the response of these signals due to TAP operations.
9. During Debug Port operation, use the normal specified timings rather than the TAP signal timings.
10. Not 100% tested. Specified by design characterization.

Note: For Figure 3 through Figure 9, the following apply:

1. Figure 3 through Figure 9 are to be used in conjunction with Table 8 through Table 20.
2. All AC timings for the AGTL+ signals at the processor edge fingers are referenced to the BCLK rising edge at 0.50 V. This reference is to account for trace length and capacitance on the processor substrate, allowing the processor core to receive the signal with a reference at 1.25 V. All AGTL+ signal timings (address bus, data bus, etc.) are referenced at 1.00 V at the processor edge fingers.
3. All AC timings for the AGTL+ signals at the processor core pins are referenced to the BCLK rising edge at 1.25 V. All AGTL+ signal timings (address bus, data bus, etc.) are referenced at 1.00 V at the processor core pins.
4. All AC timings for the CMOS signals at the processor edge fingers are referenced to the BCLK rising edge at 0.50 V. This reference is to account for trace length and capacitance on the processor substrate, allowing the processor core to receive the signal with a reference at 1.25 V. All CMOS signal timings (compatibility signals, etc.) are referenced at 1.25 V at the processor edge fingers.
5. All AC timings for the APIC I/O signals at the processor edge fingers are referenced to the PICCLK rising edge at 0.7 V. All APIC I/O signal timings are referenced at 1.25 V at the processor edge fingers.
6. All AC timings for the TAP signals at the processor edge fingers are referenced to the TCK rising edge at 0.70 V. All TAP signal timings (TMS, TDI, etc.) are referenced at 1.25 V at the processor edge fingers.

Figure 2. BCLK to Core Logic Offset

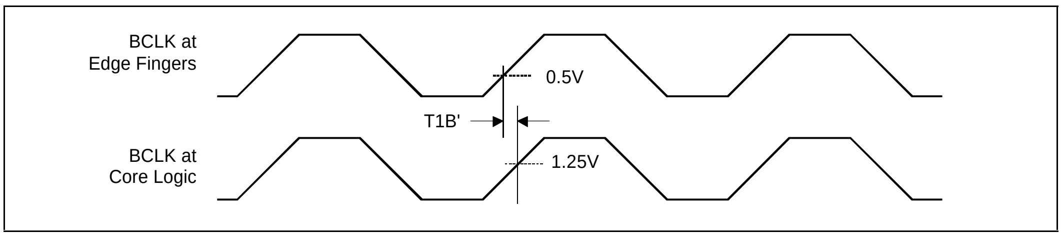


Figure 3. BCLK*, PICCLK, and TCK Generic Clock Waveform

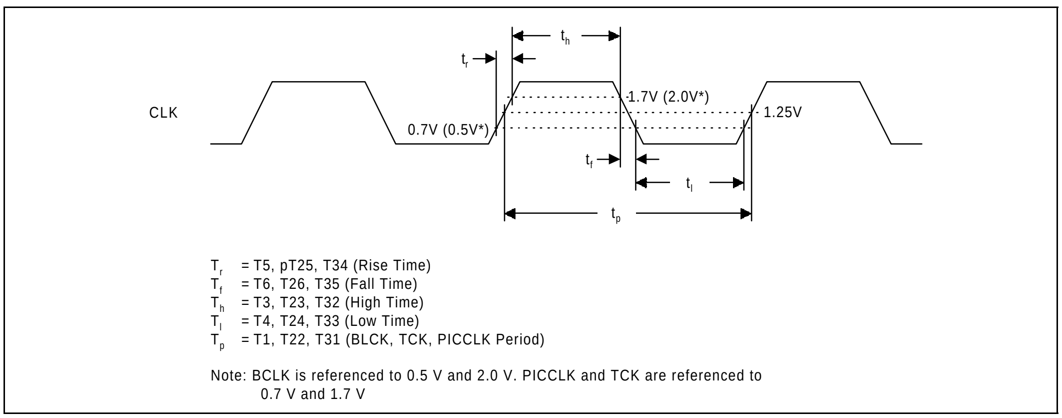
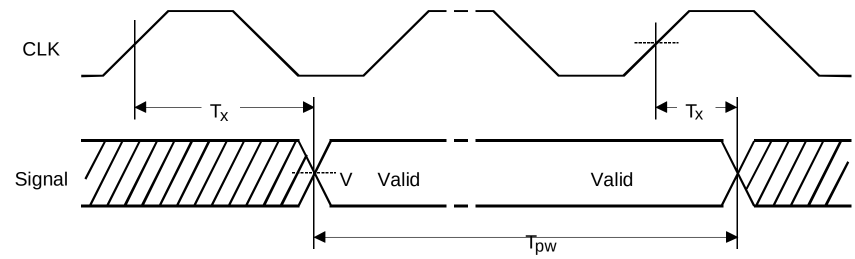


Figure 4. Intel® Celeron™ Processor System Bus Valid Delay Timings

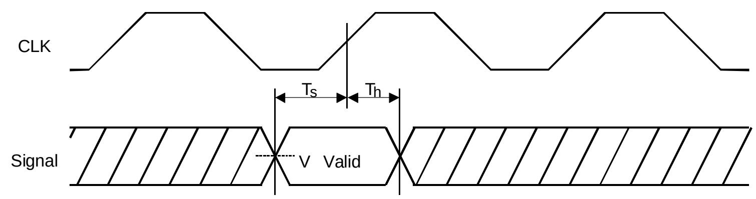


T_x = T7, T11, T29 (Valid Delay)

T_{pw} = T14, T15 (Pulse Wdith)

V = 1.0V for GTL+ signal group; 1.25V for CMOS, APIC and JTAG signal groups

Figure 5. Intel® Celeron™ Processor System Bus Setup and Hold Timings

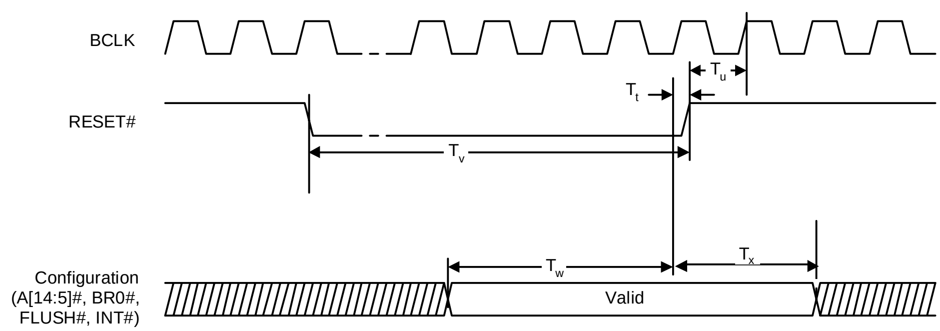


T_s = T8, T12, T27 (Setup Time)

T_h = T9, T13, T28 (Hold Time)

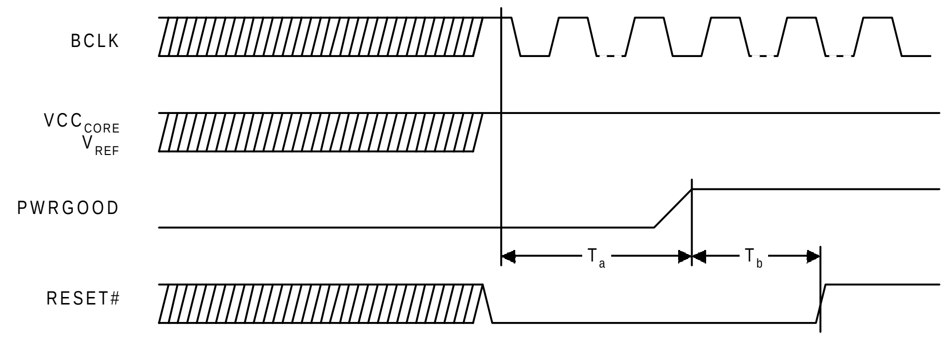
V = 1.0V for GTL+ signal group; 1.25V for CMOS, APIC and JTAG signal groups

Figure 6. Intel® Celeron™ Processor System Bus Reset and Configuration Timings



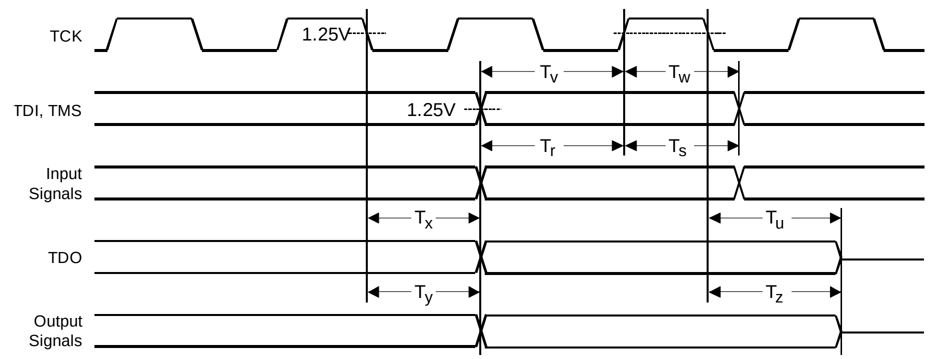
T_t = T9 (GTL+ Input Hold Time)
T_u = T8 (GTL+ Input Setup Time)
T_v = T10 (RESET# Pulse Width)
T_w = T16 (Reset Configuration Signals (A[14:5]#, BR0#, FLUSH#, INIT#) Setup
T_x = T17 (Reset Configuration Signals (A[14:5]#, BR0#, FLUSH#, INIT#) Hold

Figure 7. Power-On Reset and Configuration Timings



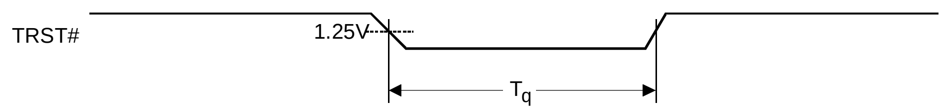
T_a = T15 (PWRGOOD Inactive Pulse Width)
T_b = T10 (RESET# Pulse Width)

Figure 8. Test Timings (TAP Connection)



T_r = T43 (All Non-Test Inputs Setup Time)
T_s = T44 (All Non-Test Inputs Hold Time)
T_u = T40 (TDO Float Delay)
T_v = T37 (TDI, TMS Setup Time)
T_w = T38 (TDI, TMS Hold Time)
T_x = T39 (TDO Valid Delay)
T_y = T41 (All Non-Test Outputs Valid Delay)
T_z = T42 (All Non-Test Outputs Float Delay)

Figure 9. Test Reset Timings



T_q = T37 (TRST# Pulse Width)

3.0 System Bus Signal Simulations

Signals driven on the Intel® Celeron™ processor system bus should meet signal quality specifications to ensure that the components read data properly and to ensure that incoming signals do not affect the long term reliability of the component. Specifications are provided for simulation at the processor core; guidelines are provided for correlation to the processor edge fingers. These edge finger guidelines are intended for use during testing and measurement of system signal integrity. Violations of these guidelines are permitted, but if they occur, simulation of signal quality at the processor core should be performed to ensure that no violations of signal quality specifications occur. Meeting the specifications at the processor core in Table 21, Table 23, and Table 25 ensures that signal quality effects will not adversely affect processor operation, but does not necessarily guarantee that the guidelines in Table 22, Table 24, and Table 26 will be met.

3.1 Intel® Celeron™ Processor System Bus Clock (BCLK) Signal Quality Specifications and Measurement Guidelines

Table 21 describes the signal quality specifications at the processor core for the Intel® Celeron™ processor system bus clock (BCLK) signal. Table 22 describes guidelines for signal quality measurement at the processor edge fingers. Figure 10 describes the signal quality waveform for the system bus clock at the processor core pins; Figure 11 describes the signal quality waveform for the system bus clock at the processor edge fingers.

Table 21. BCLK Signal Quality Specifications for Simulation at the Processor Core For Both S.E.P. and PPGA Packages [1]

T# Parameter	Min	Nom	Max	Unit	Figure	Notes
V1: BCLK V_{IL}			0.5	V	14	
V2: BCLK V_{IH}	2.0			V	14	2
V3: V_{IN} Absolute Voltage Range	–0.7		3.5	V	14	2
V4: Rising Edge Ringback	1.7			V	14	3
V5: Falling Edge Ringback			0.7	V	14	3

NOTES:
1. Unless otherwise noted, all specifications in this table apply to all Intel® Celeron™ processor frequencies.
2. This is the Intel Celeron processor system bus clock overshoot and undershoot specification for 66 MHz system bus operation.
3. The rising and falling edge ringback voltage specified is the minimum (rising) or maximum (falling) absolute voltage the BCLK signal can dip back to after passing the V_{IH} (rising) or V_{IL} (falling) voltage limits. This specification is an absolute value.

Figure 10. BCLK, TCK, PICCLK Generic Clock Waveform at the Processor Core Pins

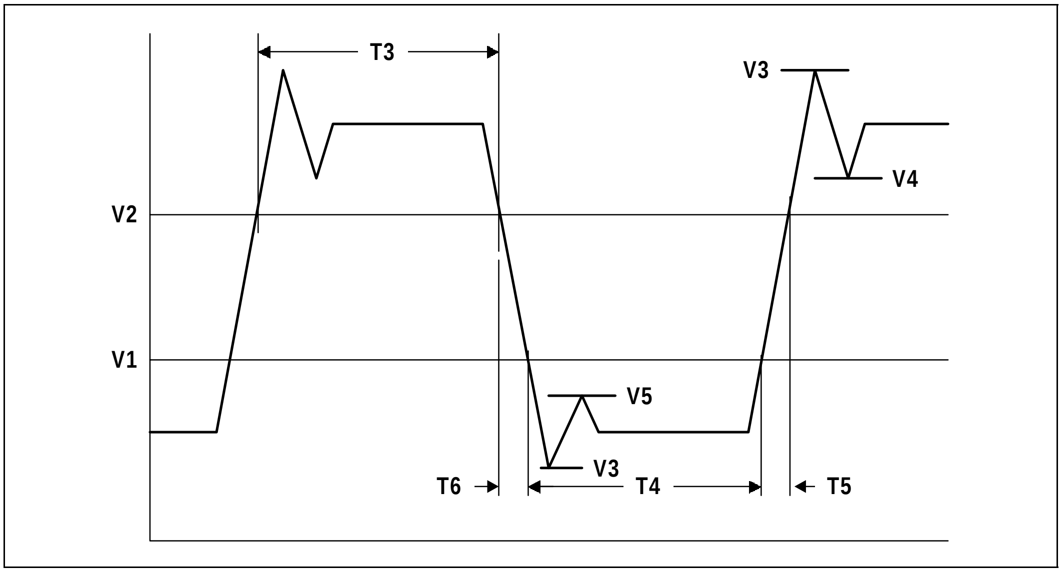
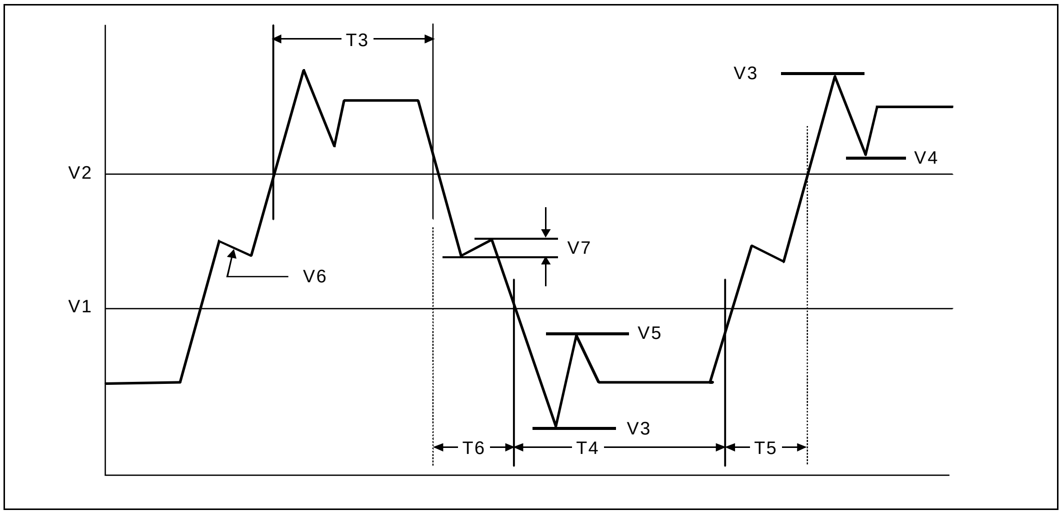


Table 22. BCLK Signal Quality Guidelines for Edge Finger Measurement on the S.E.P. Package [1]

T# Parameter	Min	Nom	Max	Unit	Figure	Notes
V1’: BCLK V_{IL}			0.5	V	14	
V2’: BCLK V_{IH}	2.0			V	14	
V3’: V_{IN} Absolute Voltage Range	–0.5		3.3	V	14	2
V4’: Rising Edge Ringback	2.0			V	14	3
V5’: Falling Edge Ringback			0.5	V	14	3
V6’: T_{line} Ledge Voltage	1.0		1.7	V	14	At Ledge Midpoint [4]
V7’: T_{line} Ledge Oscillation			0.2	V	14	Peak-to-Peak [5]

NOTES:
1. Unless otherwise noted, all specifications in this table apply to all Intel® Celeron™ processor frequencies.
2. This is the Intel Celeron processor system bus clock overshoot and undershoot measurement guideline.
3. The rising and falling edge ringback voltage guideline is the minimum (rising) or maximum (falling) absolute voltage the BCLK signal may dip back to after passing the V_{IH} (rising) or V_{IL} (falling) voltage limits. This guideline is an absolute value.
4. The BCLK at the processor edge fingers may have a dip or ledge midway on the rising or falling edge. The midpoint voltage level of this ledge should be within the range of the guideline.
5. The ledge (V7) is allowed to have peak-to-peak oscillation as given in the guideline.

Figure 11. BCLK, TCK, PICCLK Generic Clock Waveform at the Processor Edge Fingers



3.2 AGTL+ Signal Quality Specifications and Measurement Guidelines

Many scenarios have been simulated to generate a set of AGTL+ layout guidelines which are available in AP-585, *Pentium® II Processor AGTL+ Guidelines* (Order Number 243330). Refer to the *Pentium® II Processor Developer's Manual* (Order Number 243502) for the AGTL+ buffer specification.

Table 23 provides the AGTL+ signal quality specifications for Intel® Celeron™ processors for use in simulating signal quality at the processor core. Table 24 provides AGTL+ signal quality guidelines for measuring and testing signal quality at the processor edge fingers. Figure 12 describes the signal quality waveform for AGTL+ signals at the processor core and edge fingers. For more information on the AGTL+ interface, see the *Pentium® II Processor Developer's Manual* (Order Number 243502).

Table 23. AGTL+ Signal Groups Ringback Tolerance Specifications at the Processor Core For Both the S.E.P. and PPGA Packages [1, 2, 3]

T# Parameter	Min	Unit	Figure	Notes
α: Overshoot	100	mV	15	4
τ: Minimum Time at High	1.00	ns	15	4
ρ: Amplitude of Ringback	–100	mV	15	4, 5
ϕ: Final Settling Voltage	100	mV	15	4
δ: Duration of Squarewave Ringback	N/A	ns	15	

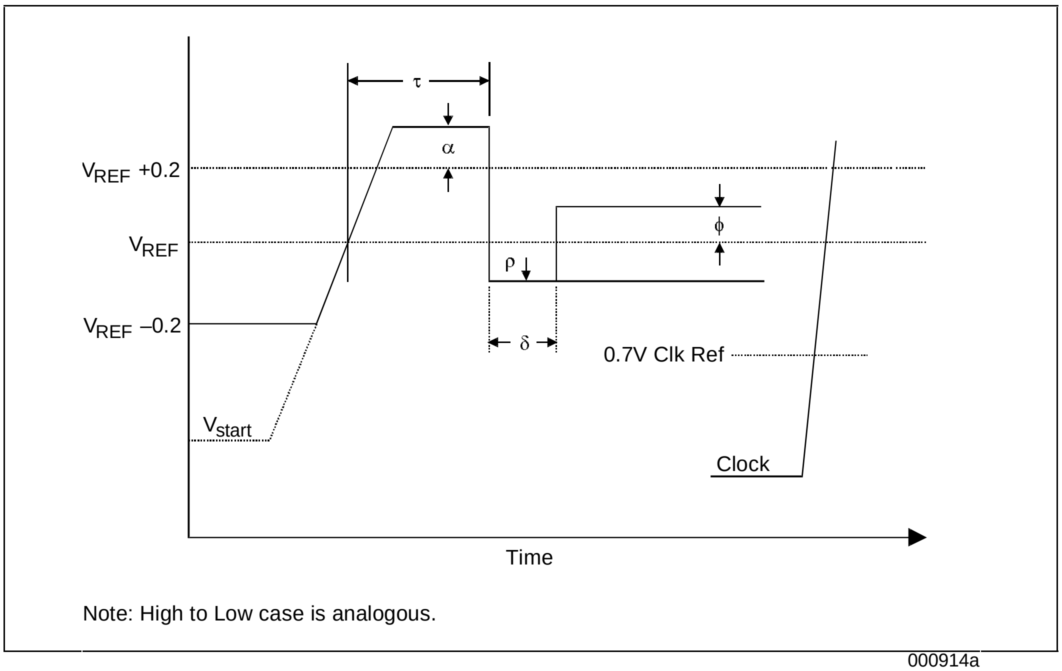
NOTES:
1. Unless otherwise noted, all specifications in this table apply to all Intel® Celeron™ processor frequencies.
2. Specifications are for the edge rate of 0.3 - 0.8 V/ns. See Figure 12 for the generic waveform.
3. All values specified by design characterization.
4. This specification applies to Intel Celeron processors operating with a 66 MHz Intel Celeron processor system bus only.
5. Ringback below V_{REF} + 20 mV is not supported.

Table 24. AGTL+ Signal Groups Ringback Tolerance Guidelines for Edge Finger Measurement on the S.E.P. Package [1, 2, 3]

T# Parameter	Min	Unit	Figure	Notes
α’: Overshoot	100	mV	15	
τ’: Minimum Time at High	1.5	ns	15	4
ρ’: Amplitude of Ringback	–250	mV	15	4, 5
φ’: Final Settling Voltage	250	mV	15	4
δ’: Duration of Squarewave Ringback	N/A	ns	15	

NOTES:
1. Unless otherwise noted, all guidelines in this table apply to all Intel® Celeron™ processor frequencies.
2. Guidelines are for the edge rate of 0.3 - 0.8 V/ns. See Figure 12 for the generic waveform.
3. All values specified by design characterization.
4. This guideline applies to Intel Celeron processors operating with a 66 MHz system bus only.
5. Ringback below V_{REF} + 250 mV is not supported.

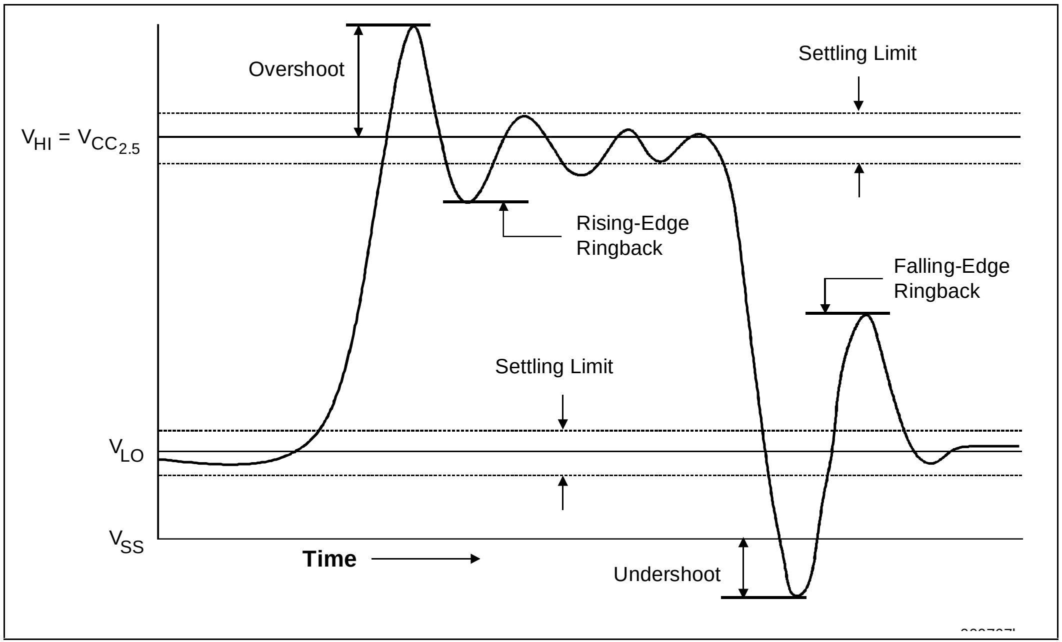
Figure 12. Low to High AGTL+ Receiver Ringback Tolerance



3.3 Non-AGTL+ Signal Quality Specifications and Measurement Guidelines

There are three signal quality parameters defined for non-AGTL+ signals: overshoot/undershoot, ringback, and settling limit. All three signal quality parameters are shown in Figure 13 for the non-AGTL+ signal group.

Figure 13. Non-AGTL+ Overshoot/Undershoot, Settling Limit, and Ringback



3.3.1 Overshoot/Undershoot Guidelines

Overshoot (or undershoot) is the absolute value of the maximum voltage above the nominal high voltage or below V_{SS}. The overshoot/undershoot guideline limits transitions beyond V_{CC} or V_{SS} due to the fast signal edge rates. (See Figure 13 for non-AGTL+ signals.) The processor can be damaged by repeated overshoot events on 2.5 V tolerant buffers if the charge is large enough (i.e., if the overshoot is great enough). However, excessive ringback is the dominant detrimental system timing effect resulting from overshoot/undershoot (i.e., violating the overshoot/undershoot guideline will make satisfying the ringback specification difficult). **The overshoot/undershoot guideline is 0.7 V** and assumes the absence of diodes on the input. These guidelines should be verified in simulations **without the on-chip ESD protection diodes present** because the diodes will begin clamping the 2.5 V tolerant signals beginning at approximately 0.7 V above the 2.5 V supply and 0.7 V below V_{SS}. If signals are not reaching the clamping voltage, this will not be an issue. A system should not rely on the diodes for overshoot/undershoot protection as this will negatively affect the life of the components and make meeting the ringback specification very difficult.

3.3.2 Ringback Specification

Ringback refers to the amount of reflection seen after a signal has switched. The ringback specification is **the voltage that the signal rings back to after achieving its maximum absolute value**. (See Figure 13 for an illustration of ringback.) Excessive ringback can cause false signal detection or extend the propagation delay. The ringback specification applies to the input pin of each receiving agent. Violations of the signal ringback specification are not allowed under any circumstances for non-AGTL+ signals.

Ringback can be simulated with or without the input protection diodes that can be added to the input buffer model. However, signals that reach the clamping voltage should be evaluated further. See Table 25 for the signal ringback specifications for non-AGTL+ signals for simulations at the processor core, and Table 26 for guidelines on measuring ringback at the edge fingers.

Table 25. Signal Ringback Specifications for Non-AGTL+ Signal Simulation at the Processor Core For Both S.E.P. and PPGA Packages [1]

Input Signal Group	Transition	Maximum Ringback (with Input Diodes Present)	Unit	Figure	Notes
Non-AGTL+ Signals	0 → 1	1.7	V	16	
Non-AGTL+ Signals	1 → 0	0.7	V	16	

NOTE:
1. Unless otherwise noted, all specifications in this table apply to all Intel® Celeron™ processor frequencies.

Table 26. Signal Ringback Guidelines for Non-AGTL+ Signal Edge Finger Measurement on the S.E.P. Package [1]

Input Signal Group	Transition	Maximum Ringback (with Input Diodes Present)	Unit	Figure	Notes
Non-AGTL+ Signals	0 → 1	2.0	V	16	
Non-AGTL+ Signals	1 → 0	0.7	V	16	

NOTE:
1. Unless otherwise noted, all specifications in this table apply to all Intel® Celeron™ processor frequencies.

3.3.3 Settling Limit Guideline

Settling limit defines the maximum amount of ringing at the receiving pin that a signal must reach before its next transition. The amount allowed is 10 percent of the total signal swing ($V_{HI} - V_{LO}$) above and below its final value. A signal should be within the settling limits of its final value, when either in its high state or low state, before it transitions again.

Signals that are not within their settling limit before transitioning are at risk of unwanted oscillations which could jeopardize signal integrity. Simulations to verify settling limit may be done either with or without the input protection diodes present. Violation of the settling limit guideline is acceptable if simulations of 5 to 10 successive transitions do not show the amplitude of the ringing increasing in the subsequent transitions.

4.0 Thermal Specifications and Design Considerations

The Intel® Celeron™ processor does not use a thermal plate. The heatsink for this processor is attached directly to the processor's heatslug.

4.1 Thermal Specifications

Table 27 and Table 28 provide both the Processor Power and Heatsink Design Target for Intel® Celeron™ processors. Processor Power is defined as the total power dissipated by the processor core and its package. Therefore, the S.E.P. Package's Processor Power would also include power dissipated by the AGTL+ termination resistors. The overall system chassis thermal design must comprehend the entire Processor Power. The Heatsink Design Target consists of only the processor core, which dissipates the majority of the thermal power.

Systems should design for the highest possible thermal power, even if a processor with a lower thermal dissipation is planned. The processor's heatslug is the attach location for all thermal solutions. The maximum and minimum case temperatures are also specified in Table 27 and Table 28. A thermal solution should be designed to ensure the temperature of the case never exceeds these specifications.

Table 27. Intel® Celeron™ Processor Power for the S.E.P. Package [1]

Processor Core Frequency (MHz)	L2 Cache Size (KB)	Processor Power (W)[2]	Heatsink Design Target (W)[3]	Minimum T_{CASE} (°C)	Maximum T_{CASE} (°C)
266	0	16.6	16.0	5	85
300	0	18.4	17.8	5	85
300A	128	18.4	17.8	5	85
333	128	20.2	19.7	5	85
366	128	22.2	21.7	5	85
400	128	24.2	23.7	5	85
433	128	24.6	24.1	5	85

NOTES:
1. These values are specified at nominal $V_{CC_{CORE}}$ for the processor core.
2. Processor Power is power generated from the S.E.P. Package's substrate, which includes the processor core and the AGTL+ termination resistors.
3. Heatsink Design Target refers to the power consumption of the processor core.

Table 28. Intel® Celeron™ Processor Power for the PPGA Package [1,2]

Processor Core Frequency (MHz)	L2 Cache Size (KB)	Processor Power (W)	Heatsink Design Target (W)	Minimum TCASE (°C)	Maximum TCASE (°C)
300A	128	17.8	17.8	5	85
333	128	19.7	19.7	5	85
366	128	21.7	21.7	5	85
400	128	23.7	23.7	5	85
433	128	24.1	24.1	5	85

NOTES:

1. These values are specified at nominal Vcc_{CORE} for the processor core.
2. Processor Power and Heatsink Design Target are the same value because the PPGA package does not have AGTL+ termination resistors.

4.1.1 Thermal Diode

The Intel® Celeron™ Processor incorporates an on-die diode that can be used to monitor the die temperature. A thermal sensor located on the motherboard may monitor the die temperature of the Intel Celeron processor for thermal management purposes. Table 29 and Table 30 provide the diode parameter and interface specifications.

Table 29. Thermal Diode Parameters[4]

Symbol	Min	Typ	Max	Unit	Notes
$I_{forward\ bias}$	5		500	uA	1
n_ideality	1.0000	1.0065	1.0173		2,3

NOTES:

1. Intel does not support or recommend operation of the thermal diode under reverse bias.
2. At room temperature with a forward bias of 630 mV.
3. n_ideality is the diode ideality factor parameter, as represented by the diode equation: I-Io(e (Vd*q)/(nkT) - 1).
4. Not 100% tested. Specified by design characterization.

Table 30. Thermal Diode Interface

Pin Name	SC242 Connector Signal #	370-Pin Socket Pin #	Pin Description
THERMDP	B14	AL31	diode anode (p junction)
THERMDN	B15	AL29	diode cathode (n junction)

4.2 Thermal Parameters

This section defines the terms used for Intel® Celeron™ processor thermal analysis.

4.2.1 Ambient Temperature

Ambient temperature, T_A, is the temperature of the ambient air surrounding the package. The design recommendation of T_A is 45 °C. In a system environment, ambient temperature is the temperature of the air upstream from the package and in its close vicinity; or in an active cooling system, it is the inlet air to the active cooling device.

4.2.2 Thermal Resistance

The thermal resistance value for the case to ambient, Θ_{CA} is used as a measure of the cooling solution's performance. Θ_{CA} is comprised of the case to sink thermal, Θ_{CS} and the sink to ambient thermal resistance, Θ_{SA}. Θ_{CS} is a measure of the thermal resistance along the heat flow path from the top of the heatslug to the bottom of the cooling solution. This value is strongly dependent on the material, conductivity, and thickness of the thermal interface used. Θ_{SA} is a measure of the thermal resistance from the top of the cooling solution to the local ambient air. Θ_{SA} values depend on the material, thermal conductivity, and geometry of the thermal cooling solution as well as on the airflow rates.

4.2.3 Thermal Solution Performance

All processor thermal solutions should attach to the processor's heatslug.

The thermal solution must adequately control the processor's case temperatures below the maximum and above the minimum specified in Table 27. The performance of any thermal solution is defined as the thermal resistance between the case temperature and the ambient air around the processor (Θ_{CA}). The lower the thermal resistance between the case and the ambient air, the more efficient the thermal solution is. The required Θ_{CA} is dependent upon the maximum allowed case temperature (T_{CASE}), the local ambient temperature (T_{LA}) and the maximum power dissipation of the processor.

$$\Theta_{CA} = (T_{CASE} – T_{LA}) / P_D$$

The case temperature and device power is listed in Table 27. T_{LA} is a function of the system design. Table 31 provides an example of the resulting thermal solution performance required for a 266 MHz Intel Celeron processor at different ambient air temperatures around the processor.

Table 31. Example Thermal Solution Performance for 266 MHz Intel® Celeron™ Processor at Power of 16.6 Watts

	Local Ambient Temperature (T_{LA})		
	35 °C	40 °C	45 °C
Θ_{CA} (°C/Watt)	3.01	2.71	2.41

A critical but controllable factor to decrease the value of Θ_{CS} is management of the thermal interface between the case and heatsink. The other controllable factor (Θ_{SA}) is determined by the design of the heatsink and airflow around the heatsink.

4.3 Thermal Solution Attach Methods

It is recommended that the Intel Celeron processor be integrated with an Intel designed heatsink and clip. These components are available from major manufacturers.

5.0 Mechanical Specifications

There are two package technologies which Intel® Celeron™ processors use. They are the S.E.P. Package and the PPGA package. The S.E.P. Package contains the processor core and passive components, while the PPGA package does not have passive components.

The processor edge connector defined in this document is referred to as the "SC242 connector." See the *SC242 Design Guidelines* (Order Number 243397) for further details on the edge connector.

The processor socket connector is defined in this document is referred to as the "370-pin socket." See the *370-Pin Socket (PGA370) Design Guidelines* (Order Number 244410) for further details on the socket.

5.1 S.E.P. Package

This section defines the mechanical specifications and signal definitions for the Intel® Celeron™ processor in the S.E.P. Package.

5.1.1 Materials Information

The Intel® Celeron™ processor requires a retention mechanism. This retention mechanism may require motherboard hole dimensions to be 0.159" diameter holes if low cost plastic fasteners are used to secure the retention mechanisms in place. The larger diameter holes are necessary to provide a robust structural design that can guarantee stringent shock and vibe testing. If captive nuts are used in place of the plastic fasteners, then either the 0.159" or the 0.140" diameter holes will suffice as long as the corresponding sized attached mount is used.

Figure 14 with substrate dimensions is provided to aid in the design of a heatsink and clip. In Figure 15 all area on the secondary side of the substrate is zoned "keep out", except for 25 mils around the tooling holes and the top and side edges of the substrate.

Figure 14. Intel® Celeron™ Processor Substrate Dimensions (S.E.P. Package)

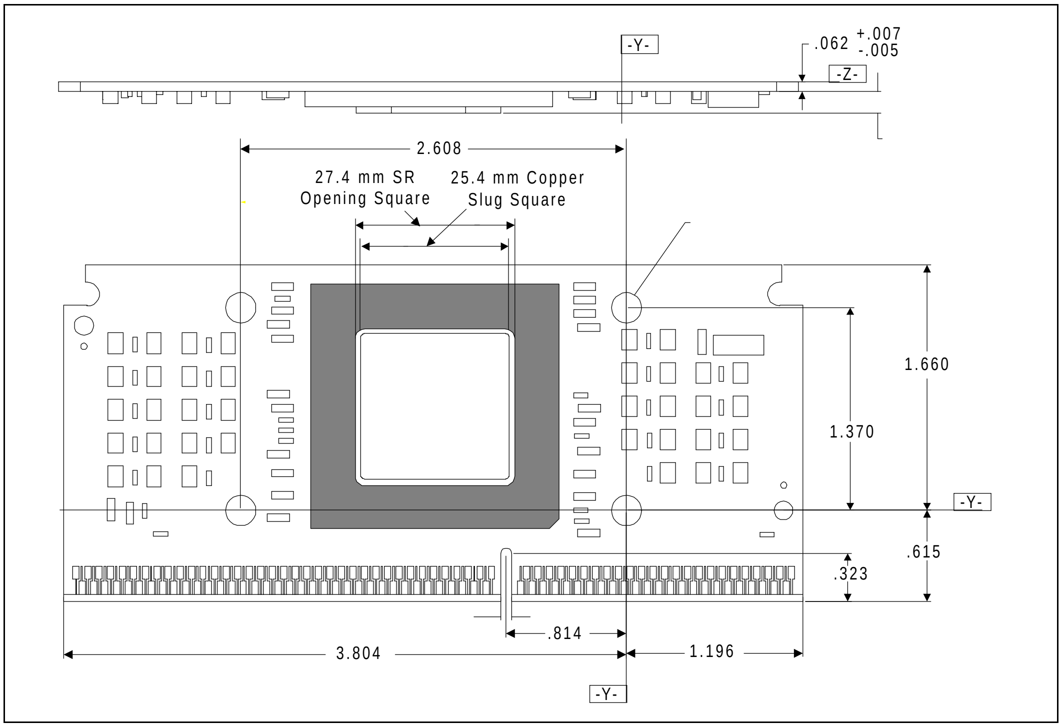
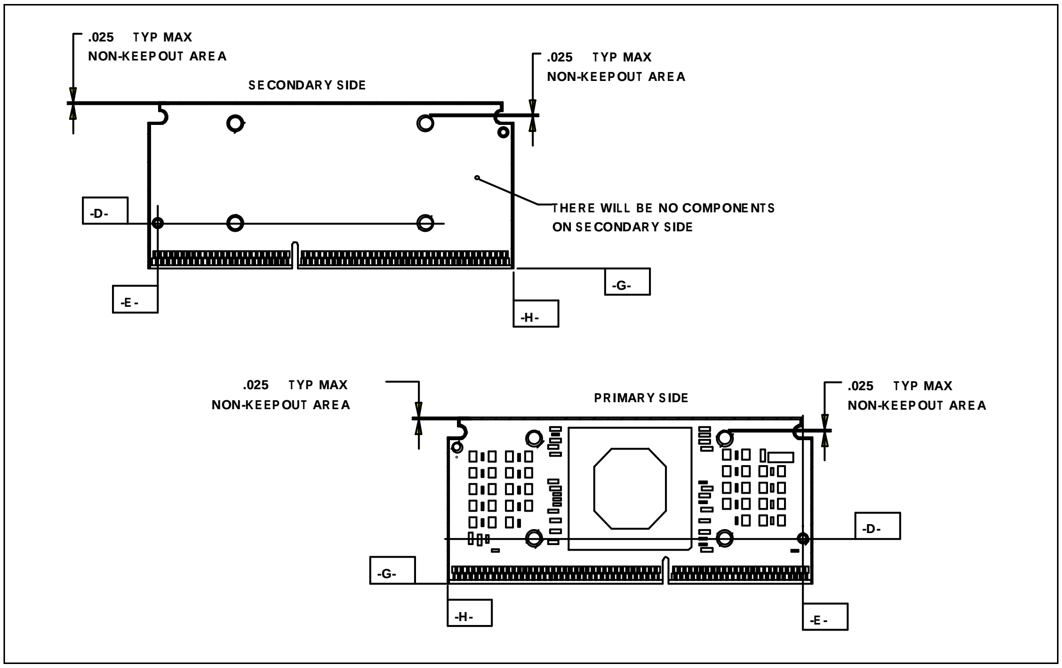


Figure 15. Intel® Celeron™ Processor Substrate Primary/Secondary Side Dimensions (S.E.P. Package)



5.1.2 Signal Listing

Table 32 and Table 33 provide the processor edge finger and SC242 connector signal definitions for Intel® Celeron™ processor. The signal locations on the SC242 edge connector are to be used for signal routing, simulation, and component placement on the motherboard.

Table 32 is the Intel Celeron processor substrate edge finger listing in order by pin number.

Table 32. S.E.P. Package Signal Listing in Order by Pin Number (Sheet 1 of 4)

Pin No.	Pin Name	Signal Buffer Type	Pin No.	Pin Name	Signal Buffer Type
A1	VTT	AGTL+ VTT Supply	B1	EMI	EMI Management
A2	GND	VSS	B2	FLUSH#	CMOS Input
A3	VTT	AGTL+ VTT Supply	B3	SMI#	CMOS Input
A4	IERR#	CMOS Output	B4	INIT#	CMOS Input
A5	A20M#	CMOS Input	B5	VTT	AGTL+ VTT Supply
A6	GND	VSS	B6	STPCLK#	CMOS Input
A7	FERR#	CMOS Output	B7	TCK	TAP Input
A8	IGNNE#	CMOS Input	B8	SLP#	CMOS Input
A9	TDI	TAP Input	B9	VTT	AGTL+ VTT Supply
A10	GND	VSS	B10	TMS	TAP Input
A11	TDO	TAP Output	B11	TRST#	TAP Input
A12	PWRGOOD	CMOS Input	B12	Reserved	Reserved for Future Use
A13	TESTHI	CMOS Test Input	B13	VCC_{CORE}	Processor Core VCC
A14	GND	VSS	B14	THERMDP	Diode Anode (p junction)
A15	THERMTRIP#	CMOS Output	B15	THERMDN	Diode Cathode (n junction)
A16	Reserved	Reserved for Future Use	B16	LINT1/NMI	CMOS Input
A17	LINT0/INTR	CMOS Input	B17	VCC_{CORE}	Processor Core Vcc
A18	GND	VSS	B18	PICCLK	APIC Clock Input
A19	PICD0	CMOS I/O	B19	BP2#	AGTL+ I/O
A20	PREQ#	CMOS Input	B20	Reserved	Reserved for Future Use
A21	BP3#	AGTL+ I/O	B21	BSEL	VSS
A22	GND	VSS	B22	PICD1	CMOS I/O
A23	BPM0#	AGTL+ I/O	B23	PRDY#	AGTL+ Output
A24	Reserved	Reserved for Pentium II processor	B24	BPM1#	AGTL+ I/O
A25	Reserved	Reserved for Pentium II processor	B25	VCC_{CORE}	Processor Core Vcc
A26	GND	VSS	B26	Reserved	Reserved for Pentium II processor
A27	Reserved	Reserved for Pentium II processor	B27	Reserved	Reserved for Pentium II processor
A28	Reserved	Reserved for Pentium II processor	B28	Reserved	Reserved for Pentium II processor
A29	Reserved	Reserved for Pentium II processor	B29	VCC_{CORE}	Processor Core Vcc

Table 32. S.E.P. Package Signal Listing in Order by Pin Number (Sheet 2 of 4)

Pin No.	Pin Name	Signal Buffer Type	Pin No.	Pin Name	Signal Buffer Type
A30	GND	Vss	B30	D62#	AGTL+ I/O
A31	Reserved	Reserved for Pentium II processor	B31	D58#	AGTL+ I/O
A32	D61#	AGTL+ I/O	B32	D63#	AGTL+ I/O
A33	D55#	AGTL+ I/O	B33	$V_{CC_{CORE}}$	Processor Core Vcc
A34	GND	Vss	B34	D56#	AGTL+ I/O
A35	D60#	AGTL+ I/O	B35	D50#	AGTL+ I/O
A36	D53#	AGTL+ I/O	B36	D54#	AGTL+ I/O
A37	D57#	AGTL+ I/O	B37	$V_{CC_{CORE}}$	Processor Core Vcc
A38	GND	Vss	B38	D59#	AGTL+ I/O
A39	D46#	AGTL+ I/O	B39	D48#	AGTL+ I/O
A40	D49#	AGTL+ I/O	B40	D52#	AGTL+ I/O
A41	D51#	AGTL+ I/O	B41	EMI	EMI Management
A42	GND	Vss	B42	D41#	AGTL+ I/O
A43	D42#	AGTL+ I/O	B43	D47#	AGTL+ I/O
A44	D45#	AGTL+ I/O	B44	D44#	AGTL+ I/O
A45	D39#	AGTL+ I/O	B45	$V_{CC_{CORE}}$	Processor Core Vcc
A46	GND	Vss	B46	D36#	AGTL+ I/O
A47	Reserved	Reserved for Future Use	B47	D40#	AGTL+ I/O
A48	D43#	AGTL+ I/O	B48	D34#	AGTL+ I/O
A49	D37#	AGTL+ I/O	B49	$V_{CC_{CORE}}$	Processor Core Vcc
A50	GND	Vss	B50	D38#	AGTL+ I/O
A51	D33#	AGTL+ I/O	B51	D32#	AGTL+ I/O
A52	D35#	AGTL+ I/O	B52	D28#	AGTL+ I/O
A53	D31#	AGTL+ I/O	B53	$V_{CC_{CORE}}$	Processor Core Vcc
A54	GND	Vss	B54	D29#	AGTL+ I/O
A55	D30#	AGTL+ I/O	B55	D26#	AGTL+ I/O
A56	D27#	AGTL+ I/O	B56	D25#	AGTL+ I/O
A57	D24#	AGTL+ I/O	B57	$V_{CC_{CORE}}$	Processor Core Vcc
A58	GND	Vss	B58	D22#	AGTL+ I/O
A59	D23#	AGTL+ I/O	B59	D19#	AGTL+ I/O
A60	D21#	AGTL+ I/O	B60	D18#	AGTL+ I/O
A61	D16#	AGTL+ I/O	B61	EMI	EMI Management
A62	GND	Vss	B62	D20#	AGTL+ I/O
A63	D13#	AGTL+ I/O	B63	D17#	AGTL+ I/O
A64	D11#	AGTL+ I/O	B64	D15#	AGTL+ I/O
A65	D10#	AGTL+ I/O	B65	$V_{CC_{CORE}}$	Processor Core Vcc
A66	GND	Vss	B66	D12#	AGTL+ I/O
A67	D14#	AGTL+ I/O	B67	D7#	AGTL+ I/O
A68	D9#	AGTL+ I/O	B68	D6#	AGTL+ I/O

Table 32. S.E.P. Package Signal Listing in Order by Pin Number (Sheet 3 of 4)

Pin No.	Pin Name	Signal Buffer Type	Pin No.	Pin Name	Signal Buffer Type
A69	D8#	AGTL+ I/O	B69	$V_{CC_{CORE}}$	Processor Core Vcc
A70	GND	Vss	B70	D4#	AGTL+ I/O
A71	D5#	AGTL+ I/O	B71	D2#	AGTL+ I/O
A72	D3#	AGTL+ I/O	B72	D0#	AGTL+ I/O
A73	D1#	AGTL+ I/O	B73	$V_{CC_{CORE}}$	Processor Core Vcc
A74	GND	Vss	B74	RESET#	AGTL+ Input
A75	BCLK	Processor Clock Input	B75	Reserved	Reserved for Future Use
A76	Reserved	Reserved for Pentium II processor	B76	Reserved	Reserved for Future Use
A77	Reserved	Reserved for Pentium II processor	B77	$V_{CC_{CORE}}$	Processor Core Vcc
A78	GND	Vss	B78	Reserved	Reserved for Pentium II processor
A79	Reserved	Reserved for Pentium II processor	B79	Reserved	Reserved for Pentium II processor
A80	Reserved	Reserved for Pentium II processor	B80	A29#	AGTL+ I/O
A81	A30#	AGTL+ I/O	B81	EMI	EMI Management
A82	GND	Vss	B82	A26#	AGTL+ I/O
A83	A31#	AGTL+ I/O	B83	A24#	AGTL+ I/O
A84	A27#	AGTL+ I/O	B84	A28#	AGTL+ I/O
A85	A22#	AGTL+ I/O	B85	$V_{CC_{CORE}}$	Processor Core Vcc
A86	GND	Vss	B86	A20#	AGTL+ I/O
A87	A23#	AGTL+ I/O	B87	A21#	AGTL+ I/O
A88	Reserved	Reserved for Future Use	B88	A25#	AGTL+ I/O
A89	A19#	AGTL+ I/O	B89	$V_{CC_{CORE}}$	Processor Core Vcc
A90	GND	Vss	B90	A15#	AGTL+ I/O
A91	A18#	AGTL+ I/O	B91	A17#	AGTL+ I/O
A92	A16#	AGTL+ I/O	B92	A11#	AGTL+ I/O
A93	A13#	AGTL+ I/O	B93	$V_{CC_{CORE}}$	Processor Core Vcc
A94	GND	Vss	B94	A12#	AGTL+ I/O
A95	A14#	AGTL+ I/O	B95	A8#	AGTL+ I/O
A96	A10#	AGTL+ I/O	B96	A7#	AGTL+ I/O
A97	A5#	AGTL+ I/O	B97	$V_{CC_{CORE}}$	Processor Core Vcc
A98	GND	Vss	B98	A3#	AGTL+ I/O
A99	A9#	AGTL+ I/O	B99	A6#	AGTL+ I/O
A100	A4#	AGTL+ I/O	B100	EMI	EMI Management
A101	BNR#	AGTL+ I/O	B101	SLOTOCC#	SC242 Occupied
A102	GND	Vss	B102	REQ0#	AGTL+ I/O
A103	BPRI#	AGTL+ Input	B103	REQ1#	AGTL+ I/O
A104	TRDY#	AGTL+ Input	B104	REQ4#	AGTL+ I/O
A105	DEFER#	AGTL+ Input	B105	$V_{CC_{CORE}}$	Processor Core Vcc

Table 32. S.E.P. Package Signal Listing in Order by Pin Number (Sheet 4 of 4)

Pin No.	Pin Name	Signal Buffer Type	Pin No.	Pin Name	Signal Buffer Type
A106	GND	Vss	B106	LOCK#	AGTL+ I/O
A107	REQ2#	AGTL+ I/O	B107	DRDY#	AGTL+ I/O
A108	REQ3#	AGTL+ I/O	B108	RS0#	AGTL+ Input
A109	HITM#	AGTL+ I/O	B109	V_{CC_5}	Other Vcc
A110	GND	Vss	B110	HIT#	AGTL+ I/O
A111	DBSY#	AGTL+ I/O	B111	RS2#	AGTL+ Input
A112	RS1#	AGTL+ Input	B112	Reserved	Reserved for Future Use
A113	Reserved	Reserved for Future Use	B113	$V_{CC_{L2}}$	Reserved for Pentium II processor
A114	GND	Vss	B114	Reserved	Reserved for Pentium II processor
A115	ADS#	AGTL+ I/O	B115	Reserved	Reserved for Pentium II processor
A116	Reserved	Reserved for Future Use	B116	Reserved	Reserved for Pentium II processor
A117	Reserved	Reserved for Pentium II processor	B117	$V_{CC_{L2}}$	Reserved for Pentium II processor
A118	GND	Vss	B118	Reserved	Reserved for Pentium II processor
A119	VID2	Voltage Identification	B119	VID3	Voltage Identification
A120	VID1	Voltage Identification	B120	VID0	Voltage Identification
A121	VID4	Voltage Identification	B121	$V_{CC_{L2}}$	Reserved for Pentium II processor

Table 33 is the Intel® Celeron™ processor substrate edge connector listing in order by signal name.

Table 33. S.E.P. Package Signal Listing in Order by Signal Name (Sheet 1 of 4)

Pin No.	Pin Name	Signal Buffer Type	Pin No.	Pin Name	Signal Buffer Type
B98	A3#	AGTL+ I/O	A21	BP3#	AGTL+ I/O
A100	A4#	AGTL+ I/O	A23	BPM0#	AGTL+ I/O
A97	A5#	AGTL+ I/O	B24	BPM1#	AGTL+ I/O
B99	A6#	AGTL+ I/O	A103	BPRI#	AGTL+ Input
B96	A7#	AGTL+ I/O	B21	BSEL	Vss
B95	A8#	AGTL+ I/O	B72	D0#	AGTL+ I/O
A99	A9#	AGTL+ I/O	A73	D1#	AGTL+ I/O
A96	A10#	AGTL+ I/O	B71	D2#	AGTL+ I/O
B92	A11#	AGTL+ I/O	A72	D3#	AGTL+ I/O
B94	A12#	AGTL+ I/O	B70	D4#	AGTL+ I/O
A93	A13#	AGTL+ I/O	A71	D5#	AGTL+ I/O
A95	A14#	AGTL+ I/O	B68	D6#	AGTL+ I/O
B90	A15#	AGTL+ I/O	B67	D7#	AGTL+ I/O
A92	A16#	AGTL+ I/O	A69	D8#	AGTL+ I/O
B91	A17#	AGTL+ I/O	A68	D9#	AGTL+ I/O
A91	A18#	AGTL+ I/O	A65	D10#	AGTL+ I/O
A89	A19#	AGTL+ I/O	A64	D11#	AGTL+ I/O
B86	A20#	AGTL+ I/O	B66	D12#	AGTL+ I/O
B87	A21#	AGTL+ I/O	A63	D13#	AGTL+ I/O
A85	A22#	AGTL+ I/O	A67	D14#	AGTL+ I/O
A87	A23#	AGTL+ I/O	B64	D15#	AGTL+ I/O
B83	A24#	AGTL+ I/O	A61	D16#	AGTL+ I/O
B88	A25#	AGTL+ I/O	B63	D17#	AGTL+ I/O
B82	A26#	AGTL+ I/O	B60	D18#	AGTL+ I/O
A84	A27#	AGTL+ I/O	B59	D19#	AGTL+ I/O
B84	A28#	AGTL+ I/O	B62	D20#	AGTL+ I/O
B80	A29#	AGTL+ I/O	A60	D21#	AGTL+ I/O
A81	A30#	AGTL+ I/O	B58	D22#	AGTL+ I/O
A83	A31#	AGTL+ I/O	A59	D23#	AGTL+ I/O
A5	A20M#	CMOS Input	A57	D24#	AGTL+ I/O
A115	ADS#	AGTL+ I/O	B56	D25#	AGTL+ I/O
A75	BCLK	Processor Clock Input	B55	D26#	AGTL+ I/O
A101	BNR#	AGTL+ I/O	A56	D27#	AGTL+ I/O
B19	BP2#	AGTL+ I/O	B52	D28#	AGTL+ I/O

Table 33. S.E.P. Package Signal Listing in Order by Signal Name (Sheet 2 of 4)

Pin No.	Pin Name	Signal Buffer Type	Pin No.	Pin Name	Signal Buffer Type
B54	D29#	AGTL+ I/O	A111	DBSY#	AGTL+ I/O
A55	D30#	AGTL+ I/O	A105	DEFER#	AGTL+ Input
A53	D31#	AGTL+ I/O	B107	DRDY#	AGTL+ I/O
B51	D32#	AGTL+ I/O	B1	EMI	EMI Management
A51	D33#	AGTL+ I/O	B41	EMI	EMI Management
B48	D34#	AGTL+ I/O	B61	EMI	EMI Management
A52	D35#	AGTL+ I/O	B81	EMI	EMI Management
B46	D36#	AGTL+ I/O	B100	EMI	EMI Management
A49	D37#	AGTL+ I/O	A7	FERR#	CMOS Output
B50	D38#	AGTL+ I/O	B2	FLUSH#	CMOS Input
A45	D39#	AGTL+ I/O	A38	GND	Vss
B47	D40#	AGTL+ I/O	A42	GND	Vss
B42	D41#	AGTL+ I/O	A50	GND	Vss
A43	D42#	AGTL+ I/O	A54	GND	Vss
A48	D43#	AGTL+ I/O	A58	GND	Vss
B44	D44#	AGTL+ I/O	A62	GND	Vss
A44	D45#	AGTL+ I/O	A66	GND	Vss
A39	D46#	AGTL+ I/O	A70	GND	Vss
B43	D47#	AGTL+ I/O	A74	GND	Vss
B39	D48#	AGTL+ I/O	A78	GND	Vss
A40	D49#	AGTL+ I/O	A82	GND	Vss
B35	D50#	AGTL+ I/O	A86	GND	Vss
A41	D51#	AGTL+ I/O	A2	GND	Vss
B40	D52#	AGTL+ I/O	A6	GND	Vss
A36	D53#	AGTL+ I/O	A10	GND	Vss
B36	D54#	AGTL+ I/O	A14	GND	Vss
A33	D55#	AGTL+ I/O	A18	GND	Vss
B34	D56#	AGTL+ I/O	A22	GND	Vss
A37	D57#	AGTL+ I/O	A26	GND	Vss
B31	D58#	AGTL+ I/O	A30	GND	Vss
B38	D59#	AGTL+ I/O	A34	GND	Vss
A35	D60#	AGTL+ I/O	A98	GND	Vss
A32	D61#	AGTL+ I/O	A102	GND	Vss
B30	D62#	AGTL+ I/O	A106	GND	Vss
B32	D63#	AGTL+ I/O	A110	GND	Vss

Table 33. S.E.P. Package Signal Listing in Order by Signal Name (Sheet 3 of 4)

Pin No.	Pin Name	Signal Buffer Type	Pin No.	Pin Name	Signal Buffer Type
A114	GND	Vss	A116	Reserved	Reserved for Future Use
A118	GND	Vss	B12	Reserved	Reserved for Future Use
A46	GND	Vss	A113	Reserved	Reserved for Future Use
B110	HIT#	AGTL+ I/O	B20	Reserved	Reserved for Future Use
A109	HITM#	AGTL+ I/O	B76	Reserved	Reserved for Future Use
A4	IERR#	CMOS Output	B112	Reserved	Reserved for Future Use
A8	IGNNE#	CMOS Input	B79	Reserved	Reserved for Pentium II processor
B4	INIT#	CMOS Input	B114	Reserved	Reserved for Pentium II processor
A17	LINT0/INTR	CMOS Input	B115	Reserved	Reserved for Pentium II processor
B16	LINT1/NMI	CMOS Input	A117	Reserved	Reserved for Pentium II processor
B106	LOCK#	AGTL+ I/O	B116	Reserved	Reserved for Pentium II processor
B18	PICCLK	APIC Clock Input	A24	Reserved	Reserved for Pentium II processor
A19	PICD0	CMOS I/O	A76	Reserved	Reserved for Pentium II processor
B22	PICD1	CMOS I/O	B75	Reserved	Reserved for Future Use
B23	PRDY#	AGTL+ Output	A79	Reserved	Reserved for Pentium II processor
A20	PREQ#	CMOS Input	A80	Reserved	Reserved for Pentium II processor
A12	PWRGOOD	CMOS Input	B78	Reserved	Reserved for Pentium II processor
B102	REQ0#	AGTL+ I/O	B118	Reserved	Reserved for Pentium II processor
B103	REQ1#	AGTL+ I/O	A25	Reserved	Reserved for Pentium II processor
A107	REQ2#	AGTL+ I/O	A27	Reserved	Reserved for Pentium II processor
A108	REQ3#	AGTL+ I/O	B26	Reserved	Reserved for Pentium II processor
B104	REQ4#	AGTL+ I/O	A28	Reserved	Reserved for Pentium II processor
A16	Reserved	Reserved for Future Use	B27	Reserved	Reserved for Pentium II processor
A47	Reserved	Reserved for Future Use	A29	Reserved	Reserved for Pentium II processor
A77	Reserved	Reserved for Pentium II processor	A31	Reserved	Reserved for Pentium II processor
A88	Reserved	Reserved for Future Use	B28	Reserved	Reserved for Pentium II processor

Table 33. S.E.P. Package Signal Listing in Order by Signal Name (Sheet 4 of 4)

Pin No.	Pin Name	Signal Buffer Type	Pin No.	Pin Name	Signal Buffer Type
B74	RESET#	AGTL+ Input	B49	$V_{CC_{CORE}}$	Processor Core Vcc
B108	RS0#	AGTL+ Input	B53	$V_{CC_{CORE}}$	Processor Core Vcc
A112	RS1#	AGTL+ Input	B57	$V_{CC_{CORE}}$	Processor Core Vcc
B111	RS2#	AGTL+ Input	B65	$V_{CC_{CORE}}$	Processor Core Vcc
B101	SLOTOCC#	SC242 Occupied	B69	$V_{CC_{CORE}}$	Processor Core Vcc
B8	SLP#	CMOS Input	B73	$V_{CC_{CORE}}$	Processor Core Vcc
B3	SMI#	CMOS Input	B77	$V_{CC_{CORE}}$	Processor Core Vcc
B6	STPCLK#	CMOS Input	B85	$V_{CC_{CORE}}$	Processor Core Vcc
B7	TCK	TAP Input	B89	$V_{CC_{CORE}}$	Processor Core Vcc
A9	TDI	TAP Input	B93	$V_{CC_{CORE}}$	Processor Core Vcc
A11	TDO	TAP Output	B97	$V_{CC_{CORE}}$	Processor Core Vcc
A13	TESTHI	CMOS Test Input	B105	$V_{CC_{CORE}}$	Processor Core Vcc
B14	THERMDP	Diode Anode (p junction)	B113	$V_{CC_{L2}}$	Reserved for Pentium II processor
B15	THERMDN	Diode Cathode (n junction)	B117	$V_{CC_{L2}}$	Reserved for Pentium II processor
A15	THERMTRIP#	CMOS Output	B121	$V_{CC_{L2}}$	Reserved for Pentium II processor
B10	TMS	TAP Input	A1	V_{TT}	AGTL+ V_{TT} Supply
A104	TRDY#	AGTL+ Input	A3	V_{TT}	AGTL+ V_{TT} Supply
B11	TRST#	TAP Input	B5	V_{TT}	AGTL+ V_{TT} Supply
B13	$V_{CC_{CORE}}$	Processor Core Vcc	B9	V_{TT}	AGTL+ V_{TT} Supply
B17	$V_{CC_{CORE}}$	Processor Core Vcc	B109	V_{CC_5}	Other VCC
B25	$V_{CC_{CORE}}$	Processor Core Vcc	B120	VID0	Voltage Identification
B29	$V_{CC_{CORE}}$	Processor Core Vcc	A120	VID1	Voltage Identification
B33	$V_{CC_{CORE}}$	Processor Core Vcc	A119	VID2	Voltage Identification
B37	$V_{CC_{CORE}}$	Processor Core Vcc	B119	VID3	Voltage Identification
B45	$V_{CC_{CORE}}$	Processor Core Vcc	A121	VID4	Voltage Identification

5.2 PPGA Package

This section defines the mechanical specifications and signal definitions for the Intel® Celeron™ processor in the PPGA package.

5.2.1 Materials Information

Figure 16 and Table 34 are provided to aid in the design of a heatsink and clip.

Figure 16. PPGA Package Dimensions

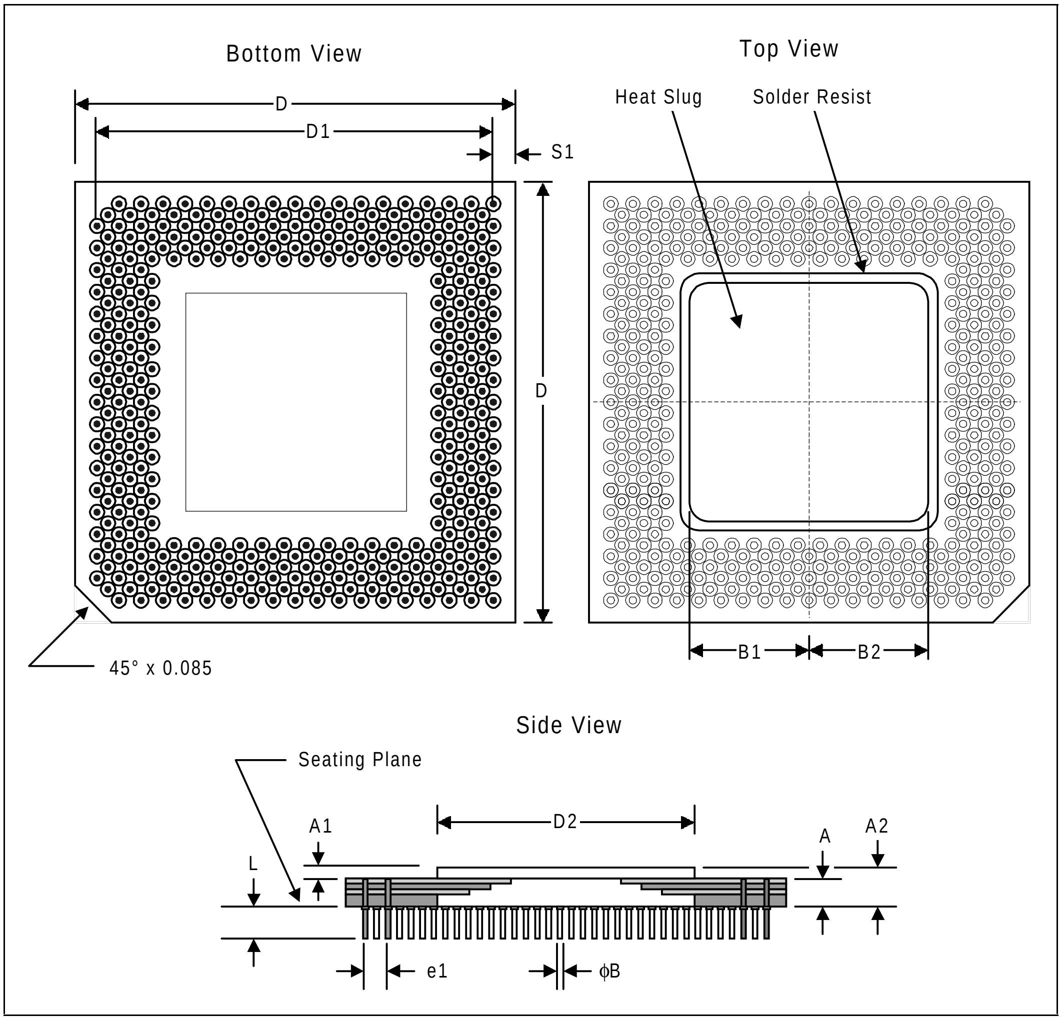


Table 34. PPGA Package Dimensions

Symbol	Millimeters			Inches		
	Min	Max	Notes	Min	Max	Notes
A	1.83	2.23		0.072	0.088	
A_1	1.00			0.039		
A_2	2.72	3.33		0.107	0.131	
B	0.40	0.51		0.016	0.020	
D	49.43	49.63		1.946	1.954	
D_1	45.59	45.85		1.795	1.805	
D_2	25.15	25.65		0.099	1.010	
e_1	2.29	2.79		0.090	0.110	
L	3.05	3.30		0.120	0.130	
N	370		Lead Count	370		Lead Count
S_1	1.52	2.54		0.060	0.100	

Table 35. PPGA Package Information Summary

Package Type	Total Pins	Pin Array	Package Size
Plastic Staggered Pin Grid Array (PPGA)	370	37 x 37	1.95" x 1.95" 4.95 cm x 4.95 cm

5.2.2 Signal Listing

Figure 17. PPGA Package (Pin Side View)

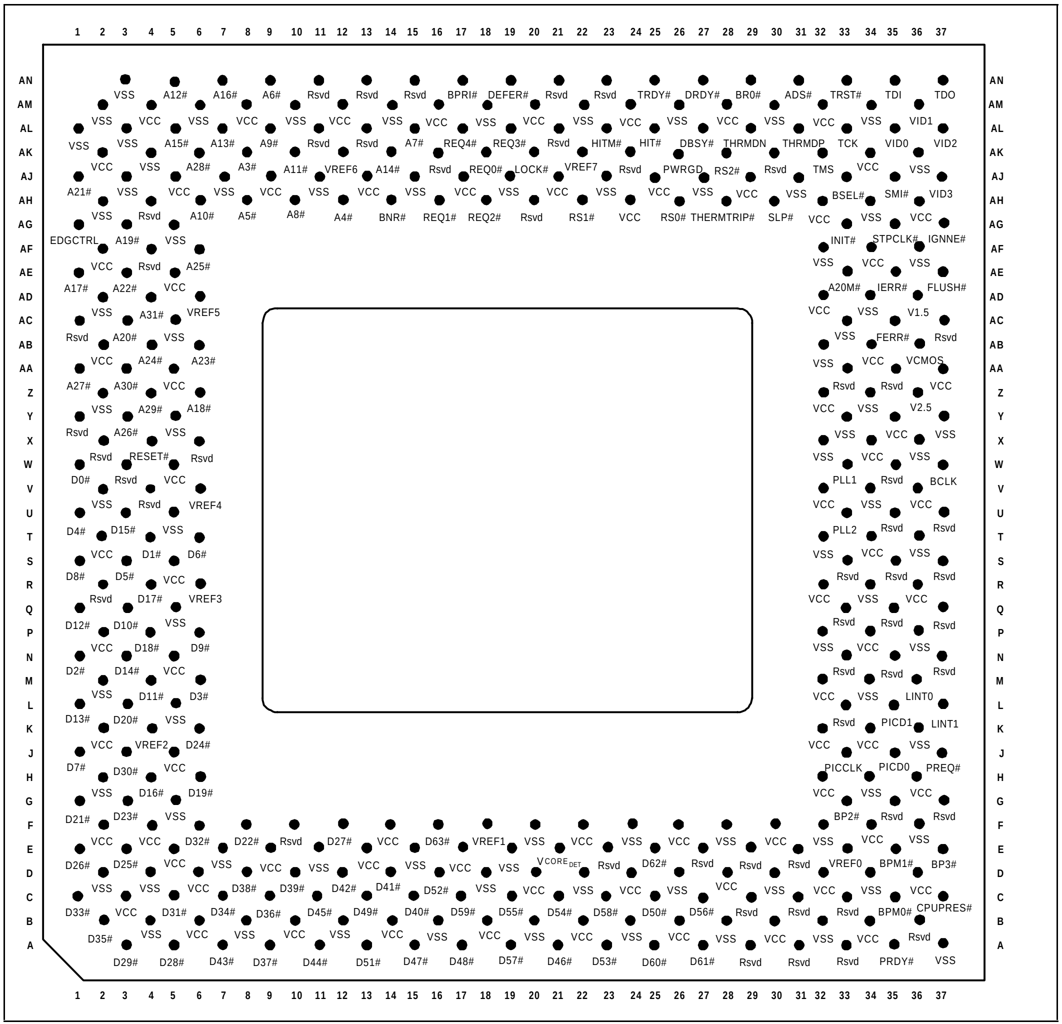


Table 36. PPGA Package Signal Listing in Order by Pin Number (Sheet 1 of 6)

Pin No.	Pin Name	Signal Buffer Type	Pin No.	Pin Name	Signal Buffer Type
A3	D29#	AGTL+ I/O	AC37	Reserved	Reserved for Future Use
A5	D28#	AGTL+ I/O	AD2	GND	Vss
A7	D43#	AGTL+ I/O	AD4	A31#	AGTL+ I/O
A9	D37#	AGTL+ I/O	AD6	V_{REF5}	AGTL+ Reference Voltage
A11	D44#	AGTL+ I/O	AD32	$V_{CC_{CORE}}$	Processor Core Vcc
A13	D51#	AGTL+ I/O	AD34	GND	Vss
A15	D47#	AGTL+ I/O	AD36	$V_{CC_{1.5}}$	1.5V CMOS Input
A17	D48#	AGTL+ I/O	AE1	A17#	AGTL+ I/O
A19	D57#	AGTL+ I/O	AE3	A22#	AGTL+ I/O
A21	D46#	AGTL+ I/O	AE5	$V_{CC_{CORE}}$	Processor Core Vcc
A23	D53#	AGTL+ I/O	AE33	A20M#	CMOS Input
A25	D60#	AGTL+ I/O	AE35	IERR#	CMOS Output
A27	D61#	AGTL+ I/O	AE37	FLUSH#	CMOS Input
A29	Reserved	Reserved for Future Use	AF2	$V_{CC_{CORE}}$	Processor Core Vcc
A31	Reserved	Reserved for Future Use	AF4	Reserved	Reserved for Future Use
A33	Reserved	Reserved for Future Use	AF6	A25#	AGTL+ I/O
A35	PRDY#	AGTL+ Output	AF32	GND	Vss
A37	GND	Vss	AF34	$V_{CC_{CORE}}$	Processor Core Vcc
AA1	A27#	AGTL+ I/O	AF36	GND	Vss
AA3	A30#	AGTL+ I/O	AG1	EDGCTRL	AGTL+ Edge Control Input
AA5	$V_{CC_{CORE}}$	Processor Core Vcc	AG3	A19#	AGTL+ I/O
AA33	Reserved	Reserved for Future Use	AG5	GND	Vss
AA35	Reserved	Reserved for Future Use	AG33	INIT#	CMOS Input
AA37	$V_{CC_{CORE}}$	Processor Core Vcc	AG35	STPCLK#	CMOS Input
AB2	$V_{CC_{CORE}}$	Processor Core Vcc	AG37	IGNNE#	CMOS Input
AB4	A24#	AGTL+ I/O	AH2	GND	Vss
AB6	A23#	AGTL+ I/O	AH4	Reserved	Reserved for Future Use
AB32	GND	Vss	AH6	A10#	AGTL+ I/O
AB34	$V_{CC_{CORE}}$	Processor Core Vcc	AH8	A5#	AGTL+ I/O
AB36	$V_{CC_{CMOS}}$	CMOS Voltage Output	AH10	A8#	AGTL+ I/O
AC1	Reserved	Reserved for Future Use	AH12	A4#	AGTL+ I/O
AC3	A20#	AGTL+ I/O	AH14	BNR#	AGTL+ I/O
AC5	GND	Vss	AH16	REQ1#	AGTL+ I/O
AC33	GND	Vss	AH18	REQ2#	AGTL+ I/O
AC35	FERR#	CMOS Output	AH20	Reserved	Reserved for Future Use

Table 36. PPGA Package Signal Listing in Order by Pin Number (Sheet 2 of 6)

Pin No.	Pin Name	Signal Buffer Type	Pin No.	Pin Name	Signal Buffer Type
AH22	RS1#	AGTL+ Input	AK18	REQ0#	AGTL+ I/O
AH24	$V_{CC_{CORE}}$	Processor Core Vcc	AK20	LOCK#	AGTL+ I/O
AH26	RS0#	AGTL+ Input	AK22	V_{REF_7}	AGTL+ Reference Voltage
AH28	THERMTRIP#	CMOS Output	AK24	Reserved	Reserved for Future Use
AH30	SLP#	CMOS Input	AK26	PWRGOOD	CMOS Input
AH32	$V_{CC_{CORE}}$	Processor Core Vcc	AK28	RS2#	AGTL+ Input
AH34	GND	Vss	AK30	Reserved	Reserved for Future Use
AH36	$V_{CC_{CORE}}$	Processor Core Vcc	AK32	TMS	TAP Input
AJ1	A21#	AGTL+ I/O	AK34	$V_{CC_{CORE}}$	Processor Core Vcc
AJ3	GND	Vss	AK36	GND	Vss
AJ5	$V_{CC_{CORE}}$	Processor Core Vcc	AL1	GND	Vss
AJ7	GND	Vss	AL3	GND	Vss
AJ9	$V_{CC_{CORE}}$	Processor Core Vcc	AL5	A15#	AGTL+ I/O
AJ11	GND	Vss	AL7	A13#	AGTL+ I/O
AJ13	$V_{CC_{CORE}}$	Processor Core Vcc	AL9	A9#	AGTL+ I/O
AJ15	GND	Vss	AL11	Reserved	Reserved for Future Use
AJ17	$V_{CC_{CORE}}$	Processor Core Vcc	AL13	Reserved	Reserved for Future Use
AJ19	GND	Vss	AL15	A7#	AGTL+ I/O
AJ21	$V_{CC_{CORE}}$	Processor Core Vcc	AL17	REQ4#	AGTL+ I/O
AJ23	GND	Vss	AL19	REQ3#	AGTL+ I/O
AJ25	$V_{CC_{CORE}}$	Processor Core Vcc	AL21	Reserved	Reserved for Future Use
AJ27	GND	Vss	AL23	HITM#	AGTL+ I/O
AJ29	$V_{CC_{CORE}}$	Processor Core Vcc	AL25	HIT#	AGTL+ I/O
AJ31	GND	Vss	AL27	DBSY#	AGTL+ I/O
AJ33	BSEL	CMOS Output	AL29	THERMDN	Thermal Diode Cathode
AJ35	SMI#	CMOS Input	AL31	THERMDP	Thermal Diode Anode
AJ37	VID3	Voltage Identification	AL33	TCK	TAP Input
AK2	$V_{CC_{CORE}}$	Processor Core Vcc	AL35	VID0	Voltage Identification
AK4	GND	Vss	AL37	VID2	Voltage Identification
AK6	A28#	AGTL+ I/O	AM2	GND	Vss
AK8	A3#	AGTL+ I/O	AM4	$V_{CC_{CORE}}$	Processor Core Vcc
AK10	A11#	AGTL+ I/O	AM6	GND	Vss
AK12	V_{REF_6}	AGTL+ Reference Voltage	AM8	$V_{CC_{CORE}}$	Processor Core Vcc
AK14	A14#	AGTL+ I/O	AM10	GND	Vss
AK16	Reserved	Reserved for Future Use	AM12	$V_{CC_{CORE}}$	Processor Core Vcc

Table 36. PPGA Package Signal Listing in Order by Pin Number (Sheet 3 of 6)

Pin No.	Pin Name	Signal Buffer Type	Pin No.	Pin Name	Signal Buffer Type
AM14	GND	Vss	B12	GND	Vss
AM16	$V_{CC_{CORE}}$	Processor Core Vcc	B14	$V_{CC_{CORE}}$	Processor Core Vcc
AM18	GND	Vss	B16	GND	Vss
AM20	$V_{CC_{CORE}}$	Processor Core Vcc	B18	$V_{CC_{CORE}}$	Processor Core Vcc
AM22	GND	Vss	B20	GND	Vss
AM24	$V_{CC_{CORE}}$	Processor Core Vcc	B22	$V_{CC_{CORE}}$	Processor Core Vcc
AM26	GND	Vss	B24	GND	Vss
AM28	$V_{CC_{CORE}}$	Processor Core Vcc	B26	$V_{CC_{CORE}}$	Processor Core Vcc
AM30	GND	Vss	B28	GND	Vss
AM32	$V_{CC_{CORE}}$	Processor Core Vcc	B30	$V_{CC_{CORE}}$	Processor Core Vcc
AM34	GND	Vss	B32	GND	Vss
AM36	VID1	Voltage Identification	B34	$V_{CC_{CORE}}$	Processor Core Vcc
AN3	GND	Vss	B36	Reserved	Reserved for Future Use
AN5	A12#	AGTL+ I/O	C1	D33#	AGTL+ I/O
AN7	A16#	AGTL+ I/O	C3	$V_{CC_{CORE}}$	Processor Core Vcc
AN9	A6#	AGTL+ I/O	C5	D31#	AGTL+ I/O
AN11	Reserved	Reserved for Future Use	C7	D34#	AGTL+ I/O
AN13	Reserved	Reserved for Future Use	C9	D36#	AGTL+ I/O
AN15	Reserved	Reserved for Future Use	C11	D45#	AGTL+ I/O
AN17	BPRI#	AGTL+ Input	C13	D49#	AGTL+ I/O
AN19	DEFER#	AGTL+ Input	C15	D40#	AGTL+ I/O
AN21	Reserved	Reserved for Future Use	C17	D59#	AGTL+ I/O
AN23	Reserved	Reserved for Future Use	C19	D55#	AGTL+ I/O
AN25	TRDY#	AGTL+ Input	C21	D54#	AGTL+ I/O
AN27	DRDY#	AGTL+ I/O	C23	D58#	AGTL+ I/O
AN29	BR0#	AGTL+ I/O	C25	D50#	AGTL+ I/O
AN31	ADS#	AGTL+ I/O	C27	D56#	AGTL+ I/O
AN33	TRST#	TAP Input	C29	Reserved	Reserved for Future Use
AN35	TDI	TAP Input	C31	Reserved	Reserved for Future Use
AN37	TDO	TAP Output	C33	Reserved	Reserved for Future Use
B2	D35#	AGTL+ I/O	C35	BPM0#	AGTL+ I/O
B4	GND	Vss	C37	CPUPRES#	CPU Present
B6	$V_{CC_{CORE}}$	Processor Core Vcc	D2	GND	Vss
B8	GND	Vss	D4	GND	Vss
B10	$V_{CC_{CORE}}$	Processor Core Vcc	D6	$V_{CC_{CORE}}$	Processor Core Vcc

Table 36. PPGA Package Signal Listing in Order by Pin Number (Sheet 4 of 6)

Pin No.	Pin Name	Signal Buffer Type	Pin No.	Pin Name	Signal Buffer Type
D8	D38#	AGTL+ I/O	F4	$V_{CC_{CORE}}$	Processor Core Vcc
D10	D39#	AGTL+ I/O	F6	D32#	AGTL+ I/O
D12	D42#	AGTL+ I/O	F8	D22#	AGTL+ I/O
D14	D41#	AGTL+ I/O	F10	Reserved	Reserved for Future Use
D16	D52#	AGTL+ I/O	F12	D27#	AGTL+ I/O
D18	GND	Vss	F14	$V_{CC_{CORE}}$	Processor Core Vcc
D20	$V_{CC_{CORE}}$	Processor Core Vcc	F16	D63#	AGTL+ I/O
D22	GND	Vss	F18	V_{REF_1}	AGTL+ Reference Voltage
D24	$V_{CC_{CORE}}$	Processor Core Vcc	F20	GND	Vss
D26	GND	Vss	F22	$V_{CC_{CORE}}$	Processor Core Vcc
D28	$V_{CC_{CORE}}$	Processor Core Vcc	F24	GND	Vss
D30	GND	Vss	F26	$V_{CC_{CORE}}$	Processor Core Vcc
D32	$V_{CC_{CORE}}$	Processor Core Vcc	F28	GND	Vss
D34	GND	Vss	F30	$V_{CC_{CORE}}$	Processor Core Vcc
D36	$V_{CC_{CORE}}$	Processor Core Vcc	F32	GND	Vss
E1	D26#	AGTL+ I/O	F34	$V_{CC_{CORE}}$	Processor Core Vcc
E3	D25#	AGTL+ I/O	F36	GND	Vss
E5	$V_{CC_{CORE}}$	Processor Core Vcc	G1	D21#	AGTL+ I/O
E7	GND	Vss	G3	D23#	AGTL+ I/O
E9	$V_{CC_{CORE}}$	Processor Core Vcc	G5	GND	Vss
E11	GND	Vss	G33	BP2#	AGTL+ I/O
E13	$V_{CC_{CORE}}$	Processor Core Vcc	G35	Reserved	Reserved for Future Use
E15	GND	Vss	G37	Reserved	Reserved for Future Use
E17	$V_{CC_{CORE}}$	Processor Core Vcc	H2	GND	Vss
E19	GND	Vss	H4	D16#	AGTL+ I/O
E21	$V_{CORE_{DET}}$	Future Processor Detection	H6	D19#	AGTL+ I/O
E23	Reserved	Reserved for Future Use	H32	$V_{CC_{CORE}}$	Processor Core Vcc
E25	D62#	AGTL+ I/O	H34	GND	Vss
E27	Reserved	Reserved for Future Use	H36	$V_{CC_{CORE}}$	Processor Core Vcc
E29	Reserved	Reserved for Future Use	J1	D7#	AGTL+ I/O
E31	Reserved	Reserved for Future Use	J3	D30#	AGTL+ I/O
E33	V_{REF_0}	AGTL+ Reference Voltage	J5	$V_{CC_{CORE}}$	Processor Core Vcc
E35	BPM1#	AGTL+ I/O	J33	PICCLK	APIC Clock Input
E37	BP3#	AGTL+ I/O	J35	PICD0	CMOS I/O
F2	$V_{CC_{CORE}}$	Processor Core Vcc	J37	PREQ#	CMOS Input

Table 36. PPGA Package Signal Listing in Order by Pin Number (Sheet 5 of 6)

Pin No.	Pin Name	Signal Buffer Type	Pin No.	Pin Name	Signal Buffer Type
K2	VCC_{CORE}	Processor Core Vcc	Q37	Reserved	Reserved for Future Use
K4	$VREF_2$	AGTL+ Reference Voltage	R2	Reserved	Reserved for Future Use
K6	D24#	AGTL+ I/O	R4	D17#	AGTL+ I/O
K32	VCC_{CORE}	Processor Core Vcc	R6	$VREF_3$	AGTL+ Reference Voltage
K34	VCC_{CORE}	Processor Core Vcc	R32	VCC_{CORE}	Processor Core Vcc
K36	GND	Vss	R34	GND	Vss
L1	D13#	AGTL+ I/O	R36	VCC_{CORE}	Processor Core Vcc
L3	D20#	AGTL+ I/O	S1	D8#	AGTL+ I/O
L5	GND	Vss	S3	D5#	AGTL+ I/O
L33	Reserved	Reserved for Future Use	S5	VCC_{CORE}	Processor Core Vcc
L35	PICD1	CMOS I/O	S33	Reserved	Reserved for Future Use
L37	LINT1/NMI	CMOS Input	S35	Reserved	Reserved for Future Use
M2	GND	Vss	S37	Reserved	Reserved for Future Use
M4	D11#	AGTL+ I/O	T2	VCC_{CORE}	Processor Core Vcc
M6	D3#	AGTL+ I/O	T4	D1#	AGTL+ I/O
M32	VCC_{CORE}	Processor Core Vcc	T6	D6#	AGTL+ I/O
M34	GND	Vss	T32	GND	Vss
M36	LINT0/INTR	CMOS Input	T34	VCC_{CORE}	Processor Core Vcc
N1	D2#	AGTL+ I/O	T36	GND	Vss
N3	D14#	AGTL+ I/O	U1	D4#	AGTL+ I/O
N5	VCC_{CORE}	Processor Core Vcc	U3	D15#	AGTL+ I/O
N33	Reserved	Reserved for Future Use	U5	GND	Vss
N35	Reserved	Reserved for Future Use	U33	PLL2	PLL Analog Decoupling
N37	Reserved	Reserved for Future Use	U35	Reserved	Reserved for Future Use
P2	VCC_{CORE}	Processor Core Vcc	U37	Reserved	Reserved for Future Use
P4	D18#	AGTL+ I/O	V2	GND	Vss
P6	D9#	AGTL+ I/O	V4	Reserved	Reserved for Future Use
P32	GND	Vss	V6	$VREF_4$	AGTL+ Reference Voltage
P34	VCC_{CORE}	Processor Core Vcc	V32	VCC_{CORE}	Processor Core Vcc
P36	GND	Vss	V34	GND	Vss
Q1	D12#	AGTL+ I/O	V36	VCC_{CORE}	Processor Core Vcc
Q3	D10#	AGTL+ I/O	W1	D0#	AGTL+ I/O
Q5	GND	Vss	W3	Reserved	Reserved for Future Use
Q33	Reserved	Reserved for Future Use	W5	VCC_{CORE}	Processor Core Vcc
Q35	Reserved	Reserved for Future Use	W33	PLL1	PLL Analog Decoupling

Table 36. PPGA Package Signal Listing in Order by Pin Number (Sheet 6 of 6)

Pin No.	Pin Name	Signal Buffer Type	Pin No.	Pin Name	Signal Buffer Type
W35	Reserved	Reserved for Future Use	Y5	GND	Vss
W37	BCLK	Processor Clock Input	Y33	GND	Vss
X2	Reserved	Reserved for Future Use	Y35	$V_{CC_{CORE}}$	Processor Core Vcc
X4	RESET#	AGTL+ Input	Y37	GND	Vss
X6	Reserved	Reserved for Future Use	Z2	GND	Vss
X32	GND	Vss	Z4	A29#	AGTL+ I/O
X34	$V_{CC_{CORE}}$	Processor Core Vcc	Z6	A18#	AGTL+ I/O
X36	GND	Vss	Z32	$V_{CC_{CORE}}$	Processor Core Vcc
Y1	Reserved	Reserved for Future Use	Z34	GND	Vss
Y3	A26#	AGTL+ I/O	Z36	$V_{CC_{2.5}}$	2.5V CMOS Input

Table 37. PPGA Package Signal Listing in Order by Signal Name (Sheet 1 of 5)

Pin No.	Pin Name	Signal Buffer Type	Pin No.	Pin Name	Signal Buffer Type
AK8	A3#	AGTL+ I/O	E37	BP3#	AGTL+ I/O
AH12	A4#	AGTL+ I/O	C35	BPM0#	AGTL+ I/O
AH8	A5#	AGTL+ I/O	E35	BPM1#	AGTL+ I/O
AN9	A6#	AGTL+ I/O	AN17	BPRI#	AGTL+ Input
AL15	A7#	AGTL+ I/O	AN29	BR0#	AGTL+ I/O
AH10	A8#	AGTL+ I/O	AJ33	BSEL	CMOS Output
AL9	A9#	AGTL+ I/O	C37	CPUPRES#	CPU Present
AH6	A10#	AGTL+ I/O	W1	D0#	AGTL+ I/O
AK10	A11#	AGTL+ I/O	T4	D1#	AGTL+ I/O
AN5	A12#	AGTL+ I/O	N1	D2#	AGTL+ I/O
AL7	A13#	AGTL+ I/O	M6	D3#	AGTL+ I/O
AK14	A14#	AGTL+ I/O	U1	D4#	AGTL+ I/O
AL5	A15#	AGTL+ I/O	S3	D5#	AGTL+ I/O
AN7	A16#	AGTL+ I/O	T6	D6#	AGTL+ I/O
AE1	A17#	AGTL+ I/O	J1	D7#	AGTL+ I/O
Z6	A18#	AGTL+ I/O	S1	D8#	AGTL+ I/O
AG3	A19#	AGTL+ I/O	P6	D9#	AGTL+ I/O
AC3	A20#	AGTL+ I/O	Q3	D10#	AGTL+ I/O
AJ1	A21#	AGTL+ I/O	M4	D11#	AGTL+ I/O
AE3	A22#	AGTL+ I/O	Q1	D12#	AGTL+ I/O
AB6	A23#	AGTL+ I/O	L1	D13#	AGTL+ I/O
AB4	A24#	AGTL+ I/O	N3	D14#	AGTL+ I/O
AF6	A25#	AGTL+ I/O	U3	D15#	AGTL+ I/O
Y3	A26#	AGTL+ I/O	H4	D16#	AGTL+ I/O
AA1	A27#	AGTL+ I/O	R4	D17#	AGTL+ I/O
AK6	A28#	AGTL+ I/O	P4	D18#	AGTL+ I/O
Z4	A29#	AGTL+ I/O	H6	D19#	AGTL+ I/O
AA3	A30#	AGTL+ I/O	L3	D20#	AGTL+ I/O
AD4	A31#	AGTL+ I/O	G1	D21#	AGTL+ I/O
AE33	A20M#	CMOS Input	F8	D22#	AGTL+ I/O
AN31	ADS#	AGTL+ I/O	G3	D23#	AGTL+ I/O
W37	BCLK	Processor Clock Input	K6	D24#	AGTL+ I/O
AH14	BNR#	AGTL+ I/O	E3	D25#	AGTL+ I/O
G33	BP2#	AGTL+ I/O	E1	D26#	AGTL+ I/O

Table 37. PPGA Package Signal Listing in Order by Signal Name (Sheet 2 of 5)

Pin No.	Pin Name	Signal Buffer Type	Pin No.	Pin Name	Signal Buffer Type
F12	D27#	AGTL+ I/O	AN19	DEFER#	AGTL+ Input
A5	D28#	AGTL+ I/O	AN27	DRDY#	AGTL+ I/O
A3	D29#	AGTL+ I/O	AG1	EDGCTRL	AGTL+ Edge Control Input
J3	D30#	AGTL+ I/O	AC35	FERR#	CMOS Output
C5	D31#	AGTL+ I/O	AE37	FLUSH#	CMOS Input
F6	D32#	AGTL+ I/O	A37	GND	Vss
C1	D33#	AGTL+ I/O	AB32	GND	Vss
C7	D34#	AGTL+ I/O	AC33	GND	Vss
B2	D35#	AGTL+ I/O	AC5	GND	Vss
C9	D36#	AGTL+ I/O	AD2	GND	Vss
A9	D37#	AGTL+ I/O	AD34	GND	Vss
D8	D38#	AGTL+ I/O	AF32	GND	Vss
D10	D39#	AGTL+ I/O	AF36	GND	Vss
C15	D40#	AGTL+ I/O	AG5	GND	Vss
D14	D41#	AGTL+ I/O	AH2	GND	Vss
D12	D42#	AGTL+ I/O	AH34	GND	Vss
A7	D43#	AGTL+ I/O	AJ11	GND	Vss
A11	D44#	AGTL+ I/O	AJ15	GND	Vss
C11	D45#	AGTL+ I/O	AJ19	GND	Vss
A21	D46#	AGTL+ I/O	AJ23	GND	Vss
A15	D47#	AGTL+ I/O	AJ27	GND	Vss
A17	D48#	AGTL+ I/O	AJ3	GND	Vss
C13	D49#	AGTL+ I/O	AJ7	GND	Vss
C25	D50#	AGTL+ I/O	AK36	GND	Vss
A13	D51#	AGTL+ I/O	AK4	GND	Vss
D16	D52#	AGTL+ I/O	AL1	GND	Vss
A23	D53#	AGTL+ I/O	AL3	GND	Vss
C21	D54#	AGTL+ I/O	AM10	GND	Vss
C19	D55#	AGTL+ I/O	AM14	GND	Vss
C27	D56#	AGTL+ I/O	AM18	GND	Vss
A19	D57#	AGTL+ I/O	AM2	GND	Vss
C23	D58#	AGTL+ I/O	AM22	GND	Vss
C17	D59#	AGTL+ I/O	AM26	GND	Vss
A25	D60#	AGTL+ I/O	AM30	GND	Vss
A27	D61#	AGTL+ I/O	AM34	GND	Vss
E25	D62#	AGTL+ I/O	AM6	GND	Vss
F16	D63#	AGTL+ I/O	AN3	GND	Vss
AL27	DBSY#	AGTL+ I/O	B12	GND	Vss

Table 37. PPGA Package Signal Listing in Order by Signal Name (Sheet 3 of 5)

Pin No.	Pin Name	Signal Buffer Type	Pin No.	Pin Name	Signal Buffer Type
B16	GND	Vss	V34	GND	Vss
B20	GND	Vss	X32	GND	Vss
B24	GND	Vss	X36	GND	Vss
B28	GND	Vss	Y37	GND	Vss
B32	GND	Vss	Y5	GND	Vss
B4	GND	Vss	Z2	GND	Vss
B8	GND	Vss	Z34	GND	Vss
D18	GND	Vss	AJ31	GND	Vss
D2	GND	Vss	Y33	GND	Vss
D22	GND	Vss	AL25	HIT#	AGTL+ I/O
D26	GND	Vss	AL23	HITM#	AGTL+ I/O
D30	GND	Vss	AE35	IERR#	CMOS Output
D34	GND	Vss	AG37	IGNNE#	CMOS Input
D4	GND	Vss	AG33	INIT#	CMOS Input
E11	GND	Vss	M36	LINT0/INTR	CMOS Input
E15	GND	Vss	L37	LINT1/NMI	CMOS Input
E19	GND	Vss	AK20	LOCK#	AGTL+ I/O
E7	GND	Vss	J33	PICCLK	APIC Clock Input
F20	GND	Vss	J35	PICD0	CMOS I/O
F24	GND	Vss	L35	PICD1	CMOS I/O
F28	GND	Vss	W33	PLL1	PLL Bypass Decoupling
F32	GND	Vss	U33	PLL2	PLL Bypass Decoupling
F36	GND	Vss	A35	PRDY#	AGTL+ Output
G5	GND	Vss	J37	PREQ#	CMOS Input
H2	GND	Vss	AK26	PWRGOOD	CMOS Input
H34	GND	Vss	AK18	REQ0#	AGTL+ I/O
K36	GND	Vss	AH16	REQ1#	AGTL+ I/O
L5	GND	Vss	AH18	REQ2#	AGTL+ I/O
M2	GND	Vss	AL19	REQ3#	AGTL+ I/O
M34	GND	Vss	AL17	REQ4#	AGTL+ I/O
P32	GND	Vss	X4	RESET#	AGTL+ Input
P36	GND	Vss	AH20	Reserved	Reserved for Future Use
Q5	GND	Vss	AH4	Reserved	Reserved for Future Use
R34	GND	Vss	A29	Reserved	Reserved for Future Use
T32	GND	Vss	A31	Reserved	Reserved for Future Use
T36	GND	Vss	A33	Reserved	Reserved for Future Use
U5	GND	Vss	AA33	Reserved	Reserved for Future Use
V2	GND	Vss	AA35	Reserved	Reserved for Future Use

Table 37. PPGA Package Signal Listing in Order by Signal Name (Sheet 4 of 5)

Pin No.	Pin Name	Signal Buffer Type	Pin No.	Pin Name	Signal Buffer Type
AC1	Reserved	Reserved for Future Use	X6	Reserved	Reserved for Future Use
AC37	Reserved	Reserved for Future Use	Y1	Reserved	Reserved for Future Use
AF4	Reserved	Reserved for Future Use	E27	Reserved	Reserved for Future Use
AK16	Reserved	Reserved for Future Use	R2	Reserved	Reserved for Future Use
AK24	Reserved	Reserved for Future Use	S35	Reserved	Reserved for Future Use
AK30	Reserved	Reserved for Future Use	X2	Reserved	Reserved for Future Use
AL11	Reserved	Reserved for Future Use	AH26	RS0#	AGTL+ Input
AL13	Reserved	Reserved for Future Use	AH22	RS1#	AGTL+ Input
AL21	Reserved	Reserved for Future Use	AK28	RS2#	AGTL+ Input
AN11	Reserved	Reserved for Future Use	AH30	SLP#	CMOS Input
AN13	Reserved	Reserved for Future Use	AJ35	SMI#	CMOS Input
AN15	Reserved	Reserved for Future Use	AG35	STPCLK#	CMOS Input
AN21	Reserved	Reserved for Future Use	AL33	TCK	TAP Input
AN23	Reserved	Reserved for Future Use	AN35	TDI	TAP Input
B36	Reserved	Reserved for Future Use	AN37	TDO	TAP Output
C29	Reserved	Reserved for Future Use	AH28	THERMTRIP#	CMOS Output
C31	Reserved	Reserved for Future Use	AK32	TMS	TAP Input
C33	Reserved	Reserved for Future Use	AL31	THERMDP	Thermal Diode Anode
E23	Reserved	Reserved for Future Use	AL29	THERMDN	Thermal Diode Cathode
E29	Reserved	Reserved for Future Use	AN25	TRDY#	AGTL+ Input
E31	Reserved	Reserved for Future Use	AN33	TRST#	TAP Input
F10	Reserved	Reserved for Future Use	AD36	$Vcc_{1.5}$	1.5V CMOS Input
G35	Reserved	Reserved for Future Use	Z36	$Vcc_{2.5}$	2.5V CMOS Input
G37	Reserved	Reserved for Future Use	AB36	Vcc_{CMOS}	CMOS Voltage Output
L33	Reserved	Reserved for Future Use	AA37	Vcc_{CORE}	Processor Core Vcc
N33	Reserved	Reserved for Future Use	AA5	Vcc_{CORE}	Processor Core Vcc
N35	Reserved	Reserved for Future Use	AB2	Vcc_{CORE}	Processor Core Vcc
N37	Reserved	Reserved for Future Use	AB34	Vcc_{CORE}	Processor Core Vcc
Q33	Reserved	Reserved for Future Use	AD32	Vcc_{CORE}	Processor Core Vcc
Q35	Reserved	Reserved for Future Use	AE5	Vcc_{CORE}	Processor Core Vcc
Q37	Reserved	Reserved for Future Use	AF2	Vcc_{CORE}	Processor Core Vcc
S33	Reserved	Reserved for Future Use	AF34	Vcc_{CORE}	Processor Core Vcc
S37	Reserved	Reserved for Future Use	AH24	Vcc_{CORE}	Processor Core Vcc
U35	Reserved	Reserved for Future Use	AH32	Vcc_{CORE}	Processor Core Vcc
U37	Reserved	Reserved for Future Use	AH36	Vcc_{CORE}	Processor Core Vcc
V4	Reserved	Reserved for Future Use	AJ13	Vcc_{CORE}	Processor Core Vcc
W3	Reserved	Reserved for Future Use	AJ17	Vcc_{CORE}	Processor Core Vcc
W35	Reserved	Reserved for Future Use	AJ21	Vcc_{CORE}	Processor Core Vcc

Table 37. PPGA Package Signal Listing in Order by Signal Name (Sheet 5 of 5)

Pin No.	Pin Name	Signal Buffer Type	Pin No.	Pin Name	Signal Buffer Type
AJ25	$V_{CC_{CORE}}$	Processor Core Vcc	F30	$V_{CC_{CORE}}$	Processor Core Vcc
AJ29	$V_{CC_{CORE}}$	Processor Core Vcc	F34	$V_{CC_{CORE}}$	Processor Core Vcc
AJ5	$V_{CC_{CORE}}$	Processor Core Vcc	F4	$V_{CC_{CORE}}$	Processor Core Vcc
AJ9	$V_{CC_{CORE}}$	Processor Core Vcc	H32	$V_{CC_{CORE}}$	Processor Core Vcc
AK2	$V_{CC_{CORE}}$	Processor Core Vcc	H36	$V_{CC_{CORE}}$	Processor Core Vcc
AK34	$V_{CC_{CORE}}$	Processor Core Vcc	J5	$V_{CC_{CORE}}$	Processor Core Vcc
AM12	$V_{CC_{CORE}}$	Processor Core Vcc	K2	$V_{CC_{CORE}}$	Processor Core Vcc
AM16	$V_{CC_{CORE}}$	Processor Core Vcc	K32	$V_{CC_{CORE}}$	Processor Core Vcc
AM20	$V_{CC_{CORE}}$	Processor Core Vcc	K34	$V_{CC_{CORE}}$	Processor Core Vcc
AM24	$V_{CC_{CORE}}$	Processor Core Vcc	M32	$V_{CC_{CORE}}$	Processor Core Vcc
AM28	$V_{CC_{CORE}}$	Processor Core Vcc	N5	$V_{CC_{CORE}}$	Processor Core Vcc
AM32	$V_{CC_{CORE}}$	Processor Core Vcc	P2	$V_{CC_{CORE}}$	Processor Core Vcc
AM4	$V_{CC_{CORE}}$	Processor Core Vcc	P34	$V_{CC_{CORE}}$	Processor Core Vcc
AM8	$V_{CC_{CORE}}$	Processor Core Vcc	R32	$V_{CC_{CORE}}$	Processor Core Vcc
B10	$V_{CC_{CORE}}$	Processor Core Vcc	R36	$V_{CC_{CORE}}$	Processor Core Vcc
B14	$V_{CC_{CORE}}$	Processor Core Vcc	S5	$V_{CC_{CORE}}$	Processor Core Vcc
B18	$V_{CC_{CORE}}$	Processor Core Vcc	T2	$V_{CC_{CORE}}$	Processor Core Vcc
B22	$V_{CC_{CORE}}$	Processor Core Vcc	T34	$V_{CC_{CORE}}$	Processor Core Vcc
B26	$V_{CC_{CORE}}$	Processor Core Vcc	V32	$V_{CC_{CORE}}$	Processor Core Vcc
B30	$V_{CC_{CORE}}$	Processor Core Vcc	V36	$V_{CC_{CORE}}$	Processor Core Vcc
B34	$V_{CC_{CORE}}$	Processor Core Vcc	W5	$V_{CC_{CORE}}$	Processor Core Vcc
B6	$V_{CC_{CORE}}$	Processor Core Vcc	X34	$V_{CC_{CORE}}$	Processor Core Vcc
C3	$V_{CC_{CORE}}$	Processor Core Vcc	Y35	$V_{CC_{CORE}}$	Processor Core Vcc
D20	$V_{CC_{CORE}}$	Processor Core Vcc	Z32	$V_{CC_{CORE}}$	Processor Core Vcc
D24	$V_{CC_{CORE}}$	Processor Core Vcc	E21	$V_{CORE_{DET}}$	Future Processor Detection
D28	$V_{CC_{CORE}}$	Processor Core Vcc	E33	V_{REF_0}	AGTL+ Reference Voltage
D32	$V_{CC_{CORE}}$	Processor Core Vcc	F18	V_{REF_1}	AGTL+ Reference Voltage
D36	$V_{CC_{CORE}}$	Processor Core Vcc	K4	V_{REF_2}	AGTL+ Reference Voltage
D6	$V_{CC_{CORE}}$	Processor Core Vcc	R6	V_{REF_3}	AGTL+ Reference Voltage
E13	$V_{CC_{CORE}}$	Processor Core Vcc	V6	V_{REF_4}	AGTL+ Reference Voltage
E17	$V_{CC_{CORE}}$	Processor Core Vcc	AD6	V_{REF_5}	AGTL+ Reference Voltage
E5	$V_{CC_{CORE}}$	Processor Core Vcc	AK12	V_{REF_6}	AGTL+ Reference Voltage
E9	$V_{CC_{CORE}}$	Processor Core Vcc	AK22	V_{REF_7}	AGTL+ Reference Voltage
F14	$V_{CC_{CORE}}$	Processor Core Vcc	AL35	VID0	Voltage Identification
F2	$V_{CC_{CORE}}$	Processor Core Vcc	AM36	VID1	Voltage Identification
F22	$V_{CC_{CORE}}$	Processor Core Vcc	AL37	VID2	Voltage Identification
F26	$V_{CC_{CORE}}$	Processor Core Vcc	AJ37	VID3	Voltage Identification

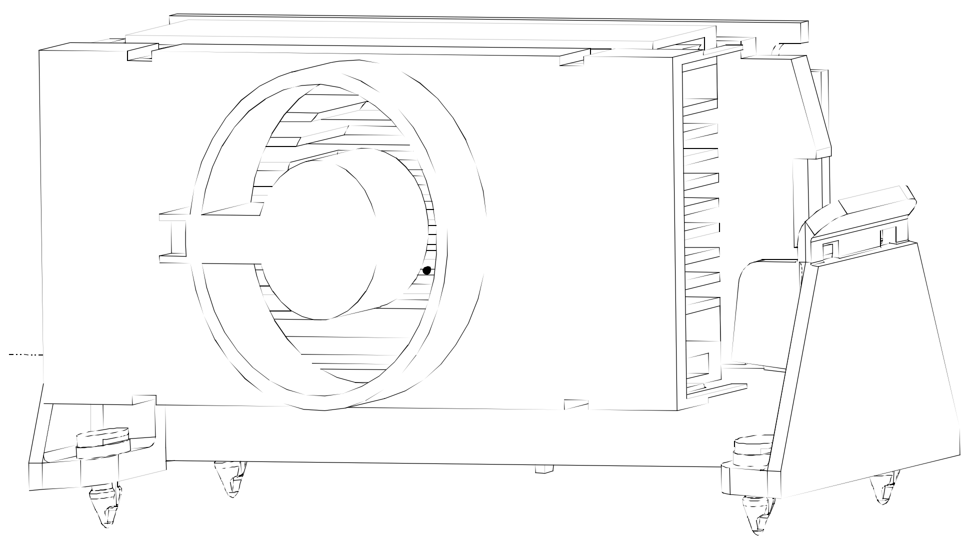
6.0 Boxed Processor Specifications

6.1 S.E.P. Package

6.1.1 Introduction

The Intel® Celeron™ processor is also offered as an Intel boxed processor in the S.E.P. Package at the following processor speeds: 400 MHz, 366 MHz, 333 MHz, 300A MHz, 300 MHz, and 266 MHz. Intel boxed processors are intended for system integrators who build systems from motherboards and standard components. The boxed Intel Celeron processor in the S.E.P. Package will be supplied with an attached fan heatsink. This section documents motherboard and system requirements for the fan heatsink that will be supplied with the boxed Intel Celeron processor. This section is particularly important for OEMs that manufacture motherboards for system integrators. Unless otherwise noted, all figures in this section are dimensioned in inches. Figure 18 shows a mechanical representation of the boxed Intel Celeron processor in a S.E.P. Package in the retention mechanism, which is not shipped with the boxed Intel Celeron processor. Note that the airflow of the fan heatsink is into the center and out of the sides of the fan heatsink.

Figure 18. Boxed Intel® Celeron™ Processor in S.E.P. Package in the Retention Mechanism



6.1.2 Mechanical Specifications

This section documents the mechanical specifications of the boxed Intel® Celeron™ processor fan heatsink.

The boxed processor ships with an attached fan heatsink. Clearance is required around the fan heatsink to ensure unimpeded airflow for proper cooling. The space requirements and dimensions for the boxed Processor with integrated fan heatsink are shown in Figure 19, Figure 20, and Figure 21. All dimensions are in inches. Note that these drawings show a conceptual attachment interface to a S.E.P. Package low profile retention mechanism.

Figure 19. Side View Space Requirements for the Boxed Processor

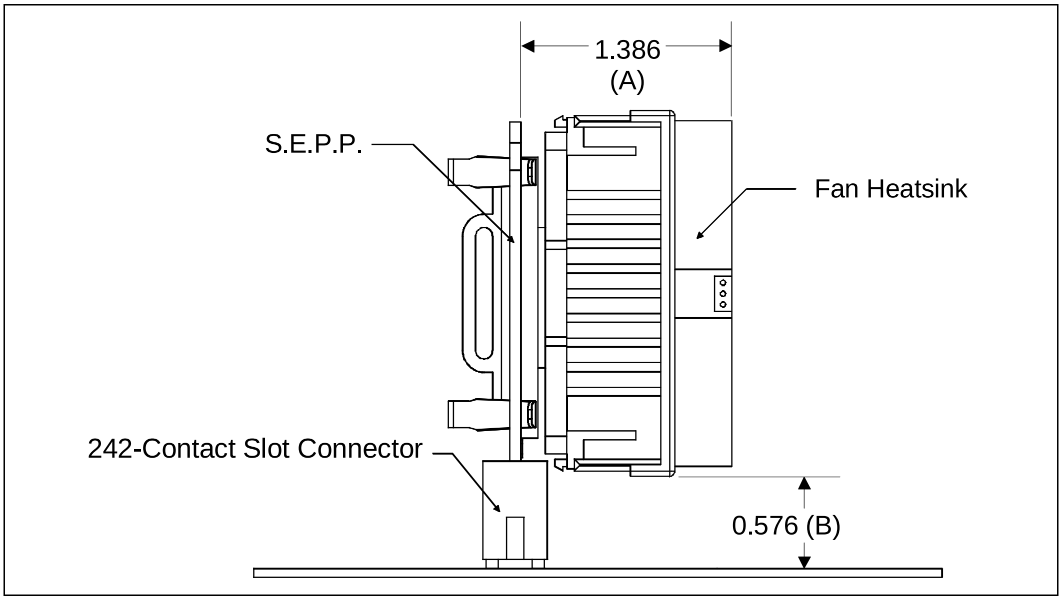


Figure 20. Front View Space Requirements for the Boxed Processor

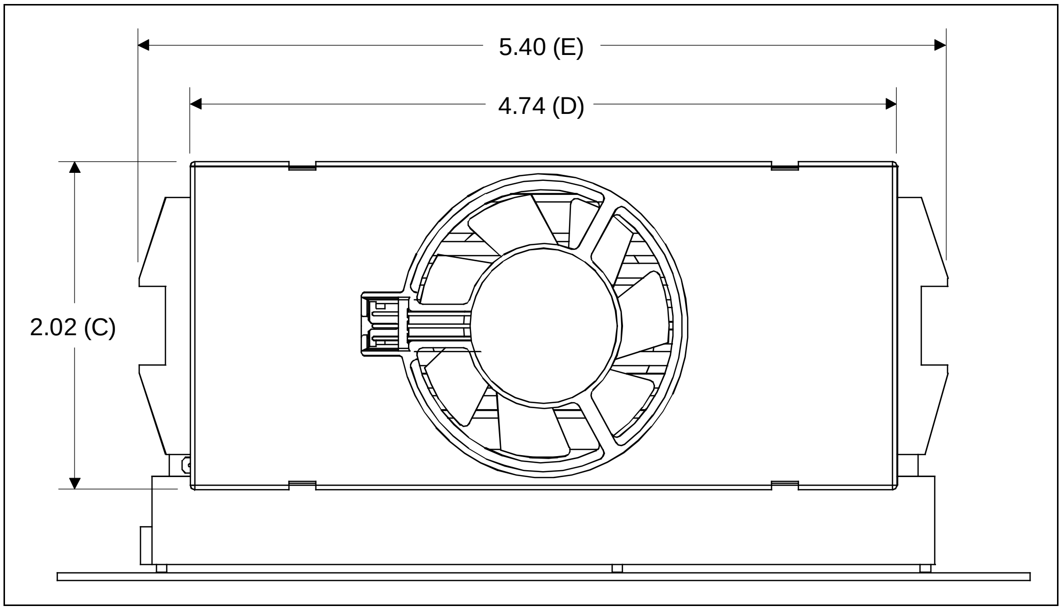
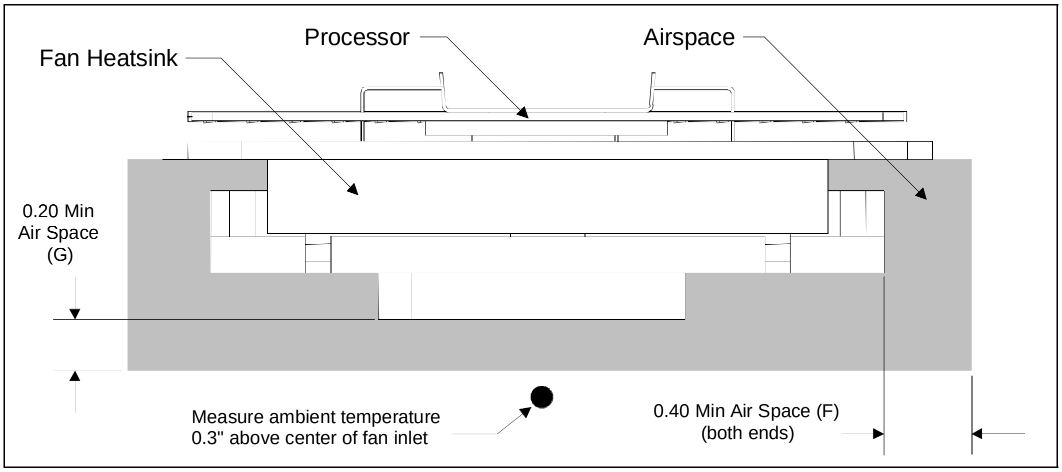


Figure 21. Top View Airspace Requirements for the Boxed Processor



6.1.2.1 Boxed Processor Heatsink Dimensions

Table 38. Boxed Processor Fan Heatsink Spatial Dimensions

Fig. Ref. Label	Dimensions (Inches)	Min	Typ	Max
A	Fan Heatsink Depth (see Figure 19)			1.386
B	Fan Heatsink Height from Motherboard (see Figure 19)		0.576	
C	Fan Heatsink Height (see Figure 20)			2.02
D	Fan Heatsink Width (see Figure 20)			4.74
E	Fan Heatsink Base Width (see Figure 20)		5.40	
F	Airflow keepout zones from end of fan heatsink	0.40		
G	Airflow keepout zones from face of fan heatsink	0.20		

6.1.2.2 Boxed Processor Heatsink Weight

The boxed processor heatsink will not weigh more than 225 grams.

6.1.2.3 Boxed Processor Retention Mechanism

The boxed Intel® Celeron™ processor requires a S.E.P. Package retention mechanism to secure the processor in the SC242 connector. A S.E.P. Package retention mechanism will not be provided with the boxed processor. Motherboards designed for use by system integrators should include a retention mechanism and appropriate installation instructions.

The boxed Intel Celeron processor does not require additional fan heatsink supports. Fan heatsink supports will not be shipped with the boxed Intel Celeron processor.

Motherboards designed for flexible use by system integrators must still recognize the boxed Pentium II processor's fan heatsink clearance requirements, which are described in *Pentium® II Processor at 233, 266, 300, and 333 MHz Datasheet* (Order Number 243335).

6.1.3 Boxed Processor Requirements

The boxed processor's fan heatsink requires a +12 V power supply. A fan power cable is shipped with the boxed processor to draw power from a power header on the motherboard. The power cable connector and pinout are shown in Figure 22. Motherboards must provide a matched power header to support the boxed processor. Table 39 contains specifications for the input and output signals at the fan heatsink connector. The cable length is 7.0 inches (±0.25"). The fan heatsink outputs a SENSE signal, which is an open-collector output, that pulses at a rate of two pulses per fan revolution. A motherboard pull-up resistor provides VOH to match the motherboard-mounted fan speed monitor requirements, if applicable. Use of the SENSE signal is optional. If the SENSE signal is not used, pin 3 of the connector should be tied to GND.

The power header on the baseboard must be positioned to allow the fan heatsink power cable to reach it. The power header identification and location should be documented in the motherboard documentation or on the motherboard. Figure 23 shows the recommended location of the fan power connector relative to the SC242 connector. The motherboard power header should be positioned within 4.75 inches (lateral) of the fan power connector.

Figure 22. Boxed Processor Fan Heatsink Power Cable Connector Description

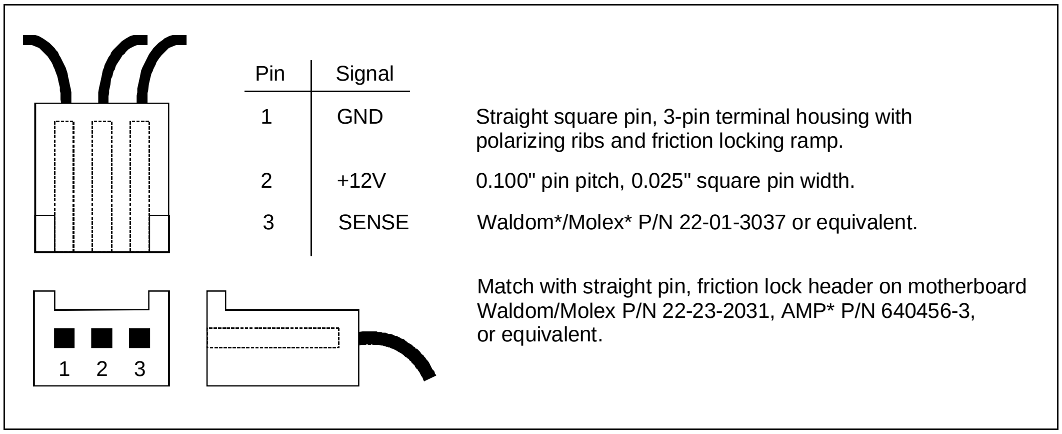
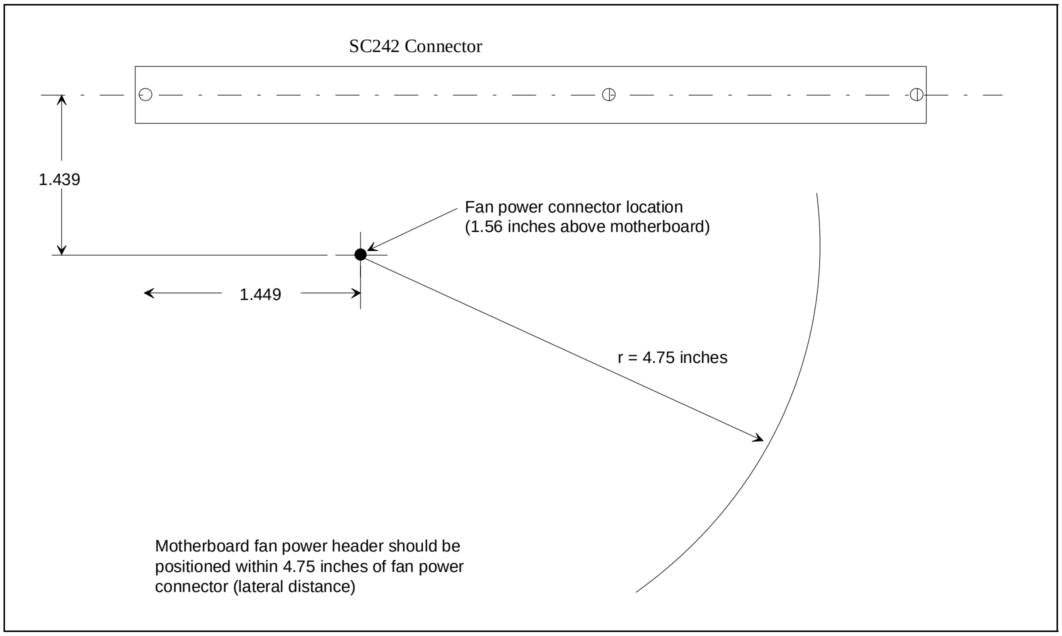


Table 39. Fan Heatsink Power and Signal Specifications

Description	Min	Typ	Max
+12 V: 12 volt fan power supply	7 V	12 V	13.8 V
IC: Fan current draw			100 mA
SENSE: SENSE frequency (motherboard should pull this pin up to appropriate V_{CC} with resistor)		2 pulses per fan revolution	

Figure 23. Motherboard Power Header Placement Relative to Fan Power Connector and SC242



6.1.4 Thermal Specifications

This section describes the cooling requirements of the fan heatsink solution utilized by the boxed processor.

6.1.4.1 Boxed Processor Cooling Requirements

The boxed processor is cooled with a fan heatsink. The boxed processor fan heatsink will keep the processor core case temperature, T_{CASE}, within the specifications (see Table 27), provided airflow through the fan heatsink is unimpeded and the air temperature entering the fan is below 45 °C (see Figure 21 for measurement location).

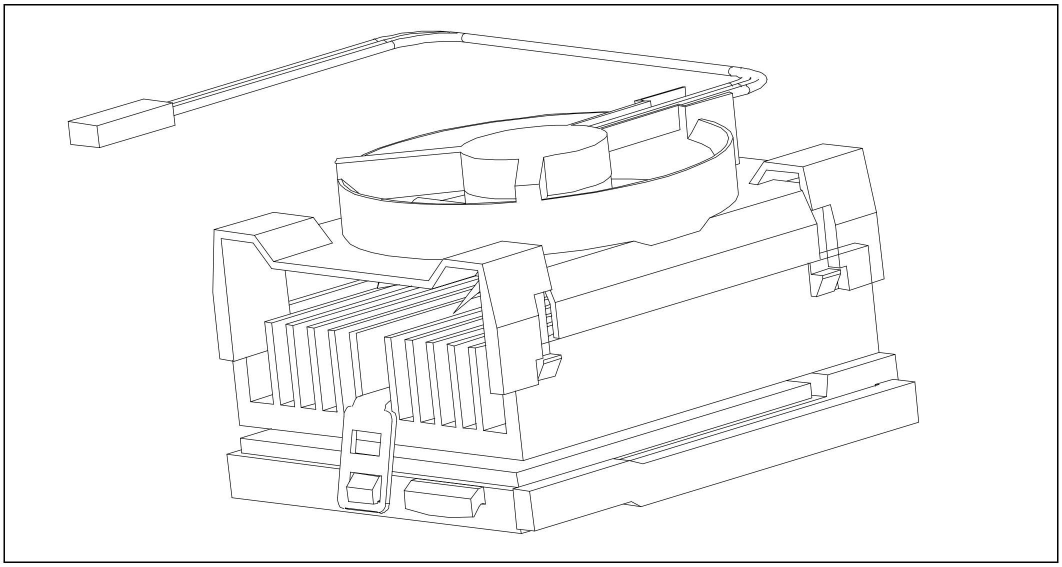
Airspace is required around the fan to ensure that the airflow through the fan heatsink is not blocked. Blocking the airflow to the fan heatsink reduces the cooling efficiency and decreases fan life. Figure 21 illustrates an acceptable airspace clearance for the fan heatsink.

6.2 PPGA Package

6.2.1 Introduction

The Intel® Celeron™ processor is also offered as an Intel boxed processor in the PPGA package at the following processor speeds: 433 MHz, 400 MHz, 366 MHz, 333 MHz, and 300A MHz. Intel boxed processors are intended for system integrators who build systems from motherboards and standard components. The boxed Intel Celeron processor in the PPGA package will be supplied with an unattached fan heatsink. This section documents motherboard and system requirements for the fan heatsink that will be supplied with the boxed Intel Celeron processor. This section is particularly important for OEMs that manufacture motherboards for system integrators. Unless otherwise noted, all figures in this section are dimensioned in inches. Figure 24 shows a mechanical representation of the boxed Intel Celeron processor in the PPGA package. Note that the airflow of the fan heatsink is into the center and out of the sides of the fan heatsink.

Figure 24. Boxed Intel® Celeron™ Processor in PPGA Package



6.2.2 Mechanical Specifications

This section documents the mechanical specifications of the boxed Intel® Celeron™ processor fan heatsink.

The boxed processor in the PPGA package ships with an unattached fan heatsink which has an attached integrated clip. Clearance is required around the fan heatsink to ensure unimpeded airflow for proper cooling. The space requirements and dimensions for the boxed Processor with integrated fan heatsink are shown in Figure 25 and Figure 26. All dimensions are in inches.

Figure 25. Side View Space Requirements for the Boxed Processor

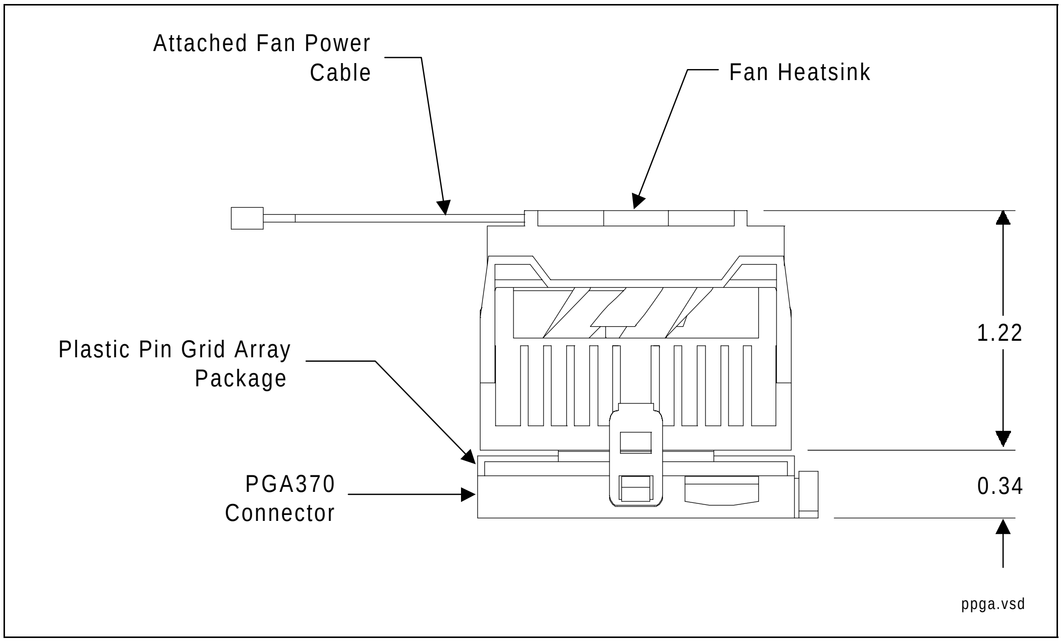


Figure 26. Top View Space Requirements for the Boxed Processor

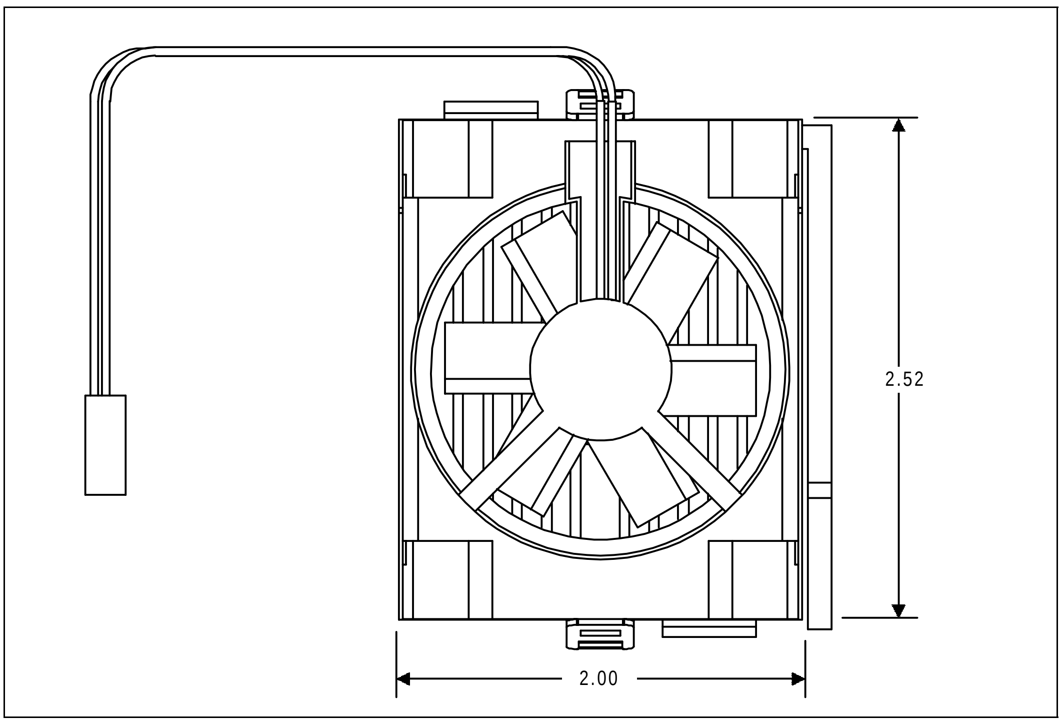
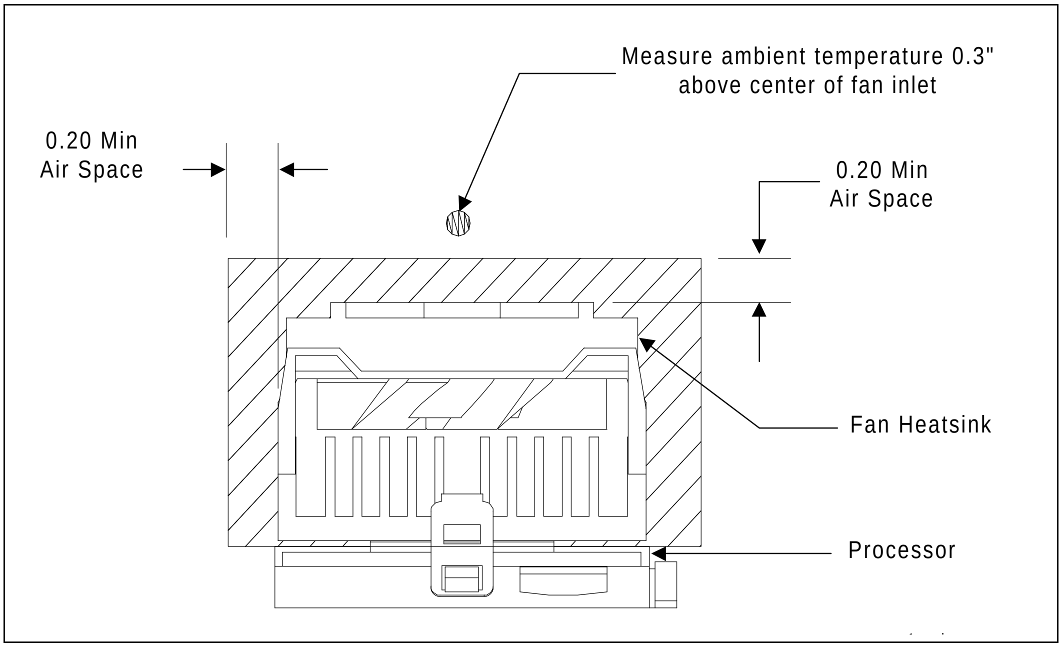


Figure 27. Side View Airspace Requirements for the Boxed Processor



6.2.2.1 Boxed Processor Heatsink Dimensions

Table 40. Boxed Processor Fan Heatsink Spatial Dimensions

Dimensions (Inches)	Min	Typ	Max
Fan Heatsink Length (see Figure 26)			2.52
Fan Heatsink Height from Motherboard (see Figure 25)		0.34	
Fan Heatsink Height (see Figure 25)			1.22
Fan Heatsink Width (see Figure 26)			2.00
Airflow keepout zones from end of fan heatsink	0.20		
Airflow keepout zones from face of fan heatsink	0.20		

6.2.2.2 Boxed Processor Heatsink Weight

The boxed processor heatsink will not weigh more than 180 grams.

6.2.2.3 Boxed Processor Thermal Cooling Solution Clip

The boxed processor thermal solution requires installation by a system integrator to secure the thermal cooling solution to the processor after it is installed in the 370-pin socket ZIF socket. Motherboards designed for use by system integrators should take care to consider the implications of clip installation and potential scraping of the motherboard PCB underneath the 370-pin socket attach tabs. Motherboard components should not be placed too close to the 370-pin socket attach tabs in a way that interferes with the installation of the boxed processor thermal cooling solution (see Figure 30 for specification).

6.2.3 Boxed Processor Requirements

The boxed processor's fan heatsink requires a +12 V power supply. A fan power cable is attached to the fan and will draw power from a power header on the motherboard. The power cable connector and pinout are shown in Figure 28. Motherboards must provide a matched power header to support the boxed processor. Table 41 contains specifications for the input and output signals at the fan heatsink connector. The cable length is 7.0 inches (±0.25").

The power header on the baseboard must be positioned to allow the fan heatsink power cable to reach it. The power header identification and location should be documented in the motherboard documentation or on the motherboard. Figure 29 shows the recommended location of the fan power connector relative to the 370-pin socket. The motherboard power header should be positioned within 4.00 inches from the center of the 370-pin socket.

Figure 28. Boxed Processor Fan Heatsink Power Cable Connector Description

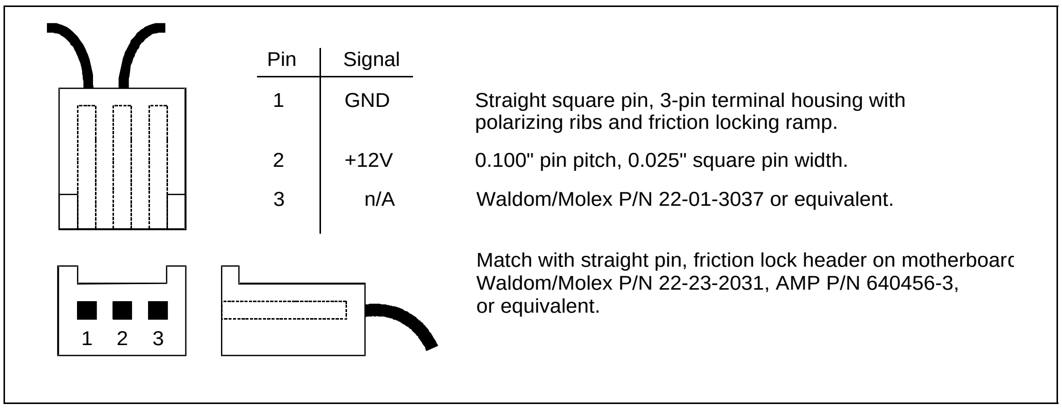


Table 41. Fan Heatsink Power and Signal Specifications

Description	Min	Typ	Max
+12 V: 12 volt fan power supply	7 V	12 V	13.8 V
IC: Fan current draw			100 mA

Figure 29. Motherboard Power Header Placement Relative to the Intel® Celeron™ Processor in the PPGA Package

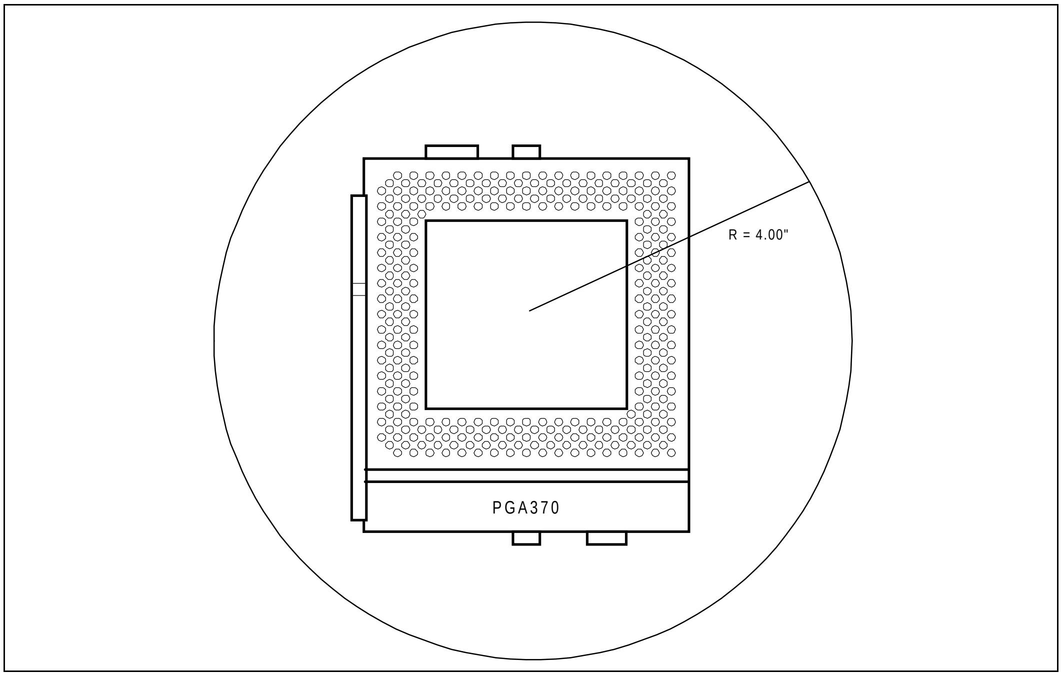


Figure 30. Top View of Motherboard Keepout Requirements

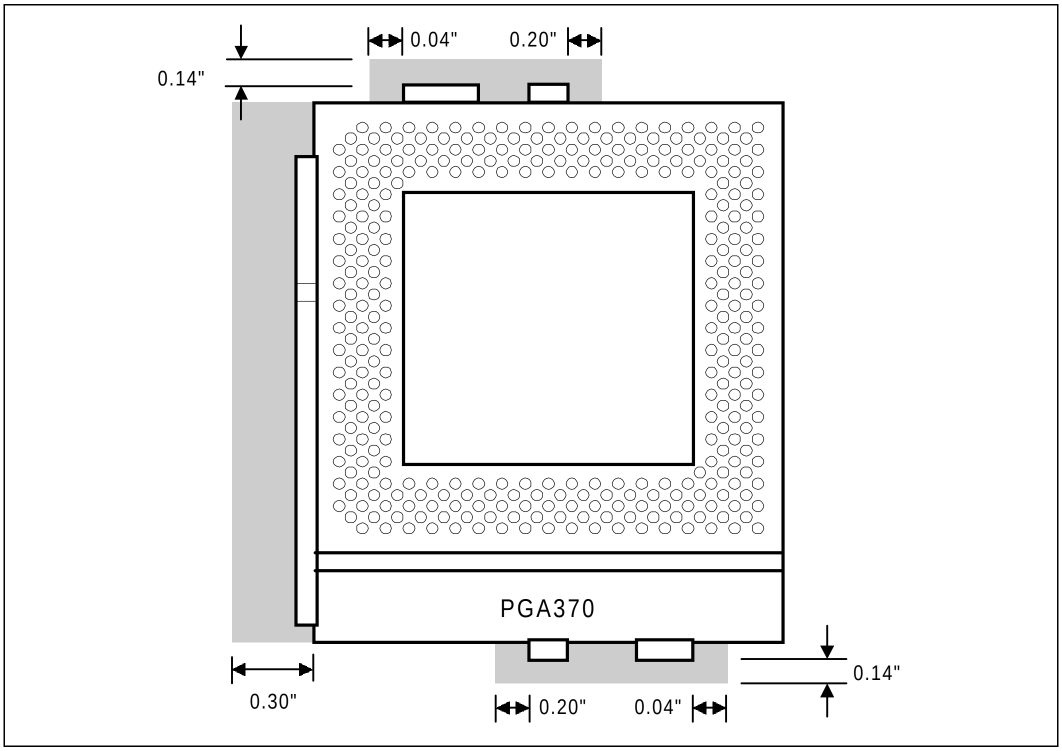
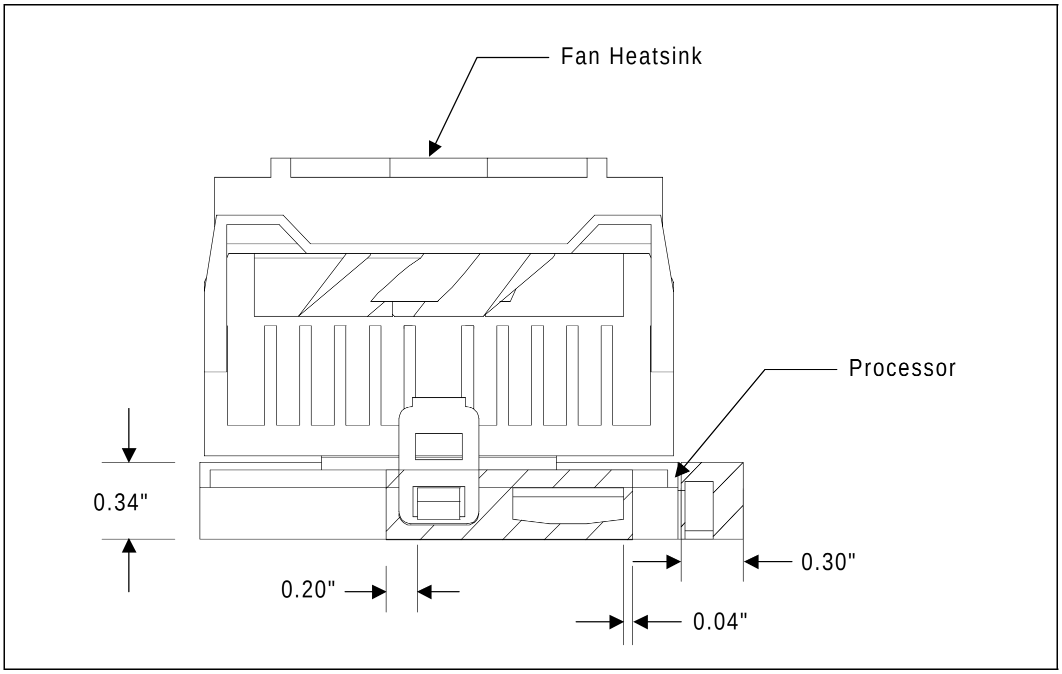


Figure 31. Side View of Motherboard Keepout Requirements



6.2.4 Thermal Specifications

This section describes the cooling requirements of the fan heatsink solution utilized by the boxed processor.

6.2.4.1 Boxed Processor Cooling Requirements

The boxed processor is cooled with a fan heatsink. The boxed processor fan heatsink will keep the processor core case temperature, T_{CASE}, within the specifications (see Table 27), provided airflow through the fan heatsink is unimpeded and the air temperature entering the fan is below 45 °C (see Figure 27 for measurement location).

Airspace is required around the fan to ensure that the airflow through the fan heatsink is not blocked. Blocking the airflow to the fan heatsink reduces the cooling efficiency and decreases fan life. Figure 27 illustrates an acceptable airspace clearance for the fan heatsink.

7.0 Intel® Celeron™ Processor Signal Description

Table 42 provides an alphabetical listing of all Intel® Celeron™ processor signals. The tables at the end of this section summarize the signals by direction: output, input, and I/O.

Note: Unless otherwise noted, the signals apply to both S.E.P. and PPGA Packages

Table 42. Alphabetical Signal Reference (Sheet 1 of 6)

Signal	Type	Description
A[31:3]#	I/O	The A[31:3]# (Address) signals define a 2^{32}-byte physical memory address space. When ADS# is active, these pins transmit the address of a transaction; when ADS# is inactive, these pins transmit transaction type information. These signals must connect the appropriate pins of all agents on the Intel® Celeron™ processor system bus. The A[31:24]# signals are parity-protected by the AP1# parity signal, and the A[23:3]# signals are parity-protected by the AP0# parity signal. On the active-to-inactive transition of RESET#, the processors sample the A[31:3]# pins to determine their power-on configuration. See the *Pentium® II Processor Developer's Manual* (Order Number 243502) for details.
A20M#	I	If the A20M# (Address-20 Mask) input signal is asserted, the Intel Celeron processor masks physical address bit 20 (A20#) before looking up a line in any internal cache and before driving a read/write transaction on the bus. Asserting A20M# emulates the 8086 processor's address wrap-around at the 1 MB boundary. Assertion of A20M# is only supported in real mode. A20M# is an asynchronous signal. However, to ensure recognition of this signal following an I/O write instruction, it must be valid along with the TRDY# assertion of the corresponding I/O Write bus transaction.
ADS#	I/O	The ADS# (Address Strobe) signal is asserted to indicate the validity of the transaction address on the A[31:3]# pins. All bus agents observe the ADS# activation to begin parity checking, protocol checking, address decode, internal snoop, or deferred reply ID match operations associated with the new transaction. This signal must connect the appropriate pins on all Intel Celeron processor system bus agents.
BCLK	I	The BCLK (Bus Clock) signal determines the bus frequency. All Intel Celeron processor system bus agents must receive this signal to drive their outputs and latch their inputs on the BCLK rising edge. All external timing parameters are specified with respect to the BCLK signal.
BNR#	I/O	The BNR# (Block Next Request) signal is used to assert a bus stall by any bus agent who is unable to accept new bus transactions. During a bus stall, the current bus owner cannot issue any new transactions. Since multiple agents might need to request a bus stall at the same time, BNR# is a wire-OR signal which must connect the appropriate pins of all Intel Celeron processor system bus agents. In order to avoid wire-OR glitches associated with simultaneous edge transitions driven by multiple drivers, BNR# is activated on specific clock edges and sampled on specific clock edges.
BP[3:2]#	I/O	The BP[3:2]# (Breakpoint) signals are outputs from the processor that indicate the status of breakpoints.
BPM[1:0]#	I/O	The BPM[1:0]# (Breakpoint Monitor) signals are breakpoint and performance monitor signals. They are outputs from the processor which indicate the status of breakpoints and programmable counters used for monitoring processor performance.

Table 42. Alphabetical Signal Reference (Sheet 2 of 6)

Signal	Type	Description
BPRI#	I	The BPRI# (Bus Priority Request) signal is used to arbitrate for ownership of the Intel Celeron processor system bus. It must connect the appropriate pins of all Intel Celeron processor system bus agents. Observing BPRI# active (as asserted by the priority agent) causes all other agents to stop issuing new requests, unless such requests are part of an ongoing locked operation. The priority agent keeps BPRI# asserted until all of its requests are completed, then releases the bus by deasserting BPRI#.
BSEL	I/O	This signal indicates the host bus frequency supported by the processor. A logic low indicates a host bus frequency of 66 MHz.
BR0#	I/O	The BR0# (Bus Request) pin drives the BREQ[0]# signal in the system. During power-up configuration, the central agent asserts the BREQ0# bus signal in the system to assign the symmetric agent ID to the processor. The processor samples it's BR0# pin on the active-to-inactive transition of RESET# to obtain it's symmetric agent ID. The processor asserts BR0# to request the system bus.
CPUPRES# (PPGA only)	O	The CPUPRES# signal provides the ability for a system board to detect the presence of a processor. This pin is a ground on the processor indicating to the system that a processor is installed.
D[63:0]#	I/O	The D[63:0]# (Data) signals are the data signals. These signals provide a 64-bit data path between the Intel Celeron processor system bus agents, and must connect the appropriate pins on all such agents. The data driver asserts DRDY# to indicate a valid data transfer.
DBSY#	I/O	The DBSY# (Data Bus Busy) signal is asserted by the agent responsible for driving data on the Intel Celeron processor system bus to indicate that the data bus is in use. The data bus is released after DBSY# is deasserted. This signal must connect the appropriate pins on all Intel Celeron processor system bus agents.
DEFER#	I	The DEFER# signal is asserted by an agent to indicate that a transaction cannot be guaranteed in-order completion. Assertion of DEFER# is normally the responsibility of the addressed memory or I/O agent. This signal must connect the appropriate pins of all Intel Celeron processor system bus agents.
DRDY#	I/O	The DRDY# (Data Ready) signal is asserted by the data driver on each data transfer, indicating valid data on the data bus. In a multicycle data transfer, DRDY# may be deasserted to insert idle clocks. This signal must connect the appropriate pins of all Intel Celeron processor system bus agents.
EDGCTRL	I	The EDGCTRL input provides AGTL+ edge control and should be pulled up to $V_{CC_{CORE}}$ with a 51 Ω ±5% resistor.
EMI (S.E.P.P. only)	I	EMI pins should be connected to motherboard ground and/or to chassis ground through zero ohm (0Ω) resistors. The zero ohm resistors should be placed in close proximity to the Intel Celeron processor connector. The path to chassis ground should be short in length and have a low impedance. These pins are used for EMI management purposes.
FERR#	O	The FERR# (Floating-point Error) signal is asserted when the processor detects an unmasked floating-point error. FERR# is similar to the ERROR# signal on the Intel 387 coprocessor, and is included for compatibility with systems using MS-DOS*-type floating-point error reporting.
FLUSH#	I	When the FLUSH# input signal is asserted, the processor writes back all data in the Modified state from the internal cache and invalidates all internal cache lines. At the completion of this operation, the processor issues a Flush Acknowledge transaction. The processor does not cache any new data while the FLUSH# signal remains asserted. FLUSH# is an asynchronous signal. However, to ensure recognition of this signal following an I/O write instruction, it must be valid along with the TRDY# assertion of the corresponding I/O Write bus transaction. On the active-to-inactive transition of RESET#, the processor samples FLUSH# to determine its power-on configuration. See *Pentium® Pro Family Developer's Manual, Volume 1: Specifications* (Order Number 242690) for details.

Table 42. Alphabetical Signal Reference (Sheet 3 of 6)

Signal	Type	Description
HIT#, HITM#	I/O	The HIT# (Snoop Hit) and HITM# (Hit Modified) signals convey transaction snoop operation results, and must connect the appropriate pins of all Intel Celeron processor system bus agents. Any such agent may assert both HIT# and HITM# together to indicate that it requires a snoop stall, which can be continued by reasserting HIT# and HITM# together.
IERR#	O	The IERR# (Internal Error) signal is asserted by a processor as the result of an internal error. Assertion of IERR# is usually accompanied by a SHUTDOWN transaction on the Intel Celeron processor system bus. This transaction may optionally be converted to an external error signal (e.g., NMI) by system core logic. The processor will keep IERR# asserted until the assertion of RESET#, BINIT#, or INIT#.
IGNNE#	I	The IGNNE# (Ignore Numeric Error) signal is asserted to force the processor to ignore a numeric error and continue to execute noncontrol floating-point instructions. If IGNNE# is deasserted, the processor generates an exception on a noncontrol floating-point instruction if a previous floating-point instruction caused an error. IGNNE# has no effect when the NE bit in control register 0 is set. IGNNE# is an asynchronous signal. However, to ensure recognition of this signal following an I/O write instruction, it must be valid along with the TRDY# assertion of the corresponding I/O Write bus transaction.
INIT#	I	The INIT# (Initialization) signal, when asserted, resets integer registers inside all processors without affecting their internal (L1) caches or floating-point registers. Each processor then begins execution at the power-on Reset vector configured during power-on configuration. The processor continues to handle snoop requests during INIT# assertion. INIT# is an asynchronous signal and must connect the appropriate pins of all bus agents. If INIT# is sampled active on the active to inactive transition of RESET#, then the processor executes its Built-in Self-Test (BIST).
LINT[1:0]	I	The LINT[1:0] (Local APIC Interrupt) signals must connect the appropriate pins of all APIC Bus agents, including all processors and the core logic or I/O APIC component. When the APIC is disabled, the LINT0 signal becomes INTR, a maskable interrupt request signal, and LINT1 becomes NMI, a nonmaskable interrupt. INTR and NMI are backward compatible with the signals of those names on the Pentium® processor. Both signals are asynchronous. Both of these signals must be software configured via BIOS programming of the APIC register space to be used either as NMI/INTR or LINT[1:0]. Because the APIC is enabled by default after Reset, operation of these pins as LINT[1:0] is the default configuration.
LOCK#	I/O	The LOCK# signal indicates to the system that a transaction must occur atomically. This signal must connect the appropriate pins of all system bus agents. For a locked sequence of transactions, LOCK# is asserted from the beginning of the first transaction end of the last transaction. When the priority agent asserts BPRI# to arbitrate for ownership of the system bus, it will wait until it observes LOCK# deasserted. This enables symmetric agents to retain ownership of the system bus throughout the bus locked operation and ensure the atomicity of lock.
PICCLK	I	The PICCLK (APIC Clock) signal is an input clock to the processor and core logic or I/O APIC which is required for operation of all processors, core logic, and I/O APIC components on the APIC bus.
PICD[1:0]	I/O	The PICD[1:0] (APIC Data) signals are used for bidirectional serial message passing on the APIC bus, and must connect the appropriate pins of the Intel Celeron processor for proper initialization.
PLL1, PLL2 (PPGA only)	I	All Intel Celeron processors have internal analog PLL clock generators that require quiet power supplies. PLL1 and PLL2 are inputs to the internal PLL and should be connected to $V_{CC_{CORE}}$ through a low-pass filter that minimizes jitter.
PRDY#	O	The PRDY (Probe Ready) signal is a processor output used by debug tools to determine processor debug readiness.

Table 42. Alphabetical Signal Reference (Sheet 4 of 6)

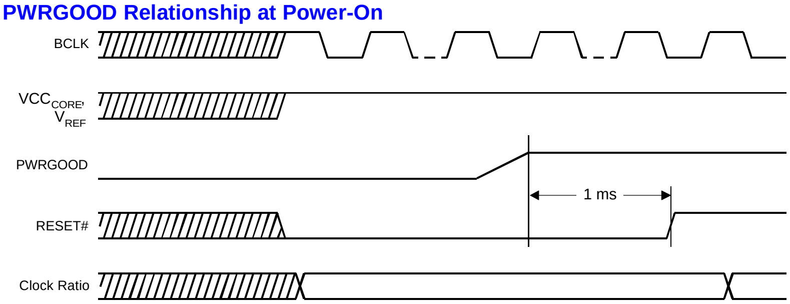
Signal	Type	Description
PREQ#	I	The PREQ# (Probe Request) signal is used by debug tools to request debug operation of the processors.
PWRGOOD	I	The PWRGOOD (Power Good) signal is a 2.5 V tolerant processor input. The processor requires this signal to be a clean indication that the clocks and power supplies ($V_{CC_{CORE}}$, etc.) are stable and within their specifications. Clean implies that the signal will remain low (capable of sinking leakage current), without glitches, from the time that the power supplies are turned on until they come within specification. The signal must then transition monotonically to a high (2.5 V) state. Figure 23 illustrates the relationship of PWRGOOD to other system signals. PWRGOOD can be driven inactive at any time, but clocks and power must again be stable before a subsequent rising edge of PWRGOOD. It must also meet the minimum pulse width specification in Table 14 and Table 15, and be followed by a 1 ms RESET# pulse. The PWRGOOD signal must be supplied to the processor; it is used to protect internal circuits against voltage sequencing issues. It should be driven high throughout boundary scan operation. **PWRGOOD Relationship at Power-On** 
REQ[4:0]#	I/O	The REQ[4:0]# (Request Command) signals must connect the appropriate pins of all processor system bus agents. They are asserted by the current bus owner over two clock cycles to define the currently active transaction type.
RESET#	I	Asserting the RESET# signal resets the processor to a known state and invalidates the L1 cache without writing back any of the contents. RESET# must remain active for one microsecond for a "warm" Reset; for a power-on Reset, RESET# must stay active for at least one millisecond after $V_{CC_{CORE}}$ and CLK have reached their proper specifications. On observing active RESET#, all system bus agents will deassert their outputs within two clocks. A number of bus signals are sampled at the active-to-inactive transition of RESET# for power-on configuration. These configuration options are described in the *Pentium® Pro Family Developer's Manual, Volume 1: Specifications* (Order Number 242690). The processor may have its outputs tristated via power-on configuration. Otherwise, if INIT# is sampled active during the active-to-inactive transition of RESET#, the processor will execute its Built-in Self-Test (BIST). Whether or not BIST is executed, the processor will begin program execution at the power on Reset vector (default 0_FFFF_FFF0h). RESET# must connect the appropriate pins of all processor system bus agents.
RS[2:0]#	I	The RS[2:0]# (Response Status) signals are driven by the response agent (the agent responsible for completion of the current transaction), and must connect the appropriate pins of all processor system bus agents.

Table 42. Alphabetical Signal Reference (Sheet 5 of 6)

<table>
<tr><th>Signal</th><th>Type</th><th>Description</th></tr>
<tr><td>SLOTOCC#
(S.E.P.P. only)</td><td>O</td><td>SLOTOCC# is defined to allow a system design to detect the presence of a terminator card or processor in a SC242 connector. This pin is not a signal; rather, it is a short to VSS. Combined with the VID combination of VID[4:0]= 11111 (see Section 2.5), a system can determine if a SC242 connector is occupied, and whether a processor core is present. The states and values for determining the type of cartridge in the SC242 connector is shown below.

SC242 Occupation Truth Table
<table>
<tr><th>Signal</th><th>Value</th><th>Status</th></tr>
<tr><td>SLOTOCC#
VID[4:0]</td><td>0
Anything other than ‘11111’</td><td>Processor with core in SC242 connector.</td></tr>
<tr><td>SLOTOCC#
VID[4:0]</td><td>0
11111</td><td>Terminator cartridge in SC242 connector (i.e., no core present).</td></tr>
<tr><td>SLOTOCC#
VID[4:0]</td><td>1
Any value</td><td>SC242 connector not occupied.</td></tr>
</table></td></tr>
<tr><td>SLP#</td><td>I</td><td>The SLP# (Sleep) signal, when asserted in Stop-Grant state, causes processors to enter the Sleep state. During Sleep state, the processor stops providing internal clock signals to all units, leaving only the Phase-Locked Loop (PLL) still operating. Processors in this state will not recognize snoops or interrupts. The processor will recognize only assertions of the SLP#, STPCLK#, and RESET# signals while in Sleep state. If SLP# is deasserted, the processor exits Sleep state and returns to Stop-Grant state, restarting its internal clock signals to the bus and APIC processor core units.</td></tr>
<tr><td>SMI#</td><td>I</td><td>The SMI# (System Management Interrupt) signal is asserted asynchronously by system logic. On accepting a System Management Interrupt, processors save the current state and enter System Management Mode (SMM). An SMI Acknowledge transaction is issued, and the processor begins program execution from the SMM handler.</td></tr>
<tr><td>STPCLK#</td><td>I</td><td>The STPCLK# (Stop Clock) signal, when asserted, causes processors to enter a low power Stop-Grant state. The processor issues a Stop-Grant Acknowledge transaction, and stops providing internal clock signals to all processor core units except the bus and APIC units. The processor continues to snoop bus transactions and service interrupts while in Stop-Grant state. When STPCLK# is deasserted, the processor restarts its internal clock to all units and resumes execution. The assertion of STPCLK# has no effect on the bus clock; STPCLK# is an asynchronous input.</td></tr>
<tr><td>TCK</td><td>I</td><td>The TCK (Test Clock) signal provides the clock input for the Intel Celeron processor Test Access Port.</td></tr>
<tr><td>TDI</td><td>I</td><td>The TDI (Test Data In) signal transfers serial test data into the processor. TDI provides the serial input needed for JTAG specification support.</td></tr>
<tr><td>TDO</td><td>O</td><td>The TDO (Test Data Out) signal transfers serial test data out of the processor. TDO provides the serial output needed for JTAG specification support.</td></tr>
<tr><td>TESTHI
(S.E.P.P. only)</td><td>I</td><td>Refer to Section 2.6 for implementation details.</td></tr>
<tr><td>THERMDN</td><td>O</td><td>Thermal Diode p-n junction. Used to calculate core temperature. See Section 4.1.</td></tr>
<tr><td>THERMDP</td><td>I</td><td>Thermal Diode p-n junction. Used to calculate core temperature. See Section 4.1.</td></tr>
</table>

Table 42. Alphabetical Signal Reference (Sheet 6 of 6)

Signal	Type	Description
THERMTRIP#	O	The processor protects itself from catastrophic overheating by use of an internal thermal sensor. This sensor is set well above the normal operating temperature to ensure that there are no false trips. The processor will stop all execution when the junction temperature exceeds approximately 135 °C. This is signaled to the system by the THERMTRIP# (Thermal Trip) pin. Once activated, the signal remains latched, and the processor stopped, until RESET# goes active. There is no hysteresis built into the thermal sensor itself; as long as the die temperature drops below the trip level, a RESET# pulse will reset the processor and execution will continue. If the temperature has not dropped below the trip level, the processor will reassert THERMTRIP# and remain stopped.
TMS	I	The TMS (Test Mode Select) signal is a JTAG specification support signal used by debug tools.
TRDY#	I	The TRDY# (Target Ready) signal is asserted by the target to indicate that it is ready to receive a write or implicit writeback data transfer. TRDY# must connect the appropriate pins of all system bus agents.
TRST#	I	The TRST# (Test Reset) signal resets the Test Access Port (TAP) logic. Intel Celeron processors require this signal to be driven low during power on Reset. A 680 ohm resistor is the suggested value for a pull down resistor on TRST#.
$V_{CC1.5}$ (PPGA only)	I	The V_{CCCMOS} pin provides the CMOS voltage for use by the platform. The 2.5 V must be provided to the $V_{CC2.5}$ input and 1.5 V must be provided to the $V_{CC1.5}$ input. The processor re-routes the 2.5 V input to the V_{CCCMOS} output via the package. Future processors requiring 1.5 V CMOS voltage levels will route the 1.5 V at the $V_{CC1.5}$ input to the V_{CCCMOS} output.
$V_{CC2.5}$ (PPGA only)	I	The V_{CCCMOS} pin provides the CMOS voltage for use by the platform. The 2.5 V must be provided to the $V_{CC2.5}$ input and 1.5 V must be provided to the $V_{CC1.5}$ input. The processor re-routes the 2.5 V input to the V_{CCCMOS} output via the package. Future processors requiring 1.5 V CMOS voltage levels will route the 1.5 V at the $V_{CC1.5}$ input to the V_{CCCMOS} output.
V_{CCCMOS} (PPGA only)	O	The V_{CCCMOS} pin provides the CMOS voltage for use by the platform. The 2.5 V must be provided to the $V_{CC2.5}$ input and 1.5 V must be provided to the $V_{CC1.5}$ input. The processor re-routes the 2.5 V input to the V_{CCCMOS} output via the package. Future processors requiring 1.5 V CMOS voltage levels will route the 1.5 V at the $V_{CC1.5}$ input to the V_{CCCMOS} output.
$V_{CORE_{DET}}$ (PPGA only)	O	The $V_{CORE_{DET}}$ signal will float for 2.0 V core processors and will be grounded for future processors with a lower core voltage.
VID[4:0] (S.E.P.P.) VID[3:0] (PPGA)	O	The VID (Voltage ID) pins can be used to support automatic selection of power supply voltages. These pins are not signals, but are either an open circuit or a short circuit to VSS on the processor. The combination of opens and shorts defines the voltage required by the processor. The VID pins are needed to cleanly support voltage specification variations on Intel Celeron processors. See Table 1 for definitions of these pins. The power supply must supply the voltage that is requested by these pins, or disable itself.
V_{REF}[7:0] (PPGA only)	I	These input signals are used by the AGTL+ inputs as a reference voltage. AGTL+ inputs are differential receivers and will use this voltage to determine whether the signal is a logic high or logic low.

7.1 Signal Summaries

Table 43 through Table 46 list attributes of the Intel® Celeron™ processor output, input, and I/O signals.

Table 43. Output Signals

Name	Active Level	Clock	Signal Group
CPUPRES# (PPGA only)	Low	Asynch	Power/Other
FERR#	Low	Asynch	CMOS Output
IERR#	Low	Asynch	CMOS Output
PRDY#	Low	BCLK	AGTL+ Output
SLOTOCC# (S.E.P.P. only)	Low	Asynch	Power/Other
TDO	High	TCK	TAP Output
THERMDN	N/A	Asynch	Power/Other
THERMTRIP#	Low	Asynch	CMOS Output
$V_{CORE_{DET}}$ (PPGA only)	High	Asynch	Power/Other
VID[4:0] (S.E.P.P.) VID[3:0] (PPGA)	High	Asynch	Power/Other

Table 44. Input Signals (Sheet 1 of 2)

Name	Active Level	Clock	Signal Group	Qualified
A20M#	Low	Asynch	CMOS Input	Always [1]
BPRI#	Low	BCLK	AGTL+ Input	Always
BCLK	High	—	System Bus Clock	Always
DEFER#	Low	BCLK	AGTL+ Input	Always
FLUSH#	Low	Asynch	CMOS Input	Always [1]
IGNNE#	Low	Asynch	CMOS Input	Always [1]
INIT#	Low	Asynch	CMOS Input	Always [1]
INTR	High	Asynch	CMOS Input	APIC disabled mode
LINT[1:0]	High	Asynch	CMOS Input	APIC enabled mode
NMI	High	Asynch	CMOS Input	APIC disabled mode
PICCLK	High	—	APIC Clock	Always
PREQ#	Low	Asynch	CMOS Input	Always
PWRGOOD	High	Asynch	CMOS Input	Always
RESET#	Low	BCLK	AGTL+ Input	Always
RS[2:0]#	Low	BCLK	AGTL+ Input	Always
SLP#	Low	Asynch	CMOS Input	During Stop-Grant state
SMI#	Low	Asynch	CMOS Input	

Table 44. Input Signals (Sheet 2 of 2)

Name	Active Level	Clock	Signal Group	Qualified
STPCLK#	Low	Asynch	CMOS Input	
TCK	High	—	TAP Input	
TDI	High	TCK	TAP Input	
TESTHI (S.E.P.P. only)	High	Asynch	Power/Other	Always
THERMDP	N/A	Asynch	Power/Other	
TMS	High	TCK	TAP Input	
TRST#	Low	Asynch	TAP Input	
TRDY#	Low	BCLK	AGTL+ Input	

NOTE:
1. Synchronous assertion with active TRDY# ensures synchronization.

Table 45. Input/Output Signals (Single Driver)

Name	Active Level	Clock	Signal Group	Qualified
BSEL	Low	Asynch	Power/Other	Always
BP[3:2]	Low	BCLK	AGTL+ I/O	Always
A[31:3]#	Low	BCLK	AGTL+ I/O	ADS#, ADS#+1
ADS#	Low	BCLK	AGTL+ I/O	Always
BPM[1:0]#	Low	BCLK	AGTL+ I/O	Always
D[63:0]#	Low	BCLK	AGTL+ I/O	DRDY#
DBSY#	Low	BCLK	AGTL+ I/O	Always
DRDY#	Low	BCLK	AGTL+ I/O	Always
LOCK#	Low	BCLK	AGTL+ I/O	Always
REQ[4:0]#	Low	BCLK	AGTL+ I/O	ADS#, ADS#+1

Table 46. Input/Output Signals (Multiple Driver)

Name	Active Level	Clock	Signal Group	Qualified
BNR#	Low	BCLK	AGTL+ I/O	Always
HIT#	Low	BCLK	AGTL+ I/O	Always
HITM#	Low	BCLK	AGTL+ I/O	Always
PICD[1:0]	High	PICCLK	APIC I/O	Always