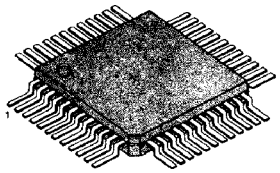
INTRODUCTION

The KA8309B is BiCMOS integrated circuit designed for the servo control of the compact disc player application.

48 - QFP - 1010D



FEATURES

- Servo control functions;
  (focus, tracking, seld servo control)
- Loop filter and VCO for EFM clock reproduction
  PLL
- Provide function
  Preventing sled runaway
  Anti-shock
  Spindle servo
  Auto-sequencer
- Provide adjustable peak of focus search,
  track jump and sled kick with external resistor
- Low power consumption
- (100mW typ; ±5V, 80mW ; 5v)
- Single power supply, 5V
- Split power supply, ±5V

ORDERING INFORMATION

Device	Package	Operating Temperature
KA8309B	48-QFP-1010D	-20℃~+75℃

BLOCK DIAGRAM

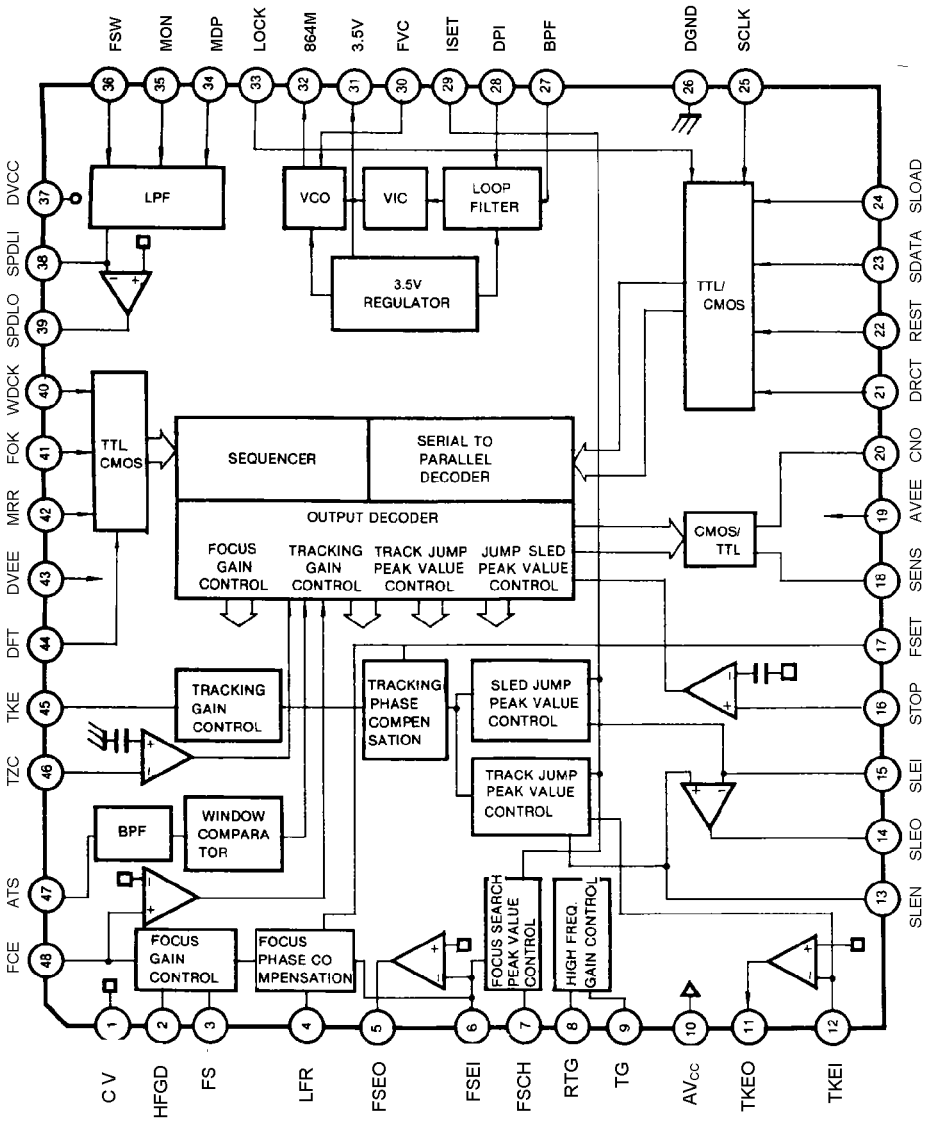


Fig. 1

PIN DESCRIPTION

Pin No	Symbol	Description
1	CV	Center voltage.
2	HFGD	Reduce high frequency gain with capacitor connected between pin 2 and pin 3.
3	FS	High frequency gain of focus servo can be changed by switching FS3 on or off.
4	LFR	Rising low frequency bandwidth of focus loop.
5	FSEO	Focus servo error output.
6	FSEI	Inverting input pin for focus amplifier.
7	FSCH	Time constant external pin to generate focus search waveform.
8	RTG	Time constant external pin to switch the tracking gain of high frequency.
9	TG	Provide time constant to change the high frequency tracking gain.
10	AV_{CC}	Analog positive power supply.
11	TKEO	Tracking error output.
12	TKEI	Inverting input pin for tracking amplifier.
13	SLEN	Non-inverting input pin for tracking amplifier.
14	SLEO	Sled output.
15	SLEI	Inventing input pin for sled amplifier.
16	STOP	Pin for detecting a signal for the on/off limit switch of the innermost part of the disc.
17	FSET	Setting the peak frequency of the focus, tracking phase compensation and of the CLV LPF.
18	SENS	Output pin for FZC, AS, TZC, STOP and BUSY by command from CPU.
19	AV_{EE}	Analog negative power supply.
20	CNO	Track number count output.
21	DRCT	Control pin for one track jump.
22	REST	Reset input pin, reset at "L".
23	SDATA	Serial data input.
24	SLOAD	Latch input.
25	SCLK	Serial data transfer clock.
26	DGND	Digital ground.
27	BPF	Provide time constant for the loop filter.

PIN DESCRIPTION (Continued)

Pin No	Symbol	Description
28	DPI	Input pin for detected phase.
29	ISET	Current is input, determining the peaks of focus search, track jump, and sled kick.
30	FVC	External resistor to adjust free running frequency of VCO.
31	3.5V	Regulated output voltage.
32	864M	Output pin of 8.64MHZ VCO.
33	LOCK	Pin for the operation of the sled runaway prevention circuit at "L".
34	MDP	Pin for connecting the DSP.
35	MON	Pin for connecting the DSP.
36	FSW	Providing an external LPF time constant of the CLV servo.
37	DV_{CC}	Digital positive power supply.
38	SPDLI	Inverting input for spindle servo amplifier.
39	SPDLO	Spindle servo error output.
40	WDCK	Clock input for auto-sequence.
41	FOK	Focus OK signal input pin.
42	MRR	Mirror signal input pin.
43	DV_{EE}	Digital negative power supply.
44	DFT	Defect signal input pin.
45	TKE	Tracking error signal input pin.
46	TZC	Input pin for the zero cross tracking comparator.
47	ATS	Input pin for detect ATSC.
48	FCE	Input pin for focus error signal.

ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC} -V_{EE}	12	V
Power Dissipation	P_D	600	mW
Operating Temperature	T_{OPR}	-20 ~ + 75	℃
Storage Temperature	T_{STG}	-55 ~ + 150	℃

ELECTRICAL CHARACTERISTICS

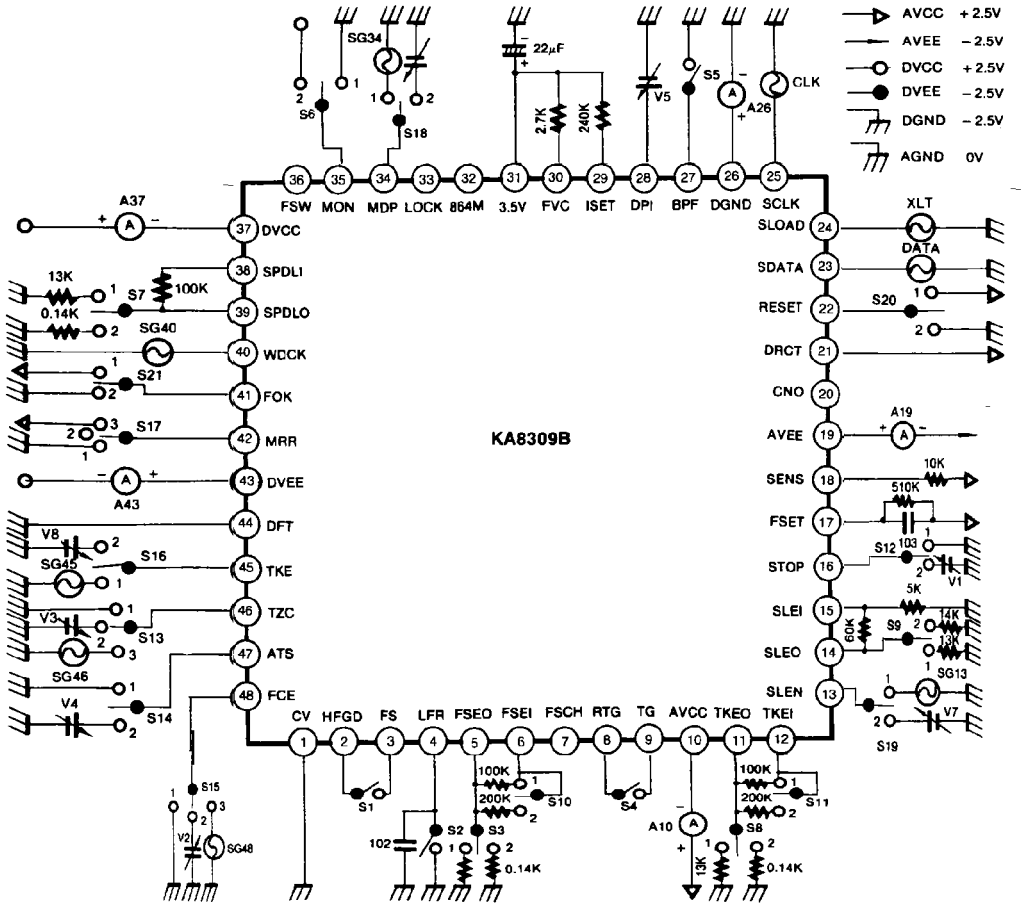
(Ta =25℃, V_{CC} =2.5V, V_{DD} =2.5V, V_{EE} = -2.5V, GND = 0V, unless otherwise specified)

Characteristic		No.	Symbol	Test Conditions	Min	Typ	Max	Unit
Circuit Current 1		1	ICC_1		2	6	10	mA
Circuit Current 2		2	ICC_2		7	10	20	mA
Circuit Current 3		3	ICC_3		-2	-7	-13	mA
Circuit Current 4		4	ICC_4		-6	-9	-19	mA
Focus Servo	DC Voltage Gain	5	$G_{V\,(DC)\,1}$	SG_{48} = 10Hz, 200mV_{P-P}	18.3	21	23.6	dB
	Feed Through	6	$G_{V\,(FF)}$	SG_{48} = 10KHz, 40mV_{P-P} Gain difference between 08 and 00 of SD			-30	dB
	Output Voltage 1	7	$V_{O\,(FCS)\,1}$	V_2 = 0.5V	1.96			V
	Output Voltage 2	8	$V_{O\,(FCS)\,2}$	V_2 = 0.5V			-1.96	V
	Output Voltage 3	9	$V_{O\,(FCS)\,3}$	V_2 = 0.5V	1.16			V
	Output Voltage 4	10	$V_{O\,(FCS)\,4}$	V_2 = 0.5V			-1.16	V
	Search Output Voltage 1	11	$V_{O(SEARCH)1}$		-0.63	-0.55	-0.37	V
	Search Output Voltage 2	12	$V_{O(SEARCH)2}$		0.39	0.55	0.65	V
Tracking Servo	DC Voltage Gain	13	$G_{V\,(DC)\,2}$	SG_{45} = 10HZ, 500mV_{P-P}	12.9	14.6	17.8	dB
	Feed Through	14	$G_{V\,(TF)}$	SG =10KHz, 500mV_{P-P} Gain difference between 25 and 20 of SD			-37	dB
	Output Voltage 1	15	$V_{O\,(TCK)\,1}$	V_8 = -1.5V	1.96			V
	Output Voltage 2	16	$V_{O\,(TCK)\,2}$	V_8 =+1.5V			-1.96	V
	Output Voltage 3	17	$V_{O\,(TCK)\,3}$	V_8 =-1.5V	1.15			V
	Output Voltage 4	18	$V_{O\,(TCK)\,4}$	V_8 =+1.5V			-1.16	V
	Jump Output Voltage 1	19	$V_{O\,(JUMP)\,1}$		-0.62	-0.55	-0.40	V
	Jump Output Voltage 2	20	$V_{O\,(JUMP)\,2}$		0.41	0.55	0.62	V
Sled Servo	DC Voltage Gain	21	$G_{V\,(DC)\,3}$	SG_3 =10Hz, 100mV_{P-P}	20.6	22.5	24.4	dB
	Output Voltage 1	22	$V_{O\,(SLD)\,1}$	V_7 = 0.4V	1.96			V
	Output Voltage 2	23	$V_{O\,(SLD)\,2}$	V_7 = -0.4V			-1.96	V
	Output Voltage 3	24	$V_{O\,(SLD)\,3}$	V_7 = 0.4V	1.16			V
	Output Voltage 4	25	$V_{O\,(SLD)\,4}$	V_7 = -0.4V			-1.16	V
	Feed Through	26	$G_{V\,(SF)}$	SG = 10KHz, 200mV Gain difference between 25 and 20 of SD			-32	dB
	Kick Output Voltage 1	27	$V_{O\,(KICK)\,1}$		0.44	0.6	0.7	V
	Kick Output Voltage 2	28	$V_{O\,(KICK)\,2}$		-0.7	-0.6	-0.43	V

ELECTRICAL CHARACTERISTICS (Continued)

Characteristic		No	Symbol	Test Conditions	Min	Typ	Max	Unit
Spindle Servo	Spindle Servo Gain	29	$G_{V\,(SPD)}$	SG =10Hz, 200mV_{P-P}	14.7	16.5	18.4	dB
	Output Voltage 1	30	$V_{O\,(SPD)\,1}$	V_6 =1 .0V	1.76			V
	Output Voltage 2	31	$V_{O\,(SPD)\,2}$	V_6 =-1 .0V			-1.76	V
	Output Voltage 3	32	$V_{O\,(SPD)\,3}$	V_6 =1 .0V	1.11			V
	Output Voltage 4	33	$V_{O\,(SPD)\,4}$	V_6 =-1 .0V			-1.11	V
PLL	PLL Regulator Output Voltage	34	V_{REG}		3.28	3.5	3.67	V
	Self-running Frequency	35	F_{VCO}	V_5 =2.5V	7.7	8.6	11.3	MHz
	Frequency Deviation 1	36	△F1	Frequency deviation from F_{VCO}, V_5 =148mV	8.0	11	14	%
	Frequency Deviation 2	37	△F2	V_5 = -148mV	-14	-11	-8.5	%
	Sens Low Level	38	V_{SENSE}				-1.96	V
Output Low Level		39	V_{OL}	SG_{46} = 10KHz, 2V_{P-P}			-1.96	V
FZC Threshold Voltage		40	$V_{TH\,(FZC)}$	V_2 = Valriable, V_{P18} = 1.1V	35	50	105	mV
ATSC Threshold Voltage		41	$V_{TH\,(ATSC)\,1}$	V_4 = Valriable, V_{P18} = 1.1V	-47	-26	-5	mV
ATSC Threshold Voltage		42	$V_{TH\,(ATSC)\,2}$	V_4 = Valriable, V_{P18} = 1.1V	5	26	47	mV
TZC Threshold Voltage		43	$V_{TH\,(TZC)}$	V_3 = Valriable, V_{P18} = 1.1V	-22	0	22	mV
SSTOP Threshold Voltage		44	$V_{TH\,(SSTOP)}$	V_1 = Valriable, V_{P18} = 1.1V	-70	-50	-30	mV

TEST CIRCUIT



TEST METHODE (SWITCH CONDITIONS)

No	Symbol	SWITCH Conditions																					I	Input	Test
		S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	S11	S12	S13	S14	S15	S16	S17	S18	S19	S20	S21	S22	S23	SD	Point	Point
1	I_{CC1}	OFF	OFF	1	OFF	OFF	1	1	1	1	1	1	1	1	1	1	1	3	1	1	2	1	OFF	1	00		10
2	I_{CC2}	OFF	OFF	1	OFF	OFF	1	1	1	1	1	1	1	1	1	1	1	1	1	1	2	1	OFF	1	00		37
3	I_{CC3}	OFF	OFF	1	OFF	OFF	1	1	1	1	1	1	1	1	1	1	1	1	1	1	2	1	OFF	1	00		19
4	I_{CC4}	OFF	OFF	1	OFF	OFF	1	1	1	1	1	1	1	1	1	1	1	1	1	1	2	1	OFF	1	00		20
5	$G_{V\,(DC)}$	OFF	OFF	1	OFF	OFF	1	1	1	1	1	1	1	1	1	3	1	1	1	1	2	1	OFF	1	08	48	5
6	$G_{V\,(FF)}$	ON	ON	1	OFF	OFF	1	1	1	1	1	1	1	1	1	3	1	1	1	1	2	1	OFF	1		48	5
7	$V_{O\,(FCS)\,1}$	OFF	OFF	1	OFF	OFF	1	1	1	1	2	1	1	1	1	2	1	1	1	1	2	1	OFF	1	08	48	5
8	$V_{O\,(FCS)\,2}$	OFF	OFF	1	OFF	OFF	1	1	1	1	2	1	1	1	1	2	1	1	1	1	2	1	OFF	1	08	48	5
9	$V_{O\,(FCS)\,3}$	OFF	OFF	2	OFF	OFF	1	1	1	1	2	1	1	1	1	2	1	1	1	1	2	1	OFF	1	08	48	5
10	$V_{O\,(FCS)\,4}$	OFF	OFF	2	OFF	OFF	1	1	1	1	2	1	1	1	1	2	1	1	1	1	2	1	OFF	1	08	48	5
11	$V_{O\,(SEARCH)\,1}$	OFF	OFF	1	OFF	OFF	1	1	1	1	1	1	1	1	1	1	1	1	1	1	2	1	OFF	1	03		5
12	$V_{O\,(SEARCH)\,2}$	OFF	OFF	1	OFF	OFF	1	1	1	1	1	1	1	1	1	1	1	1	1	1	2	1	OFF	1	03		5
13	$G_{V\,(DC)1}$	OFF	OFF	1	OFF	OFF	1	1	1	1	1	1	1	1	1	1	1	1	1	1	2	1	OFF	1	25	45	11
14	$G_{V\,(TF)}$	OFF	OFF	1	OFF	OFF	1	1	1	1	1	1	1	1	1	1	1	1	1	1	2	1	OFF	1	25	45	11
15	$V_{O\,(TCK)\,1}$	OFF	OFF	1	OFF	OFF	1	1	1	1	1	2	1	1	1	1	2	1	1	1	2	1	OFF	1	25	45	11
16	$V_{O\,(TCK)\,2}$	OFF	OFF	1	OFF	OFF	1	1	1	1	1	2	1	1	1	1	1	1	1	1	2	1	OFF	1	25	45	11
17	$V_{O\,(TCK)\,3}$	OFF	OFF	1	OFF	OFF	1	1	2	1	1	2	1	1	1	1	1	1	1	1	2	1	OFF	1	25	45	11
18	$V_{O\,(TCK)\,4}$	OFF	OFF	1	OFF	OFF	1	1	2	1	1	2	1	1	1	1	1	1	1	1	2	1	OFF	1	25	45	11
19	$V_{O\,(JUMP)1}$	OFF	OFF	1	OFF	OFF	1	1	1	1	1	1	1	1	1	1	1	1	1	1	2	1	OFF	1	20		11
20	$V_{O\,(JUMP)2}$	OFF	OFF	1	OFF	OFF	1	1	1	1	1	1	1	1	1	1	1	1	1	1	2	1	OFF	1	28		11
21	$G_{V\,(DC)\,3}$	OFF	OFF	1	OFF	OFF	1	1	1	1	1	1	1	1	1	1	1	1	1	1	2	1	OFF	1	20	13	14
22	$V_{O\,(SLD)\,1}$	OFF	OFF	1	OFF	OFF	1	1	1	1	1	1	1	1	1	1	1	1	1	2	2	1	OFF	1	25	13	14
23	$V_{O\,(SLD)\,2}$	OFF	OFF	1	OFF	OFF	1	1	1	1	1	1	1	1	1	1	1	1	1	2	2	1	OFF	1	25	13	14
24	$V_{O\,(SLD)\,3}$	OFF	OFF	1	OFF	OFF	1	1	1	2	1	1	1	1	1	1	1	1	1	2	2	1	OFF	1	25	13	14
25	$V_{O\,(SLD)\,4}$	OFF	OFF	1	OFF	OFF	1	1	1	2	1	1	1	1	1	1	1	1	1	2	2	1	OFF	1	25	13	14
26	$G_{V\,(SF)}$	OFF	OFF	1	OFF	OFF	1	1	1	1	1	1	1	1	1	3	1	1	1	1	2	1	OFF	1	20	13	14
27	$V_{O\,(KICK)\,1}$	OFF	OFF	1	OFF	OFF	1	1	1	1	1	1	1	1	1	3	1	1	1	1	2	1	OFF	1	22		14
28	$V_{O\,(KICK)\,2}$	OFF	OFF	1	OFF	OFF	1	1	1	1	1	1	1	1	1	3	1	1	1	1	2	1	OFF	1	23		14
29	$G_{V\,(SPD)}$	OFF	OFF	1	OFF	OFF	2	1	1	1	1	1	1	1	1	3	1	1	1	1	2	1	OFF	1		34	39
30	$G_{V\,(SPD)\,1}$	OFF	OFF	1	OFF	OFF	2	1	1	1	1	1	1	1	1	3	1	1	2	1	2	1	OFF	1		34	39
31	$G_{V\,(SPD)\,2}$	OFF	OFF	1	OFF	OFF	2	1	1	1	1	1	1	1	1	1	1	1	2	1	2	1	OFF	1		34	39
32	$G_{V\,(SPD)\,3}$	OFF	OFF	1	OFF	OFF	2	2	1	1	1	1	1	1	1	1	1	1	2	1	2	1	OFF	1		34	39
33	$G_{V\,(SPD)\,4}$	OFF	OFF	1	OFF	OFF	2	2	1	1	1	1	1	1	1	1	1	1	2	1	2	1	OFF	1		34	39
34	V_{RFG}	OFF	OFF	1	OFF	OFF	1	1	1	1	1	1	1	1	1	3	1	1	1	1	2	1	OFF	1			31
35	F_{VCO}	OFF	OFF	1	OFF	OFF	1	1	1	1	1	1	1	1	1	1	1	1	1	1	2	1	OFF	1			32
36	$\triangle F_1$	OFF	OFF	1	OFF	OFF	1	1	1	1	1	1	1	1	1	1	1	1	1	1	2	1	OFF	1			32
37	$\triangle F_2$	OFF	OFF	1	OFF	OFF	1	1	1	1	1	1	1	1	1	1	1	1	1	1	2	1	OFF	1			32
38	V_{SENSE}	OFF	OFF	1	OFF	OFF	1	1	1	1	1	1	1	1	1	1	1	3	1	1	2	1	OFF	1			18
39	V_{OL}	OFF	OFF	1	OFF	OFF	1	1	1	1	1	1	1	1	3	1	1	1	1	1	2	1	OFF	1			20
40	$V_{TH\,(FZC)}$	OFF	OFF	1	OFF	OFF	1	1	1	1	1	1	1	1	1	1	2	3	1	1	2	1	OFF	1	00	48	18
41	$V_{TH\,(ATSC)\,1}$	OFF	OFF	1	OFF	OFF	1	1	1	1	1	1	1	1	2	1	1	1	1	1	2	1	OFF	1	10	47	18
42	$V_{TH\,(ATSC)\,2}$	OFF	OFF	1	OFF	OFF	1	1	1	1	1	1	1	1	2	1	1	1	1	1	2	1	OFF	1	10	47	18
43	$V_{TH\,(TZC)}$	OFF	OFF	1	OFF	OFF	1	1	1	1	1	1	1	2	1	1	1	1	1	1	2	1	OFF	1	20	46	18
44	$V_{TH\,(SSTOP)}$	OFF	OFF	1	OFF	OFF	1	1	1	1	1	1	2	1	1	1	1	3	1	1	2	1	OFF	1	30	16	18

APPLICATION INFORMATION

CPU Serial Interface Timing Chart

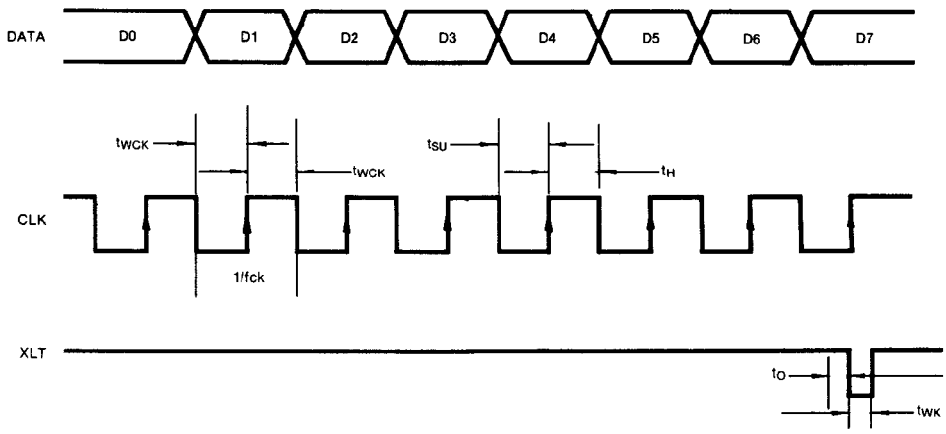


Fig. 3

DV_{CC} - D_{GND} = 4.5 to 5.5V

Item	Symbol	Min	Typ	Max	Unit
Clock Frequency	f_{CK}			1	MHz
Clock Pulse Width	f_{WCK}	500			ns
Hold Time	t_{SU}	500			ns
Setup Time	t_H	500			ns
Delay Time	t_D	500			ns
Latch Pulse Width	t_W	1000			ns

SYSTEM CONTROL

Item		Address				Data				Sens Output
		D7	D6	D5	D4	D3	D2	D1	D0	
Focus Control		0	0	0	0	FS4 Focus On	FS3 Gain Down	FS2 Search On	FS1 Search Up	FZC
Tracking Control		0	0	0	1	Anti Shock	Brake On	TG2 Gain set *1	TG1 Gain set *1	A.S
Tracking Mode		0	0	1	0	Tracking Mode *2		Sled Mode *3		TZC
Select		0	0	1	1	PS4 Focus Search + 2	PS3 Focus Search + 1	PS2 Sled Kick + 2	PS1 Sled Kick + 1	SSTOP
Auto sequence *4		0	1	0	0	AS3	AS2	AS1	AS0	Busy
	Blind(A,E)/Overflow(C)	0	1	0	1	0.18ms	0.09ms	0.045ms	0.022ms	Hi-Z
	Brake(B)					0.36ms	0.18ms	0.09ms	0.045ms	
	Kick(D)	0	1	1	0	11.6ms	5.8ms	2.9ms	1.45ms	
	Track Jump(N)	0	1	1	1	64	32	16	8	
	Track Move(M)					128	64	32	16	

Note: ***1. GAIN SET**

It is possible to set TG1 and TG2 independently.
When the anti-shock is 1 (00011xxx), invert both TG1 and TG2 when the internal anti-shock is H.

***2 TRACKING MODE**

	D3	D2
OFF	0	0
ON	0	1
FWD JUMP	1	0
REV JUMP	1	1

***3 SLED MODE**

	D1	D0
OFF	0	0
ON	0	1
FWD MOVE	1	0
REV MOVE	1	1

***4 AUTO SEZUENCE**

	AS3	AS2	AS1	AS0
CANCEL	0	0	0	0
FOCUS ON	0	1	1	1
1 TRACK JUMP	1	0	0	X
10 TRACK JUMP	1	0	1	X
2N TRACK JUMP	1	1	0	X
M TRACK MOVE	1	1	1	X

XX = 0 FORVARD
X = 1 REVERSE

- When CANCEL $40 is sent, the status immediately preceding the auto sequence mode (just before $4X is sent) is reset.
- The auto sequence mode starts with the first falling of the pin 40 input pulse (WDCK) after the $4X transfer and the falling of latch pulse.

***5 RAM SET**

- Values $0 to SE (not $F) can be set.
- The above set values are ones when WDCK (88.2KHz) is input to pin 40.
- The RAM is preset when the power is switched on and the internal initial/set values are as follows:

Address				Data			
0	1	0	1	0	1	0	1
0	1	1	0	0	1	1	1
0	1	1	1	1	1	1	0

• The actual count values are slightly different from the set values.

A	set value + 4 to 5	WDCK
B, D, E	set value + 3	WDCK
C	set value + 5	WDCK
N, M	set vlaue + 3	Count out

SERIAL DATA TRUTH TABLE

Serial Data	Hexa	Function
FOCUS CONTROL		**FS = 4321**
0 0 0 0 0 0 0 0	$00	0 0 0 0
0 0 0 0 0 0 0 1	$01	0 0 0 1
0 0 0 0 0 0 1 0	$02	0 0 1 0
0 0 0 0 0 0 1 1	$03	0 0 1 1
0 0 0 0 0 1 0 0	$04	0 1 0 0
0 0 0 0 0 1 0 1	$05	0 1 0 1
0 0 0 0 0 1 1 0	$06	0 1 1 0
0 0 0 0 0 1 1 1	$07	0 1 1 1
0 0 0 0 1 0 0 0	$08	1 0 0 0
0 0 0 0 1 0 0 1	$09	1 0 0 1
0 0 0 0 1 0 1 0	$0A	1 0 1 0
0 0 0 0 1 0 1 1	$0B	1 0 1 1
0 0 0 0 1 1 0 0	$0C	1 1 0 0
0 0 0 0 1 1 0 1	$0D	1 1 0 1
0 0 0 0 1 1 1 0	$0E	1 1 1 0
0 0 0 0 1 1 1 1	$0F	1 1 1 1
TRACKING CONTROL		**AS=0** **AS=1**
		TG=2 1 TG=2 1
0 0 0 1 0 0 0 0	$10	0 0 0 0
0 0 0 1 0 0 0 1	$11	0 1 0 1
0 0 0 1 0 0 1 0	$12	1 0 1 0
0 0 0 1 0 0 1 1	$13	1 1 1 1
0 0 0 1 0 1 0 0	$14	0 0 0 0
0 0 0 1 0 1 0 1	$15	0 1 0 1
0 0 0 1 0 1 1 0	$16	1 0 1 0
0 0 0 1 0 1 1 1	$17	1 1 1 1
0 0 0 1 1 0 0 0	$18	0 0 0 0
0 0 0 1 1 0 0 1	$19	0 1 0 1
0 0 0 1 1 0 1 0	$1A	1 0 1 0
0 0 0 1 1 0 1 1	$1B	1 1 1 1
0 0 0 1 1 1 0 0	$1C	0 0 0 0
0 0 0 1 1 1 0 1	$1D	0 1 0 1
0 0 0 1 1 1 1 0	$1E	1 0 1 0
0 0 0 1 1 1 1 1	$1F	1 1 1 1

Serial Data	Hexa.	Function		
TRACKING MODE		DIRC = 1 TM =6 5 4 3 2 1	DIRC = 0 6 5 4 3 2 1	DIRC = 1 6 5 4 3 2 1
0 0 1 0 0 0 0 0	$20	0 0 0 0 0 0	0 0 1 0 0 0	0 0 0 0 1 1
0 0 1 0 0 0 0 1	$21	0 0 0 0 1 0	0 0 1 0 1 0	0 0 0 0 1 1
0 0 1 0 0 0 1 0	$22	0 1 0 0 0 0	0 1 1 0 0 0	1 0 0 0 0 1
0 0 1 0 0 0 1 1	$23	1 0 0 0 0 0	1 0 1 0 0 0	1 0 0 0 0 1
0 0 1 0 0 1 0 0	$24	0 0 0 0 0 1	0 0 0 1 0 0	0 0 0 0 1 1
0 0 1 0 0 1 0 1	$25	0 0 0 0 1 1	0 0 0 1 1 0	0 0 0 0 1 1
0 0 1 0 0 1 1 0	$26	0 1 0 0 0 1	0 1 0 1 0 0	1 0 0 0 0 1
0 0 1 0 0 1 1 1	$27	1 0 0 0 0 1	1 0 0 1 0 0	1 0 0 0 0 1
0 0 1 0 1 0 0 0	$28	0 0 0 1 0 0	0 0 1 0 0 0	0 0 0 0 1 1
0 0 1 0 1 0 0 1	$29	0 0 0 1 1 0	0 0 1 0 1 0	0 0 0 0 1 1
0 0 1 0 1 0 1 0	$2A	0 1 0 1 0 0	0 1 1 0 0 0	1 0 0 0 0 1
0 0 1 0 1 0 1 1	$2B	1 0 0 1 0 0	1 0 1 0 0 0	1 0 0 0 0 1
0 0 1 0 1 1 0 0	$2C	0 0 1 0 0 0	0 0 0 1 0 0	0 0 0 0 1 1
0 0 1 0 1 1 0 1	$2D	0 0 1 0 1 0	0 0 0 1 1 0	0 0 0 0 1 1
0 0 1 0 1 1 1 0	$2E	0 1 1 0 0 0	0 1 0 1 0 0	1 0 0 0 0 1
0 0 1 0 1 1 1 1	$2F	1 0 1 0 0 0	1 0 0 1 0 0	1 0 0 0 0 1

APPLICATION CIRCUIT

1. ±5V SPLIT POWER SUPPLY

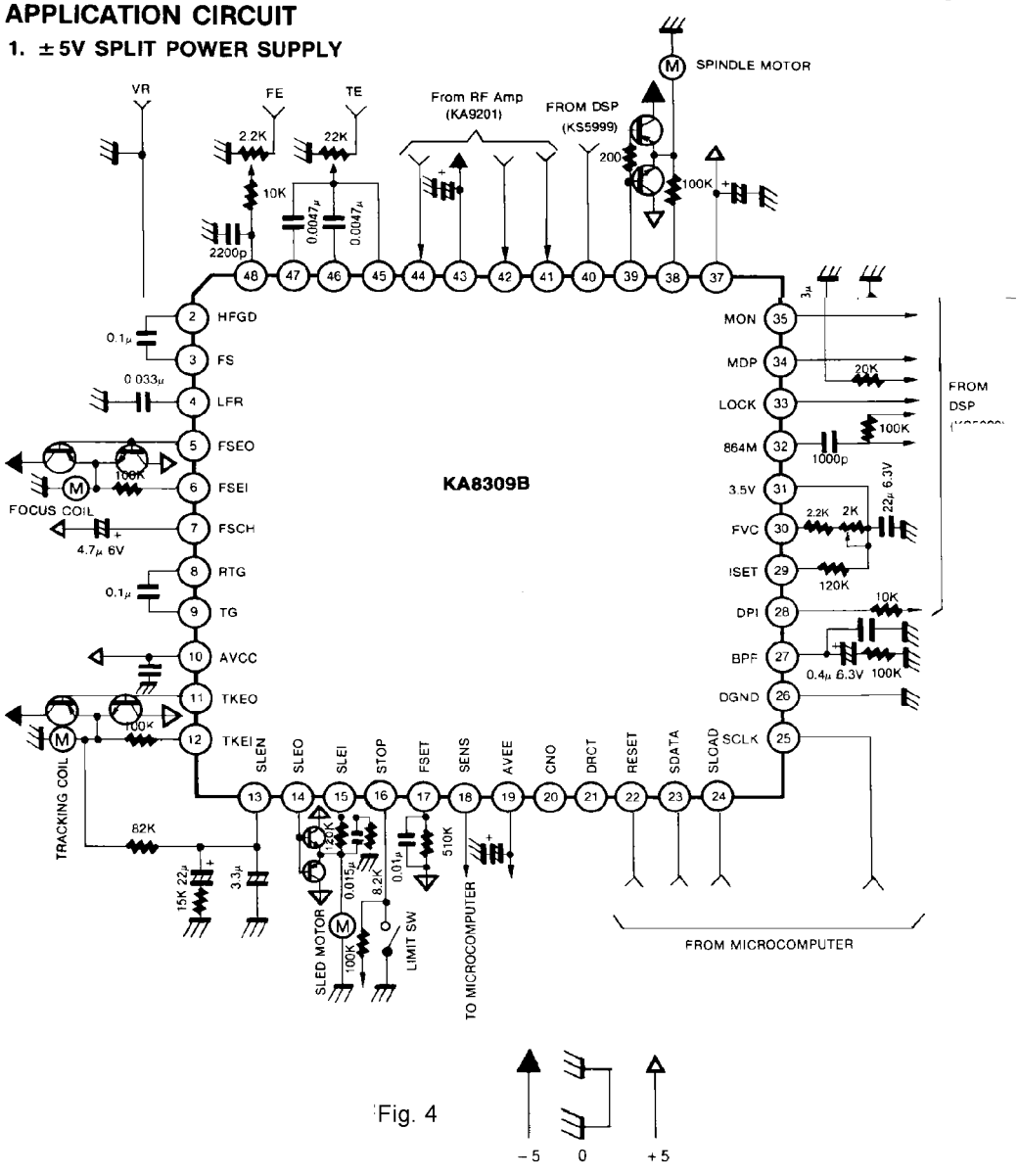


Fig. 4

2. +5V SINGLE POWER SUPPLY

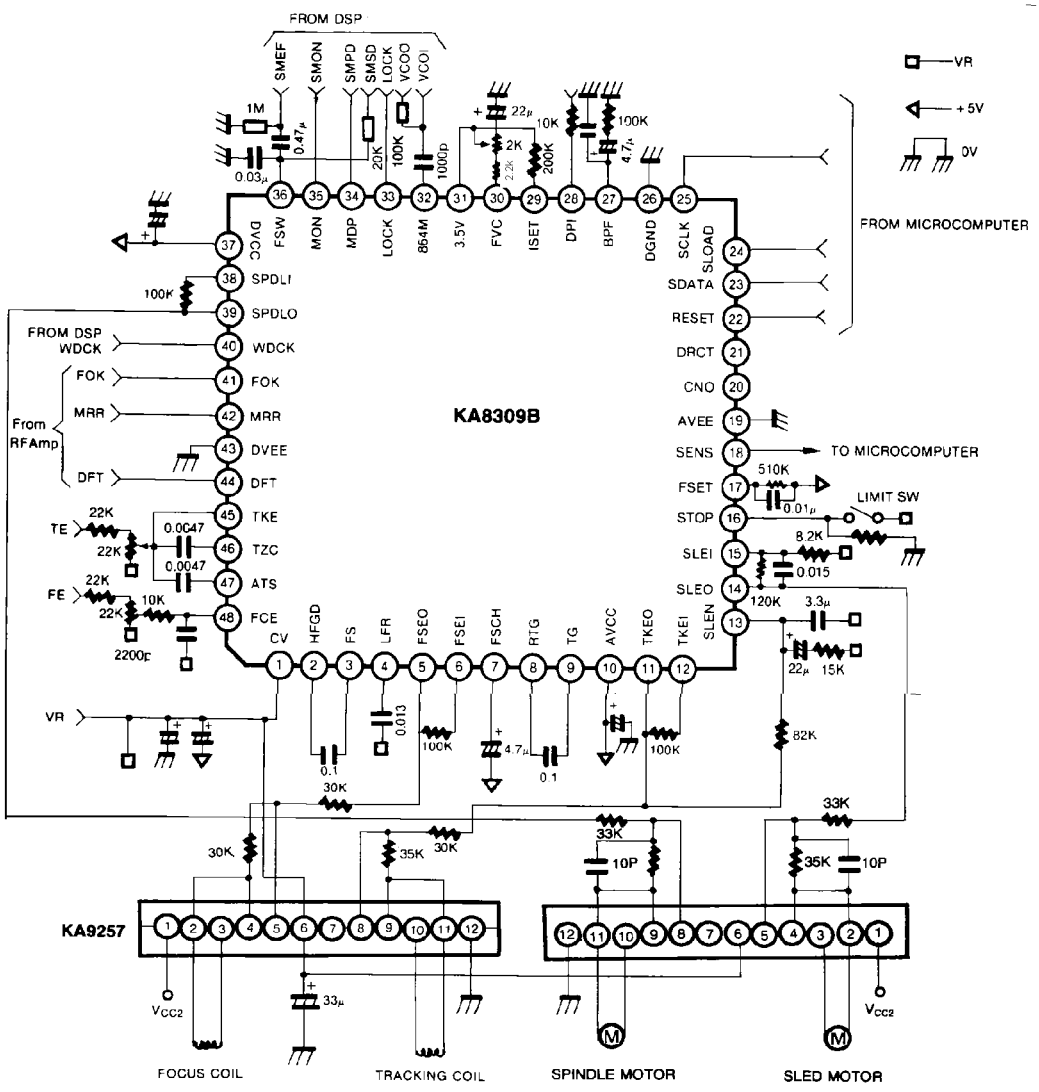
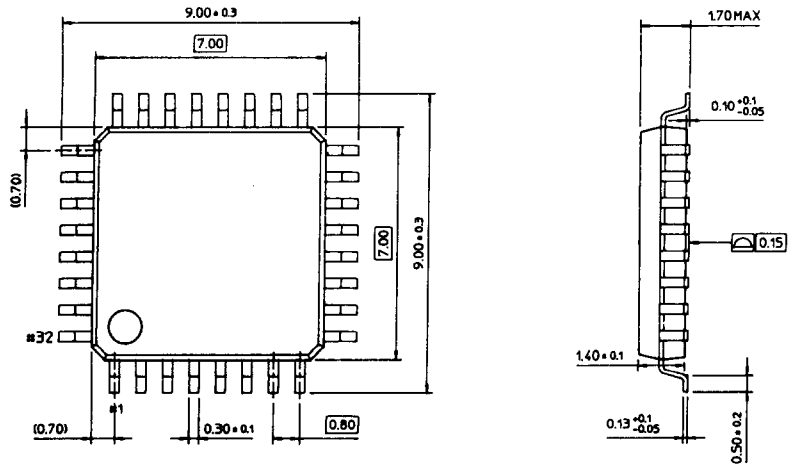


Fig. 5

Dimensions in Milimeters

32-QFP-0707



48-QFP-1010D