

Features at 2.7V

- 136µA supply current per amplifier
- 4.9MHz bandwidth

FAIRCHIL

SEMICONDUCTOR

- Output swings to within 20mV of either rail
- Input voltage range exceeds the rail by >250mV
- 5.3V/µs slew rate
- 16mA output current
- 21nV/√Hz input voltage noise
- Directly replaces MAX4126, OPA2340, LMV822, and TLV2462 in single supply applications
- Available in SOIC-8 and MSOP-8 package options

Applications

- Portable/battery-powered applications
- PCMCIA, USB
- Mobile communications, cellular phones, pagers
- Notebooks and PDA's
- Sensor Interface
- A/D buffer
- Active filters
- Signal conditioning
- Portable test instruments

KM4270 Packages



MSOP



General Description

The KM4270 is an ultra-low cost, low power, voltage feedback amplifier. At 5V, the KM4270 uses only 160μ A of supply current per amplifier and is designed to operate from a supply range of 2.5V to 5.5V (±1.25V to 2.75V). The input voltage range exceeds the negative and positive rails.

The KM4270 offers high bipolar performance at a low CMOS price. The KM4270 offers superior dynamic performance with a 4.9MHz small signal bandwidth and $5.3V/\mu s$ slew rate. The combination of low power, high bandwidth, and rail-to-rail performance make the KM4270 well suited for battery-powered communication/computing systems.

The KM4170 (single) and KM4470 (quad) are also available.







KM4270 Electrical Characteristics (V_s = +2.7V, G = 2, R_L = 10k Ω to V_s/2, R_f = 5k Ω ; unless noted)

Parameters	Conditions	ТҮР	Min & Max	UNITS	NOTES
Case Temperature		+25°C	+25°C		
Frequency Domain Response -3dB bandwidth		4.9 3.7		MHz MHz	1
full power bandwidth gain bandwidth product	$G = +2, V_0^0 = 2V_{pp}^{pp}$	1.4 2.2		MHz MHz	
Time Domain Response	11/	102			
rise and fall time overshoot	1V step 1V step	163 <1		ns %	
slew rate	1V step	5.3		V/μs	
Distortion and Noise Response		70			
2nd harmonic distortion 3rd harmonic distortion	1V _{pp} , 10kHz 1V _{pp} , 10kHz 1V _{pp} , 10kHz	-72 -72		dBc dBc	
THD	$1V_{pp}$, $10KHz$ $1V_{pp}$, $10kHz$	0.03		ивс %	
input voltage noise	>10kHz	21		nV/√Hz	
DC Performance		0.5			2
input offset voltage average drift		0.5	±6	mV μV/°C	2
input bias current		90	420	nA	2
average drift	56	32		pA/°C	
power supply rejection ratio open loop gain	DC R ₁ = $10k\Omega$	83 90	55	dB dB	2
quiescent current per channel		136	190	μΑ	2
Input Characteristics					
input resistance		12 2		MΩ	
input capacitance input common mode voltage range		-0.25 to 2.95		pF V	
common mode rejection ratio	DC, $V_{cm} = 0V$ to V_s	81	55	dB	2
Output Characteristics		0.02.1.2.00	0.00 ++ 0.04		
output voltage swing	$R_{L} = 10k\Omega \text{ to } V_{s}/2$ $R_{L} = 1k\Omega \text{ to } V_{s}/2$ $R_{L} = 200\Omega \text{ to } V_{s}/2$	0.02 to 2.68 0.05 to 2.63 0.11 to 2.52	0.06 to 2.64		2
output current		±16		mA	
power supply operating range		2.7	2.5 to 5.5	V	

Min/max ratings are based on product characterization and simulation. Individual parameters are tested as noted. Outgoing quality levels are determined from tested parameters.

NOTES:

1) For G = +1, $R_f = 0$. 2) 100% tested at +25°C.

Absolute Maximum Ratings

Package Thermal Resistance

supply voltage	0 to +6V	Package	Θ_{A}	
maximum junction temperature	+175°C	8 lead SOIC	152°C/W	
storage temperature range	-65°C to +150°C	8 lead MSOP	206°C/W	
lead temperature (10 sec)	+260°C			
operating temperature range (recom	mended) -40°C to +85°C			
input voltage range	+V _s + 0.5V, -V _s - 0.5V			

KM4270 Electrical	Characteristics ($V_s = +5V$, G = 2, $R_L = 10k\Omega$ to $V_s/2$, $R_f = 5k\Omega$; unless noted)

Parameters	Conditions	ТҮР	Min & Max	UNITS	NOTES
Case Temperature		+25°C	+25°C		
Frequency Domain Response -3dB bandwidth		4.3 3.0		MHz MHz	1
full power bandwidth gain bandwidth product	$G = +2, V_0^0 = 2V_{pp}$	2.3 2.0		MHz MHz	
Time Domain Response rise and fall time overshoot slew rate	1V step 1V step 1V step	110 <1 9		ns % V/µs	
Distortion and Noise Response 2nd harmonic distortion 3rd harmonic distortion THD input voltage noise	2V _{pp} , 10kHz 2V ^{pp} , 10kHz 2V _{pp} , 10kHz >10kHz	-73 -75 0.03 22		dBc dBc % nV/√Hz	
DC Performance input offset voltage average drift input bias current average drift power supply rejection ratio open loop gain quiescent current per channel	DC R _L = 10kΩ	1.5 15 90 40 60 80 160		mV μV/°C nA pA/°C dB dB μA	
Input Characteristics input resistance input capacitance input common mode voltage range common mode rejection ratio	DC, $V_{cm} = 0V$ to V_s	12 2 -0.25 to 5.25 85		MΩ pF V dB	
Output Characteristics output voltage swing	$R_{L} = 10k\Omega \text{ to V}/2$ $R_{L} = 1k\Omega \text{ to V}/2$ $R_{L} = 200\Omega \text{ to V}/2$	0.04 to 4.96 0.07 to 4.9 0.14 to 4.67		V V V	
output current power supply operating range		±30 5.0	2.5 to 5.5	mA V	

Min/max ratings are based on product characterization and simulation. Individual parameters are tested as noted. Outgoing quality levels are determined from tested parameters.

NOTES:

1) For G = +1, $R_f = 0$.

KM4270 Performance Characteristics ($V_s = +2.7$, G = 2, $R_L = 10k\Omega$ to $V_s/2$, $R_f = 5k\Omega$; unless noted)





KM4270 Performance Characteristics ($V_s = +2.7V$, G = 2, $R_L = 10k\Omega$ to $V_s/2$, $R_f = 5k\Omega$; unless noted)





General Description

The KM4270 is single supply, general purpose, voltagefeedback amplifier. The KM4270 is fabricated on a complimentary bipolar process, features a rail-to-rail input and output, and is unity gain stable.

The typical non-inverting circuit schematic is shown in Figure 1.



Overdrive Recovery

Overdrive of an amplifier occurs when the output and/or input ranges are exceeded. The recovery time varies based on whether the input or output is overdriven and by how much the ranges are exceeded. The KM4270 will typically recover in less than 50ns from an overdrive condition. Figure 3 shows the KM4270 in an overdriven condition.



Figure 3: Overdrive Recovery

Figure 1: Typical Non-inverting Configuration

Input Common Mode Voltage

The common mode input range extends to 250mV below ground and to 250mV above V_s , in single supply operation. Exceeding these values will not cause phase reversal. However, if the input voltage exceeds the rails by more than 0.5V, the input ESD devices will begin to conduct. The output will stay at the rail during this overdrive condition. If the absolute maximum input voltage (700mV beyond either rail) is exceeded, externally limit the input current to ±5mA as shown in Figure 2.



Figure 2: Circuit for Input Current Protection

Power Dissipation

The maximum internal power dissipation allowed is directly related to the maximum junction temperature. If the maximum junction temperature exceeds 150°C, some performance degradation will occur. It the maximum junction temperature exceeds 175°C for an extended time, device failure may occur.

Driving Capacitive Loads

The *Frequency Response vs.* C_L plot, illustrates the response of the KM4270. A small series resistance (R_s) at the output of the amplifier, illustrated in Figure 4, will improve stability and settling performance. R_s values in the *Frequency Response vs.* C_L plot were chosen to achieve maximum bandwidth with less than 2dB of peaking. For maximum flatness, use a larger R_s . As the plot indicates, the KM4270 can easily drive a 50pF capacitive load without a series resistance.





Driving a capacitive load introduces phase-lag into the output signal, which reduces phase margin in the amplifier. The unity gain follower is the most sensitive configuration. In a unity gain follower configuration, the KM4270 requires a 510Ω series resistor to drive a 100pF load.

Layout Considerations

General layout and supply bypassing play major roles in high frequency performance. Fairchild has evaluation boards to use as a guide for high frequency layout and as aid in device testing and characterization. Follow the steps below as a basis for high frequency layout:

- \bullet Include 6.8µF and 0.01µF ceramic capacitors
- \bullet Place the 6.8µF capacitor within 0.75 inches of the power pin
- \bullet Place the $0.01 \mu F$ capacitor within 0.1 inches of the power pin
- Remove the ground plane under and around the part, especially near the input and output pins to reduce parasitic capacitance
- Minimize all trace lengths to reduce series inductances

Refer to the evaluation board layouts shown in Figure 6 for more information.

Evaluation Board Information

The following evaluation boards are available to aid in the testing and layout of this device:

Eval Boar	d Description	Products
KEB006	Dual Channel, Dual Supply, 8 lead SOIC	KM4270IC8
KEB010	Dual Channel, Dual Supply, 8 lead MSOP	KM4270IM8

Evaluation board schematics and layouts are shown in Figure 5 and Figure 6.



Figure 5: Evaluation Board Schematic

KM4270 Evaluation Board Layout



Figure 6a: KEB006 (top side)



Figure 6b: KEB006 (bottom side)

KOTA LAYER1 SILK



Figure 6c: KEB010 (top side)





KOTA LAYER2

KM4270 Package Dimensions

SOIC



D







SOIC-8					
SYMBOL	MIN MAX				
A1	0.10	0.25			
В	0.36	0.46			
С	0.19	0.25			
D	4.80	4.98			
E	3.81	3.99			
е	1.27	BSC			
Н	5.80	6.20			
h	0.25	0.50			
L	0.41	1.27			
A	1.52	1.72			
	0°	8°			
ZD	0.53 ref				
A2	1.37 1.57				

NOTE:

All dimensions are in millimeters.

- 2. Lead coplanarity should be 0 to 0.10mm (.004") max.
- Package surface finishing: (2.1) Top: matte (charmilles #18~30). (2.2) All sides: matte (charmilles #18~30).
- (2.3) Bottom: smooth or matte (chamilles #18-30).
 All dimensions excluding mold flashes and end flash from the package body shall not exceed o.152mm (.006) , per side(d).



	MSOP-8	
SYMBOL	MIN	MAX
А	1.10	-
A1	0.10	±0.05
A2	0.86	±0.08
D	3.00	±0.10
D2	2.95	±0.10
E	4.90	±0.15
E1	3.00	±0.10
E2	2.95	±0.10
E3	0.51	±0.13
E4	0.51	±0.13
R	0.15	+0.15/-0.06
R1	0.15	+0.15/-0.06
t1	0.31	±0.08
t2	0.41	±0.08
b	0.33	+0.07/-0.08
b1	0.30	±0.05
С	0.18	±0.05
c1	0.15	+0.03/-0.02
01	3.0°	±3.0°
02	12.0°	±3.0°
03	12.0°	±3.0°
L	0.55	±0.15
L1	0.95 BSC	-
aaa	0.10	-
bbb	0.08	-
CCC	0.25	-
е	0.65 BSC	-
S	0.525 BSC	-

NOTE:

- 1 All dimensions are in millimeters (angle in degrees), unless otherwise specified.
- \triangle Datums -B- and -C- to be determined at datum plane -H-.
- \triangle Dimensions "D" and "E1" are to be determined at datum -H-.
- $\underline{\land}$ Dimensions "D2" and "E2" are for top package and dimensions "D" and "E1" are for bottom package.
- $\underline{\texttt{S}}$ Cross sections A A to be determined at 0.13 to 0.25mm from the leadtip.
- A Dimension "D" and "D2" does not include mold flash, protrusion or gate burrs.
- A Dimension "E1" and "E2" does not include interlead flash or protrusion.

Ordering Information

Model	Part Number	Package	Container	Pack Qty
KM4270	KM4270IC8	SOIC-8	Rail	95
	KM4270IC8TR3	SOIC-8	Reel	2500
	KM4270IM8	MSOP-8	Rail	50
	KM4270IM8TR3	MSOP-8	Reel	4000

Temperature range for all parts: -40°C to +85°C.

DISCLAIMER

FAIRCHILD SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICES TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION OR DESIGN. FAIRCHILD DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS.

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

- Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury of the user.
- A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.