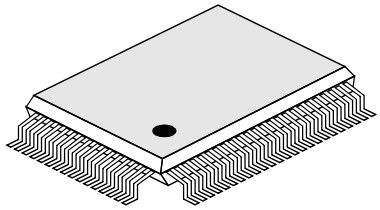
VIDEO ENCODER

The KS0119 combines NTSC encoding with conventional RAM-DAC functions so that digitized video or computer generated graphics can be displayed on either NTSC or PC monitors. There are two data input channels which allow mixing. Provision is also made for analog mixing at the output. Operation modes can be programmed under host control. The KS0119 can be used with other members of the Samsung multimedia chip set in a typical desktop multimedia environment.

80 or 100 PQFP



FEATURES

- **Accepts true color; high color; color indexed; CCIR 601 4:4:4, 4:2:2, 4:1:1, or 2:1:1 formatted video inputs**
- **Supports analog NTSC CVBS, S-VIDEO, or RGB display**
- **Fully programmable timing generation; supports CGA, VGA, SVGA display up to 45 MHz pixel clock rate (with 100 pin package)**
- **Accepts up to 2 input channels for digital mixing**
- **Operate as slave or master in timing generation**
- **Supports alpha, chroma, and window keying for digital mixing**
- **Provides an analog RGB mixing function**
- **Contains 3 256X8 color palette tables and 3 15X8 overlay color look up tables**
- **Contains 3 10-bit video grade DACs**
- **Provides a parallel microprocessor or a 3-wire serial interface**
- **Contains a two way color space converter: RGB -> NTSC, YCbCr -> RGB**
- **Supports power down mode**

ORDERING INFORMATION

Device	Package	Temp. Range	Max. CKV
KS0119	80-QFP	0° ~ +65°C	32 MHz
KS0119Q2	100-QFP	0° ~ +65°C	45 MHz

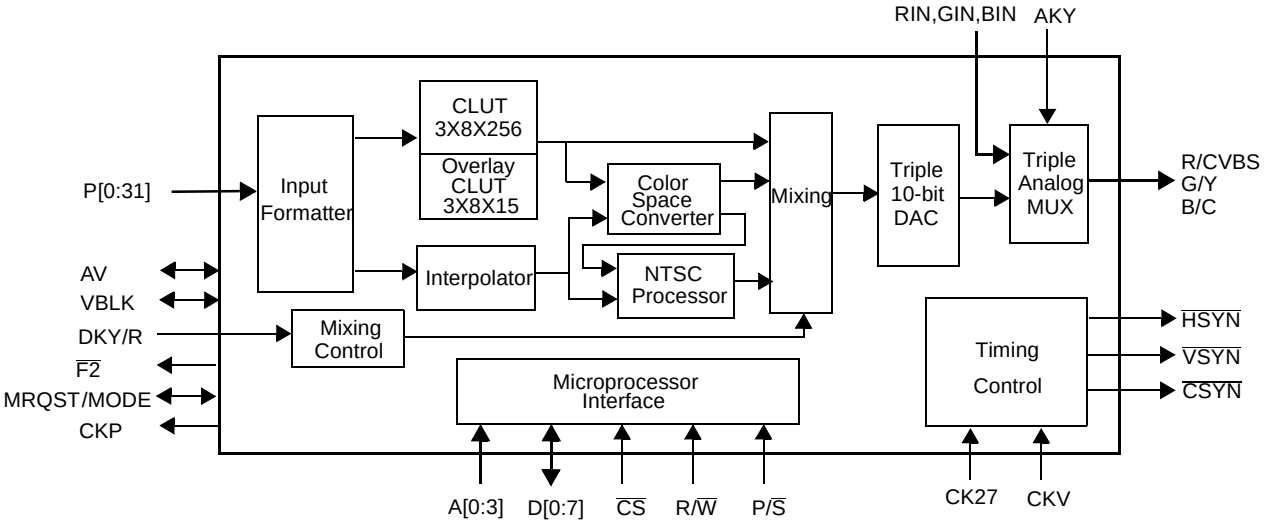
APPLICATIONS

- **PC Video**
- **RAM DAC, Gamma Correction**
- **YUV DAC for MPEG, JPEG Play Back**
- **NTSC Video Encoder**

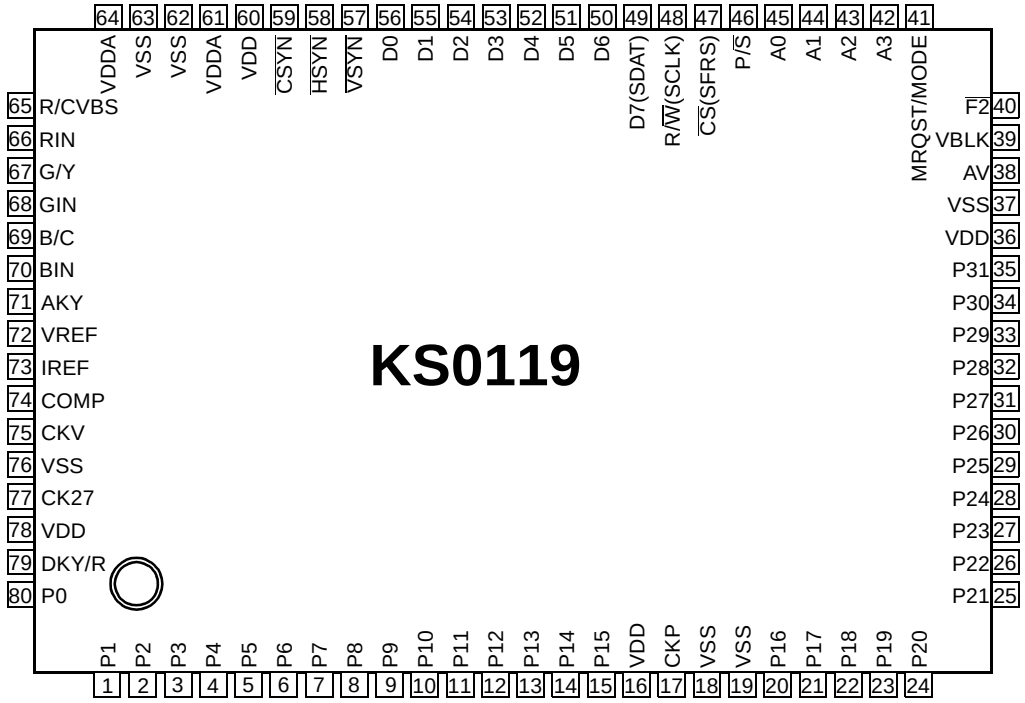
RELATED PRODUCT

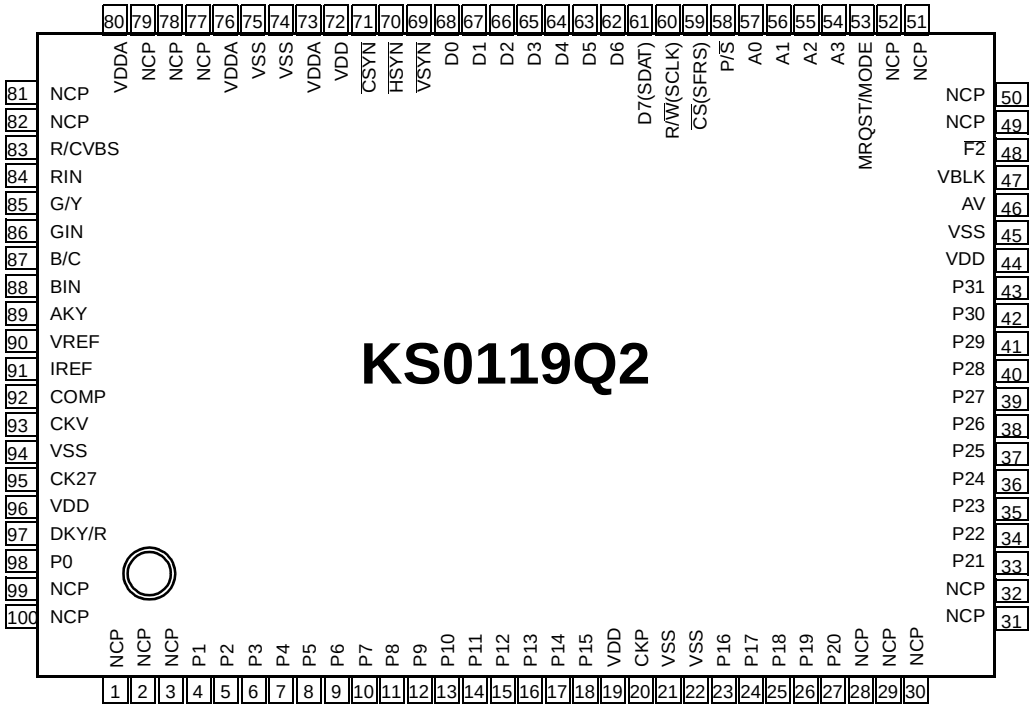
- **KS0122 MULTISTANDARD VIDEO DECODER**

BLOCK DIAGRAM



PIN ASSIGNMENT





TYPICAL APPLICATIONS

The KS0119 is shown in a VGA overlay application with the KS0122 Multistandard Video Decoder in Figure 1.

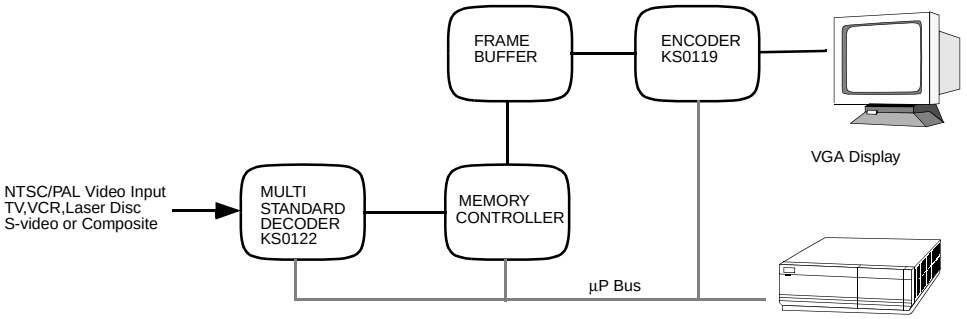


Figure 1. VGA Overlay

Figure 2 shows a video CD playback system using the KS0119 as a video encoder.

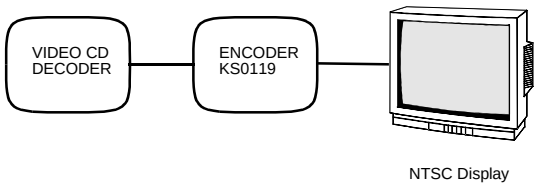


Figure 2. Video CD Playback

PIN DESCRIPTION

Pin Name	Pin # (80)	Pin # (100)	Type	Description
VIDEO BUFFER INTERFACE				
P0 - P31	80,1-15, 20 - 35	98,4-18, 23-27,33-43	I	Digital video input bus.
$\overline{F2}$	40	48	O	Field 2 indicator. Active low signal.
MRQST /MODE	41	53	I/O	Dual function pin. During power-on, it is an input and its logic state determines whether the chip operates in NTSC mode or VGA pass through mode. A 4.7 K pull-up resistor sets the chip in VGA pass through mode. Otherwise it defaults to NTSC mode. After power-on this pin becomes an output and is high during active lines' sync tip.
AV	38	46	I/O	Active video indicator. Input in slave mode; output in master mode.
VBLK	39	47	I/O	Vertical blank. Input in slave mode; output in master mode.
CKP	17	20	O	Pixel clock output.
DKY/R	79	97	I	Dual function input pin. Configured by the **CMD** register bit 2. It can be used as either digital mixing or hardware RUN input. Please refer to the command register description for more detail.
ANALOG MULTIPLEXER INPUT				
RIN	66	84	I	Analog R input to the analog mixing multiplexer.
GIN	68	86	I	Analog G input to the analog mixing multiplexer.
BIN	70	88	I	Analog B input to the analog mixing multiplexer.
AKY	71	89	I	Analog multiplexer control. A logic '0' connects analog RGB inputs to the output pins. A '1' connects DACs' outputs to the output pins.
VIDEO OUTPUT PORT				
$\overline{HSYN}$	58	70	O	Horizontal Sync. Active low, TTL signal for monitor. In the pass through mode HSYN is the inverted AV (pin 38).
$\overline{VSYN}$	57	69	O	Vertical Sync. Active low, TTL signal for monitor. In the pass through mode VSYN is the inverted VBLK (pin 39)
$\overline{CSYN}$	59	71	O	Composite Sync. Active low, TTL signal for monitor.
R/CVBS	65	83	O	Either an analog R or Composite output, controlled by **CMD** bits 5 and 1. It can drive a 37.5 Ω load (doubly terminated 75 Ω load).
G/Y	67	85	O	Either an analog G or S-video Y output, controlled by **CMD** bits 5 and 1. It can drive a 37.5 Ω load.
B/C	69	87	O	Either an analog B or S-video C output, controlled by **CMD** bits 5 and 1. It can drive a 37.5 Ω load.

PIN DESCRIPTION (Continued)

Pin Name	Pin # (80)	Pin # (100)	Type	Description
REFERENCE AND COMPENSATION				
VREF	72	90	I/O	Voltage reference. It has an internal voltage reference circuit, but may be overridden by an external voltage reference input. A 0.1 μF ceramic capacitor is required between this pin and GND.
IREF	73	91	I	A resistor is connected between this pin and GND to control the DAC output current.
COMP	74	92	I	Compensation capacitor for the DAC internal reference amplifier. A 0.1 μF ceramic capacitor is required between this pin and VDDA.
HOST INTERFACE				
P/$\overline{S}$	46	58	I	Microprocessor interface configuration control. Tie to VDD to select parallel mode. Tie to VSS to select serial mode.
$\overline{CS}$ (SFRS)	47	59	I	Chip select strobe in parallel mode (Frame Sync in serial mode).
R/$\overline{W}$ (SCLK)	48	60	I	Read/write in parallel mode (Serial clock in serial mode).
D7 (SDAT)	49	61	I/O	Data bus msb in parallel mode (Serial data in serial mode).
D0 - D6	56-50	68-62	I/O	Parallel data bus bit 0 to 6.
A0 - A3	45-42	57-54	I	Address bus for parallel interface.
CLOCK INPUT				
CKV	75	93	I	Clock input used to generate pixel clock for VGA display.
CK27	77	95	I	27 MHz clock input, required for NTSC display.
POWER AND GROUND				
VDD	16,36, 60,78	19,44,72,96	+5V	Digital power supply.
VSS	18,19, 37,62, 63,76	21,22,45,74, 75,94	GND	Digital ground.
VDDA	61,64	76,80	+5V	Analog power supply.
NCP				
NCP	N/A	1-3,28-32, 49-52,77-79,81,82,99, 100	-	These pins are directly connected to the die substrate. They are intended as heat dissipation points. It is recommended that each corner set of NCP pins be connected to as large as possible solid metal plane on the PCB component surface side. If electrical connect is desired (not required) only connection to VDDA is allowed.

PIN CROSS REFERENCE (Numerical Order by Pin Number):

80-PQFP

Pin #	Pin Name	Pin #	Pin Name	Pin #	Pin Name	Pin #	Pin Name
1	P1	21	P17	41	MRQST/MODE	61	VDDA
2	P2	22	P18	42	A3	62	VSS
3	P3	23	P19	43	A2	63	VSS
4	P4	24	P20	44	A1	64	VDDA
5	P5	25	P21	45	A0	65	R/CVBS
6	P6	26	P22	46	P/$\overline{S}$	66	RIN
7	P7	27	P23	47	$\overline{CS}$(SFRS)	67	G/Y
8	P8	28	P24	48	R/$\overline{W}$(SCLK)	68	GIN
9	P9	29	P25	49	D7(SDAT)	69	B/C
10	P10	30	P26	50	D6	70	BIN
11	P11	31	P27	51	D5	71	AKY
12	P12	32	P28	52	D4	72	VREF
13	P13	33	P29	53	D3	73	IREF
14	P14	34	P30	54	D2	74	COMP
15	P15	35	P31	55	D1	75	CKV
16	VDD	36	VDD	56	D0	76	VSS
17	CKP	37	VSS	57	$\overline{VSYN}$	77	CK27
18	VSS	38	AV	58	$\overline{HSYN}$	78	VDD
19	VSS	39	VBLK	59	$\overline{CSYN}$	79	DKY/R
20	P16	40	$\overline{F2}$	60	VDD	80	P0

PIN CROSS REFERENCE (Continued):

100-PQFP

Pin #	Pin Name	Pin #	Pin Name	Pin #	Pin Name	Pin #	Pin Name
1	NCP	26	P19	51	NCP	76	VDDA
2	NCP	27	P20	52	NCP	77	NCP
3	NCP	28	NCP	53	MRQST/MODE	78	NCP
4	P1	29	NCP	54	A3	79	NCP
5	P2	30	NCP	55	A2	80	VDDA
6	P3	31	NCP	56	A1	81	NCP
7	P4	32	NCP	57	A0	82	NCP
8	P5	33	P21	58	P/$\overline{S}$	83	R/CVBS
9	P6	34	P22	59	$\overline{CS}$(SFRS)	84	RIN
10	P7	35	P23	60	R/$\overline{W}$(SCLK)	85	G/Y
11	P8	36	P24	61	D7(SDAT)	86	GIN
12	P9	37	P25	62	D6	87	B/C
13	P10	38	P26	63	D5	88	BIN
14	P11	39	P27	64	D4	89	AKY
15	P12	40	P28	65	D3	90	VREF
16	P13	41	P29	66	D2	91	IREF
17	P14	42	P30	67	D1	92	COMP
18	P15	43	P31	68	D0	93	CKV
19	VDD	44	VDD	69	$\overline{VSYN}$	94	VSS
20	CKP	45	VSS	70	$\overline{HSYN}$	95	CK27
21	VSS	46	AV	71	$\overline{CSYN}$	96	VDD
22	VSS	47	VBLK	72	VDD	97	DKY/R
23	P16	48	$\overline{F2}$	73	VDDA	98	P0
24	P17	49	NCP	74	VSS	99	NCP
25	P18	50	NCP	75	VSS	100	NCP

1. GENERAL DESCRIPTION

The KS0119 is a digital NTSC encoder combined with basic RAM-DAC functions. It is designed to be a high performance, cost effective NTSC or PC display driver. The chip consists of a two way Color Space Converter, which is capable of supporting almost all the popular input formats pertaining to PC video, graphics, or image compression/decompression. The chip contains signal processing blocks to enhance image quality and reduce artifacts due to sampling. It provides image manipulation facilities such as masking, mixing, hue control, and color lookup tables to create special effects. It includes a programmable Timing Generator to generate the synchronization signals and color burst for different display monitors.

1.1. Application

The KS0119 is a versatile chip, which can be used for many application such as NTSC encoding, YUV DAC, RAM DAC, Gamma correction, mixing, and VGA overlay. CK27 must be used for NTSC encoder, whereas CKV must be used for the others. It is recommended that the unused clock input pin be tied to a static state.

1.2. Power On Default

The KS0119 can be configured for two power-on default states: one for NTSC video encoding and the other for VGA overlay application. For the latter the MRQST/MODE pin must be pulled up so the KS0119 defaults to *sync pass through* mode and Channel A is set to support 8-bit pseudo color format after power up. In this mode, the KS0119 functions as a RAM-DAC. The internal video timing generator is disabled; the horizontal and vertical syncs are delay compensated for the video path delay and passed to the sync output pins. The sync pass through mode is recommended for VGA overlay application.

Table 1: Power On Default State

Power On MRQST/MODE Pin State	Operations	Channel A Input Format	SYNCPT	Clock Source
0	NTSC encoding	4:2:2 YCbCr	0	CK27
1	VGA overlay	8 bit pseudo color	1	CKV

1.3. Operation Mode

The KS0119 can be configured to operate either in master mode or slave mode. In the master mode the encoder uses the parameter stored in the CRT control registers to generate all the video timings and outputs synchronizing signals (refer to "VIDEO OPERATIONAL TIMING" on page 18). In the slave mode the encoder synchronize the internal pixel counter on the falling edge of AV**,** and line counter on the rising edge or VBLK. The sync outputs, $\overline{\text{HSYN}}$ and $\overline{\text{VSYN}}$, waveform can be modified if sync pass through is disabled (**SYNCPT**=0). Table 2 shows the registers related to the sync generation.

Table 2: Sync Output Generation

	MASTER	SLAVE	
Control Registers	**MSTR**=1	**MSTR**=0, **SYNCPT**=1	**MSTR**=0, **SYNCPT**=0
$\overline{\text{HSYN}}$, $\overline{\text{VSYN}}$	Internally generated	Pass through	Regenerated
Video Output Port Sync Polarity	Active low	Inverted AV and VBLK	Active low
Input Sync Polarity Control	N/A	**VSP**, **HSP**	
CRT Control Registers	Index Registers 70 - 79h		
Comments		Recommend for VGA overlay application	

1.4. Power Down Mode

The KS0119 supports power down mode; the DAC outputs can be put into high impedance state by turning off the current source to conserve power.

1.5. Digital Video Input Format

The digital video input is a 32 bit port. This port can be used as a single channel or logically divided into two channels: A and B. Channel A's input can be true color, color indexed, or CCIR 601 formats. Channel B's input is restricted to CCIR 601 formats.The supported formats and their bit assignments are shown in Table 3 and Table 4.

The KS0119 accepts certain input combinations from Channel A and B. However the following rules must be observed when both channels are selected (their format registers contain valid numbers):

1. Channel B's input is ignored if mixing is not enabled.
2. If mixing is enabled, channel A is the foreground and will be displayed if the mixing key is false.
3. In YC/YC mixing, both channels must have the same format (e.g. Channel A's format is 4:1:1A, Channel B's format must be 4:1:1A. See Table 3 and Table 4).

Table 3: Channel A Input Format

	FORMAT REGISTER (BIT 7 - 4)																	
VALUE	**1**	**2**	**3**	**4**	**5**	**6**	**9**		**A**		**B**				**C**			
TYPE	RGB						4:2:2		2:1:1 A		4:1:1 A				4:1:1 B			
# of Bits	24	16	16	15	12	8	16		16		12				16			
Pixel Bus	Pixel Byte Sequence																	
	N	N	N	N	N	N	2N	+1	2N	+1	4N	+1	+2	+3	4N	+1	+2	+3
P0	B0	B0	B0	B0	P0	P0	Cb0	Cr0	Cb0	Cr0					Cb0		Cr0	
P1	B1	B1	B1	B1	P1	P1	Cb1	Cr1	Cb1	Cr1					Cb1		Cr1	
P2	B2	B2	B2	B2	P2	P2	Cb2	Cr2	Cb2	Cr2					Cb2		Cr2	
P3	B3	B3	B3	B3	P3	P3	Cb3	Cr3	Cb3	Cr3					Cb3		Cr3	
P4	B4	B4	G0	B4	P4	P4	Cb4	Cr4	Cb4	Cr4	Cr6	Cr4	Cr2	Cr0	Cb4		Cr4	
P5	B5	G0	G1	G0	P5	P5	Cb5	Cr5	Cb5	Cr5	Cr7	Cr5	Cr3	Cr1	Cb5		Cr5	
P6	B6	G1	G2	G1	P6	P6	Cb6	Cr6	Cb6	Cr6	Cb6	Cb4	Cb2	Cb0	Cb6		Cr6	
P7	B7	G2	G3	G2	P7	P7	Cb7	Cr7	Cb7	Cr7	Cb7	Cb5	Cb3	Cb1	Cb7		Cr7	
P8	G0	G3	G4	G3	OVL0		Y0	Y0	Y0	Y0	Y0	Y0	Y0	Y0	Y0	Y0	Y0	Y0
P9	G1	G4	G5	G4	OVL1		Y1	Y1	Y1	Y1	Y1	Y1	Y1	Y1	Y1	Y1	Y1	Y1
P10	G2	G5	R0	R0	OVL2		Y2	Y2	Y2	Y2	Y2	Y2	Y2	Y2	Y2	Y2	Y2	Y2
P11	G3	R0	R1	R1	OVL3		Y3	Y3	Y3	Y3	Y3	Y3	Y3	Y3	Y3	Y3	Y3	Y3
P12	G4	R1	R2	R2			Y4	Y4	Y4	Y4	Y4	Y4	Y4	Y4	Y4	Y4	Y4	Y4
P13	G5	R2	R3	R3			Y5	Y5	Y5	Y5	Y5	Y5	Y5	Y5	Y5	Y5	Y5	Y5
P14	G6	R3	R4	R4			Y6	Y6	Y6	Y6	Y6	Y6	Y6	Y6	Y6	Y6	Y6	Y6
P15	G7	R4	R5	TKEY			Y7	Y7	Y7	Y7	Y7	Y7	Y7	Y7	Y7	Y7	Y7	Y7
P16	R0																	
P17	R1																	
P18	R2																	
P19	R3																	
P20	R4																	
P21	R5																	
P22	R6																	
P23	R7																	

Table 4: Channel B Input Format

	FORMAT REGISTER (BIT 3 - 0)																	
VALUE	**1**	**2**		**3**		**4**		**5**		**6**				**7**				**9**
TYPE	4:4:4	4:2:2 A		4:2:2 B		2:1:1 A		2:1:1 B		4:1:1 A				4:1:1 B				4:4:4
# of Bits	24	16		24		16		24		12				16				24
Pixel Bus	Pixel Byte Sequence																	
	N	2N	+1	2N	+1	2N	+1	2N	+1	4N	+1	+2	+3	4N	+1	+2	+3	N
P0																		Cr0
P1																		Cr1
P2																		Cr2
P3																		Cr3
P4																		Cr4
P5																		Cr5
P6																		Cr6
P7																		Cr7
P8	Cr0			Cr0				Cr0										
P9	Cr1			Cr1				Cr1										
P10	Cr2			Cr2				Cr2										
P11	Cr3			Cr3				Cr3										
P12	Cr4			Cr4				Cr4										
P13	Cr5			Cr5				Cr5										
P14	Cr6			Cr6				Cr6										
P15	Cr7			Cr7				Cr7										
P16	Cb0	Cb0	Cr0	Cb0		Cb0	Cr0	Cb0						Cb0		Cr0		Cb0
P17	Cb1	Cb1	Cr1	Cb1		Cb1	Cr1	Cb1						Cb1		Cr1		Cb1
P18	Cb2	Cb2	Cr2	Cb2		Cb2	Cr2	Cb2						Cb2		Cr2		Cb2
P19	Cb3	Cb3	Cr3	Cb3		Cb3	Cr3	Cb3						Cb3		Cr3		Cb3
P20	Cb4	Cb4	Cr4	Cb4		Cb4	Cr4	Cb4		Cr6	Cr4	Cr2	Cr0	Cb4		Cr4		Cb4
P21	Cb5	Cb5	Cr5	Cb5		Cb5	Cr5	Cb5		Cr7	Cr5	Cr3	Cr1	Cb5		Cr5		Cb5
P22	Cb6	Cb6	Cr6	Cb6		Cb6	Cr6	Cb6		Cb6	Cb4	Cb2	Cb0	Cb6		Cr6		Cb6
P23	Cb7	Cb7	Cr7	Cb7		Cb7	Cr7	Cb7		Cb7	Cb5	Cb3	Cb1	Cb7		Cr7		Cb7
P24	Y0	Y0	Y0	Y0	Y0	Y0	Y0	Y0	Y0	Y0	Y0	Y0	Y0	Y0	Y0	Y0	Y0	Y0
P25	Y1	Y1	Y1	Y1	Y1	Y1	Y1	Y1	Y1	Y1	Y1	Y1	Y1	Y1	Y1	Y1	Y1	Y1
P26	Y2	Y2	Y2	Y2	Y2	Y2	Y2	Y2	Y2	Y2	Y2	Y2	Y2	Y2	Y2	Y2	Y2	Y2
P27	Y3	Y3	Y3	Y3	Y3	Y3	Y3	Y3	Y3	Y3	Y3	Y3	Y3	Y3	Y3	Y3	Y3	Y3
P28	Y4	Y4	Y4	Y4	Y4	Y4	Y4	Y4	Y4	Y4	Y4	Y4	Y4	Y4	Y4	Y4	Y4	Y4
P29	Y5	Y5	Y5	Y5	Y5	Y5	Y5	Y5	Y5	Y5	Y5	Y5	Y5	Y5	Y5	Y5	Y5	Y5
P30	Y6	Y6	Y6	Y6	Y6	Y6	Y6	Y6	Y6	Y6	Y6	Y6	Y6	Y6	Y6	Y6	Y6	Y6
P31	Y7	Y7	Y7	Y7	Y7	Y7	Y7	Y7	Y7	Y7	Y7	Y7	Y7	Y7	Y7	Y7	Y7	Y7

2. DIGITAL MIXING

The KS0119 supports digital mixing between the two input channels. Digital mixing is the process of replacing a selected area in the foreground (Channel A) with the corresponding area in the background (Channel B) according to the output of the keying function. The result is that the foreground objects appear situated in front of the background's. Mixing is an indispensable tool to create special effects, such as animation, picture in picture, and video overlay. The ability to select a small area to display can be used to reduce or hide the image download time during presentations. The digital mixing is controlled by the Mixing Control Register (**MXCTR**) and control registers 05h to 0Dh.

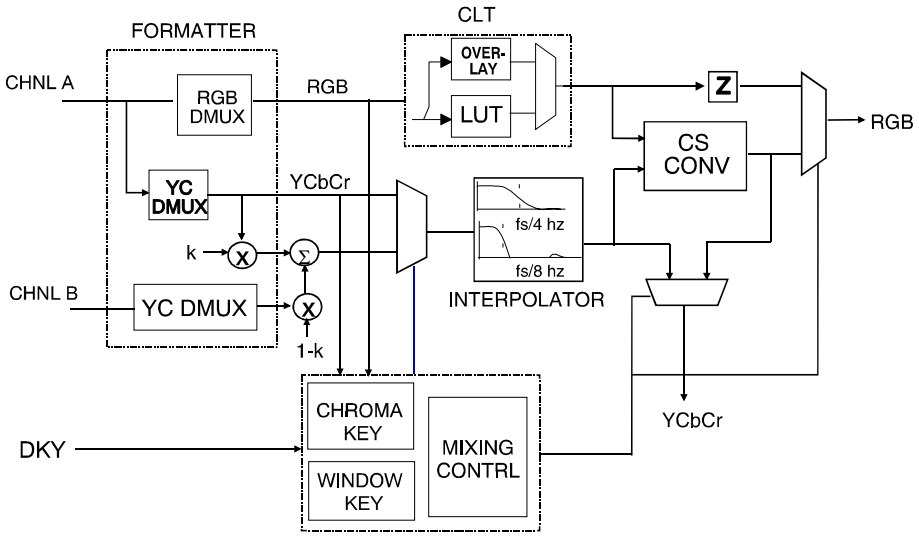


Figure 3. Digital Mixer Signal Flow Diagram

2.1. Mixing Methods

The KS0119 supports two types of mixing: RGB/YC and YC/YC.

2.1.1. RGB/YC Mixing

RGB/YC mixing is automatically selected if channel A's format is either high color or pseudo color. The process simply replaces channel A's video with Channel B's when the output of the Keying function is 1.

2.1.2. YC/YC Mixing

If channel A's input is YCbCr formatted (format register value greater than 7), then YC/YC mixing is selected. In YC/YC mixing, when the output of the Keying function is 1, the Channel A's chrominance components are replaced with Channel B's, while the luminance signals are linearly blended according to the equation

$$Yout = \frac{1}{8} \cdot [K \cdot Ya + (1 - K) \cdot Yb]$$

where K is a programmable value, from 0 to 7, stored in the **Mixing Control** register (**MXCTR**). Linear Mixing preserves the shadows inside the keyed area.

2.2. Keying Methods

The KS0119 supports Window Keying, Index Keying, Chroma Keying, Alpha Keying, External Keying, and certain combinations of them. These are described in detail below.

2.2.1. Index Keying

If channel A's input format is 2, 3, 4, 5, or 6, Index Keying can be used for mixing. Channel A's inputs are first compared with the contents in the two 8 bit **TEMPLATE** registers (**TMPLB**,**TMPLA**). The results are then filtered by the **MASK** registers (**MSKB**, **MSKA**) and ANDed together to generate the key signal. If the input is 8 or 15 bits wide, the unused bits are automatically masked out. Figure 4 shows the logic operation involved in Index Keying.

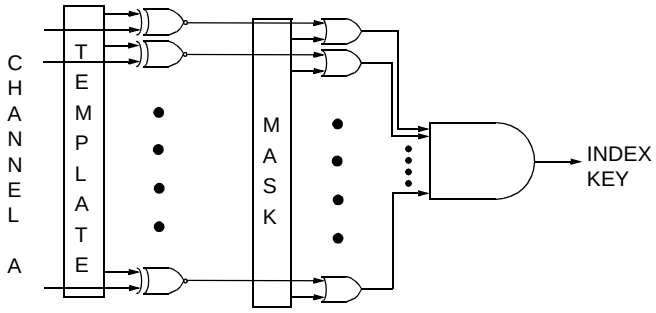


Figure 4. Index Keying Generation

2.2.2. Chroma Keying

If channel A's input is YCbCr format, Chroma Keying can be used for mixing. A rectangular area is specified in the Cb-Cr space (Figure 5). If Channel A's Cb/Cr values fall within this area, Channel B's video will be displayed. In this mode, **TMPLA** and **TMPLB** specify the lower and upper Cb, respectively, and **MSKA** and **MSKB** specify the lower and upper Cr, respectively, in the Cb-Cr space. Note that Cb and Cr are binary offset numbers with 128 corresponding to zero intensity, 0 and 255 corresponding to maximum intensity.

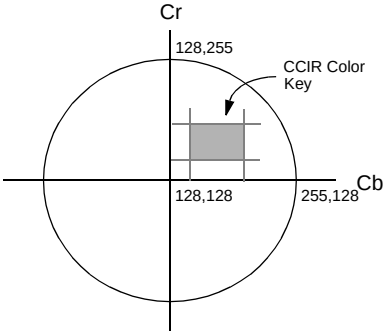


Figure 5. Cb-Cr Chroma Keying

2.2.3. Window Keying

A rectangular key window is specified in X-Y coordinates in the active display area. If window mixing is enabled and the **OUTSD** bit of the **Mixing Control** register is 0, Channel B is displayed inside the window, and Channel A is outside the window. The converse is true if the **OUTSD** bit is 1. If both the Chroma and Window Keyings are enabled, the **OUTSD** bit specifies where the Chroma Keying will be applied: 0 inside the window and 1 outside the window.

The 8 msb's of the four 10 bit coordinate registers, Window Horizontal Start Address, Window Horizontal End Address, Window Vertical Start Address and Window Vertical End Address, are stored in the **WHS**, **WHE**, **WVS** and **WVE** registers, respectively, while the 2 lsb bits are stored in the **WHV** register. The four msb registers are double clocked, and synchronized to the **WVE** write. A write to the **WVE** register will transfer the four msb registers' contents, concatenated with their corresponding lsb's, to the respective final address registers. Modifying the msb

register without writing to the **WVE** register will have no effect on the final address register. For multiplexed YCbCr video inputs, it is recommended that the horizontal window boundaries equal integer multiples of the block size.

2.2.4. Alpha Keying

If Channel A's input is only 15 bits (format 4, RGB 5:5:5), bit 15 of the input can be used as a mixing key.

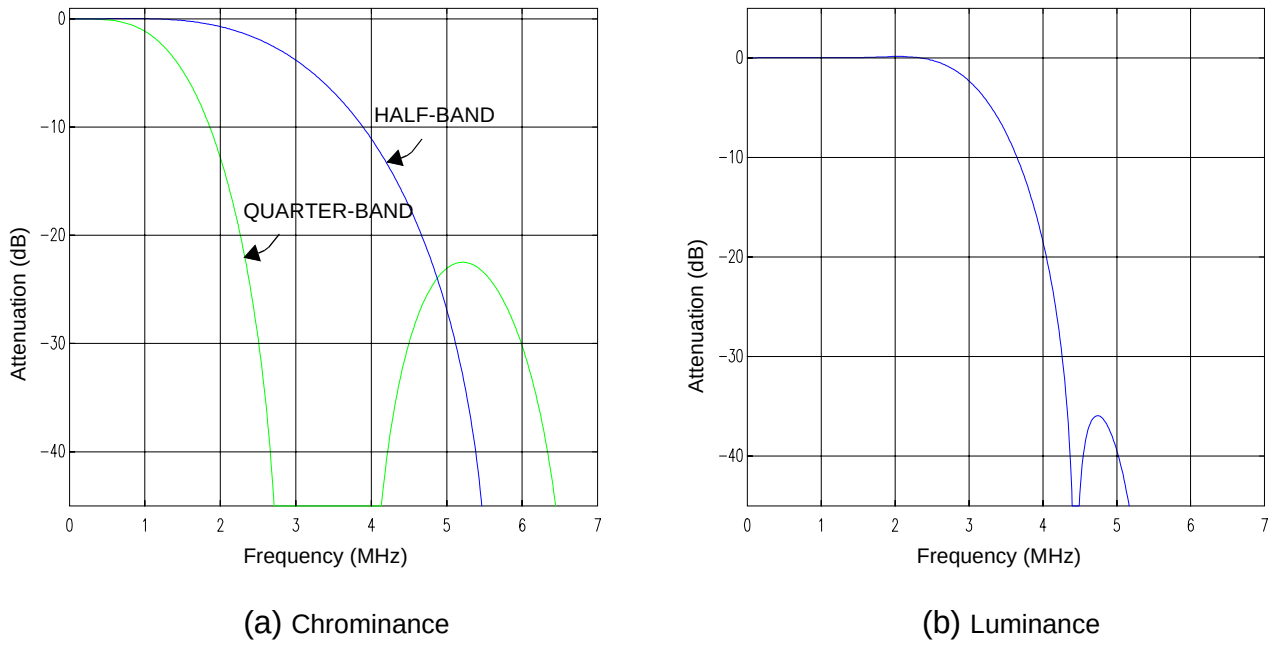
2.2.5. External Key

Pin DKY/R can be used as a mixing key if the **DKF** bit of the **Command** register (**CMD**) configures this pin as an external key input.

3. SIGNAL PROCESSING

3.1. Y/C Interpolation Filters

The incoming YCbCr signals are processed by the Interpolation Unit to increase the data rates to 13.5 MHz. (4:4:4 format). The multiplexed chroma signals are up sampled first, and then pass through either a 6th-order half-band or an 8th-order quarter-band filter. The reconstruction filters have flat 0 to 0.6 MHz frequency response as shown in Figure 6-(a). The received half-sampled luminance component (MPEG decoder output, 360 samples/line), which has a bandwidth less than 3 MHz, after being up sampled, will pass through a 14th-order smooth filter whose frequency response characteristic is shown in Figure 6-(b). These filters ensure the preservation of base band signals as well as the elimination of attendant high frequency aliasing components due to up sampling.



(a) Chrominance (b) Luminance

Figure 6. Interpolation Filter Characteristics

3.2. Band-limit Filter

The NTSC Encoder Unit consists of a 4 MHz luminance low pass filter and two equal bandwidth 1.2 MHz chrominance low pass filters. The functions of these filters are to limit the frequency contents of the computer generated image, to reduce the cross-luminance/chrominance distortion due to the mixing processes, and to enhance the resolutions.The digital filters are designed to have faster roll-off than the analog counterparts so that the quantization noise, which is monotonic decreasing along the frequency axis, are removed as soon as they pass the band of interest. Figure 7 shows the overall filter characteristics (interpolation cascaded with band-limit) for X:1:1 and X:2:2 formatted data. Also shown in Figure 8 are the luminance band-limit characteristics with and without the chroma filter.

At the filters' outputs, each pixel is represented by 3 10-bit numbers, which are maintained until the DAC inputs. Hence the block effects due to the limited quantization levels are reduced.

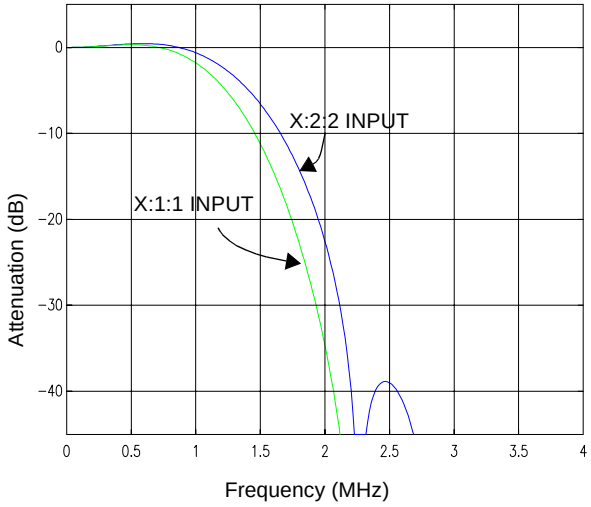


Figure 7. Chrominance Filter Characteristics

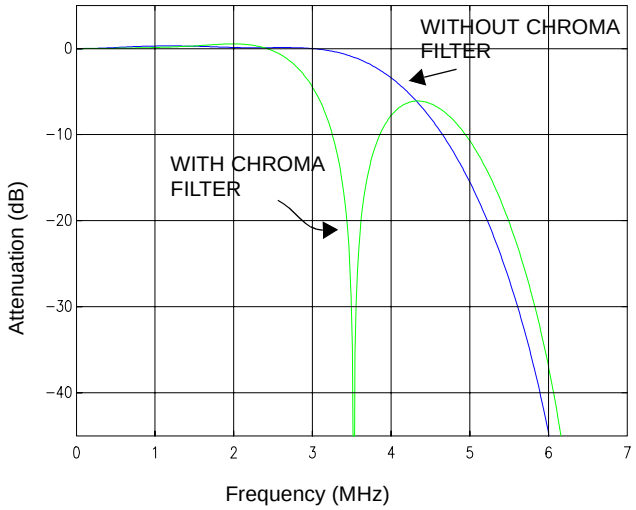


Figure 8. Luminance Band-limit Filter Characteristics

3.3. SINC (*Sin*x/x) Function Effect

The digital-to-analog converter exhibits a high frequency roll-off SINC filter characteristic owing to the zeroth order sample and hold process. The roll-off is a function of the DAC's conversion rate. The NTSC Encoder Unit also incorporates a 6th-order interpolation filter to raise the data rate to 27 MHz. The roll-off at 4 MHz is reduced from -1 dB (sampled at 13.5 MHz) to -0.2 dB. The up sampling also pushes the high frequency "image" beyond 23 MHz, greatly reducing the analog reconstruction filter requirement at the DAC's outputs.

4. SIGNAL MANIPULATION FUNCTIONS

The NTSC Encoder Unit provides the facilities for the user to control the contrast, hue, color killer and the vertical blanking period by programming the **Command Register B** (**CMDB**) and **Hue Control** register(**HUE**).

4.1. Hue Control

The chromaticity can be changed by modifying the modulation angle. The entire 360° hue range is divided into 264 equal units. To move the hue angle by k units the congruent 83*k MOD 264 should be loaded into the **HUE** register and bit 7 of **CMDB** register. The **HUE** register will not be transferred to the final **Hue Control** register until a write to the **CMDB** register occurs. Therefore, when changing the hue angle, the **HUE** register must be loaded first followed by a write to the **CMDB** register. The following examples show the value to be programmed into the HUE register for +5 and -5 degree hue angle:

Examples:

+5 degree Hue angle

$$k = \left\lfloor \frac{5}{360} \times 264 \right\rfloor = 3$$

$$HUE = mod(k \cdot 83, 264) = mod(249, 264) = 249$$

-5 degree Hue angle

$$k = \left\lfloor \frac{355}{360} \times 264 \right\rfloor = 260$$

$$HUE = mod(260 \cdot 83, 264) = mod(264 \cdot 81 + 196, 264) = 196$$

4.2. Chroma Trap Filter

The luminance path includes a Chroma Trap filter. When this filter is enabled (**CMDB**[4] = 1), the effective bandwidth is reduced to 2.8 MHz, resulting in a softer picture.

4.3. Color Killer

When bit 3 of the **CMDB** register is set to 1, the chroma data will be removed and the picture will be displayed as black and white.

4.4. Vertical Blanking

Normally, line 1 to line 9 in field 1 and the second half of line 263 to 272 in field 2 are blanked automatically. However, if bit 2 of **CMDB** register is 1, the blanking period is extended to the line specified in the **VBLK** register.

5. VIDEO OPERATIONAL TIMING

The KS0119 can operate in either slave or master mode. In slave mode, the chip uses two external input signals, active video (AV) and vertical blank (VBLK), to synchronize the internal operation. In master mode, however, the chip outputs these two signals. The chip generates two additional signals: Memory Transfer Request (MRQST) and field two indicator ($\overline{F2}$), which can be used to simplify the interface to an external frame buffer controller. Figure 9 shows the timing waveform for the NTSC output mode.

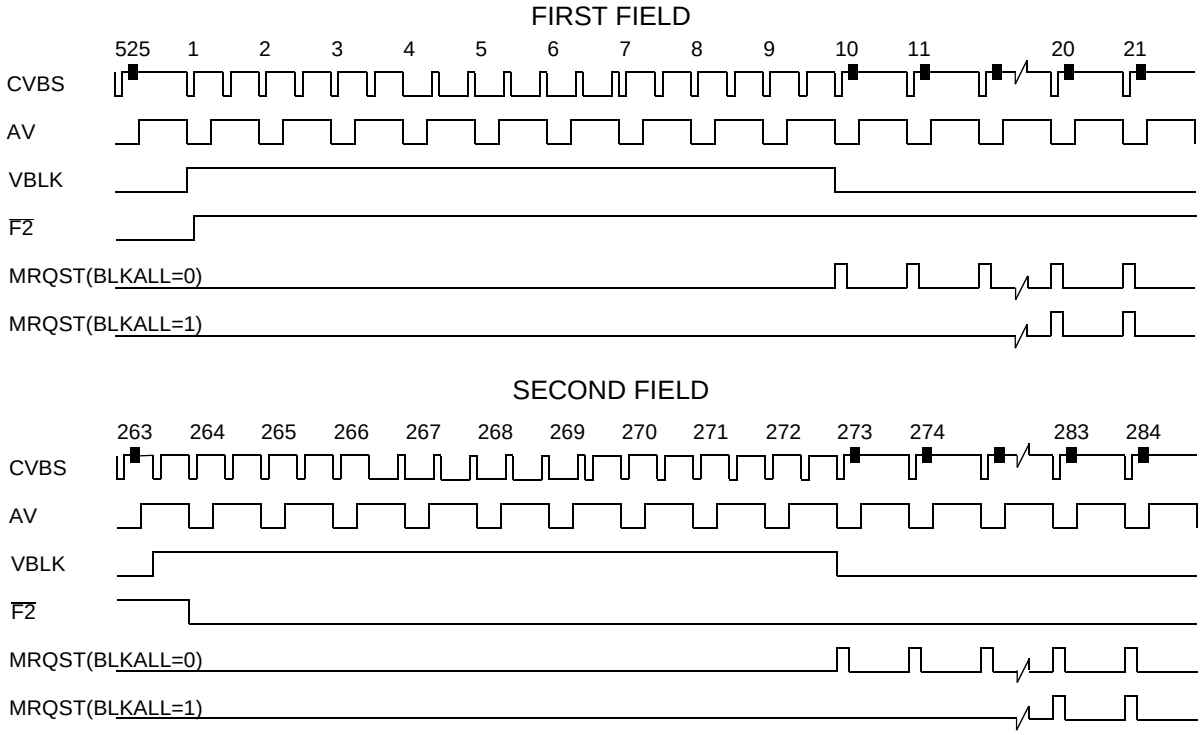


Figure 9. NTSC Output Timing

In Master mode, the timing shown in Figure 10 is maintained among AV, VBLK, and $\overline{F2}$, where n is the leading pixel number (see Figure 12 for more detail). In Slave mode, the two inputs AV and VBLK must meet the timing requirement as shown in Figure 11 in order for the Encoder to obtain the correct field information.

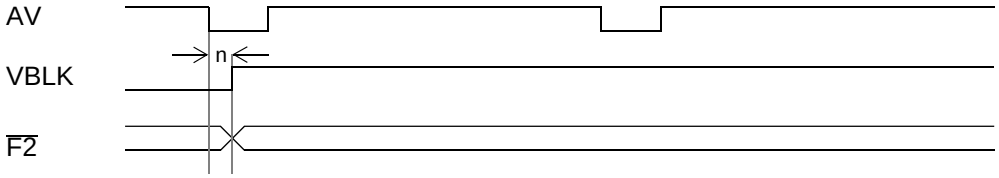


Figure 10. Master Mode AV, VBLK, and F2 Timing

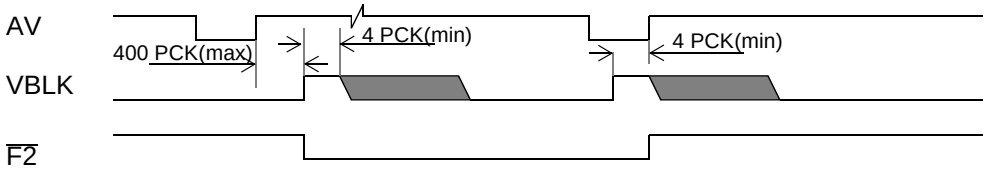


Figure 11. Slave Mode AV and VBLK Timing Requirement

5.1. Horizontal Timing

Each scan line contains hn pixels as shown in Figure 12. Of the hn pixels, only (hn - hblk) pixels are displayed. The AV signal is used to indicate the active portion of the horizontal scan line. The Horizontal Blank portion actually consists of three parts: Horizontal Front Porch, Horizontal Sync, and Horizontal Back Porch. The KS0119 outputs the Horizontal Sync signal to the display monitor.

In Master mode, the NTSC Encoder generates the AV signal. AV can be used by the external frame buffer to control the pixel read out. Because of the memory access latency associated with the external memory subsystem, AV should lead the pixel data by n pixel clocks. This is done by controlling the hav parameter. All horizontal timing parameters are programmable and Table 5 contains the information on how to calculate the line timing control register values for both NTSC and RGB displays.

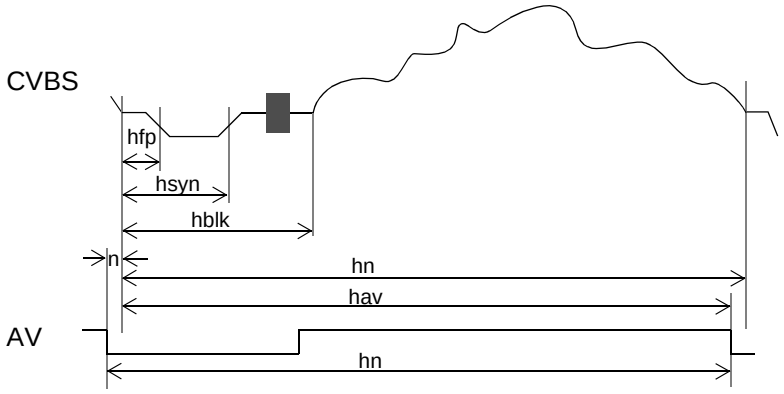


Figure 12. Horizontal Timing

Table 5: Line Timing Register Values

Register	Parameter	NTSC Value	RGB Value
HFP	Horizontal Front Porch	11	Thfp + 1
HSYN	Horizontal Sync Tip	184*	Thsyn + 1
HBLK	Horizontal Blanking	135	Thblk - 3
HN	Number of Pixels per Line	856	Thn - 2
HAV	End of Active Video	854 - n	Thn - 4 - n

*: This number is not used to control the Horizontal Sync Tip in NTSC mode.

5.2. Vertical Timing

Each field contains the active line and vertical blank portions. The vertical blank portion is further divided into Vertical Front Porch, Verical Sync, and Vertical Back Porch.There are four parameters that control the vertical timing: VFP, VSYN, VBLK, and VN. They are specified in terms of lines. Figure 13 shows the timing related to the four parameters. For NTSC output, these parameters are fixed and the power on default values should be used. However, if the **BLKALL** bit in the **Command Register** is set to 1, the **VBLK** value will be used instead. Table 6 provides information on how to program these parameters.

In Master mode, the NTSC Encoder outputs the VBLK signal. This signal can be used to synchronize the external frame buffer controller's line counter. In Slave mode, VBLK is an input and is used to synchronize the chip's internal operation.

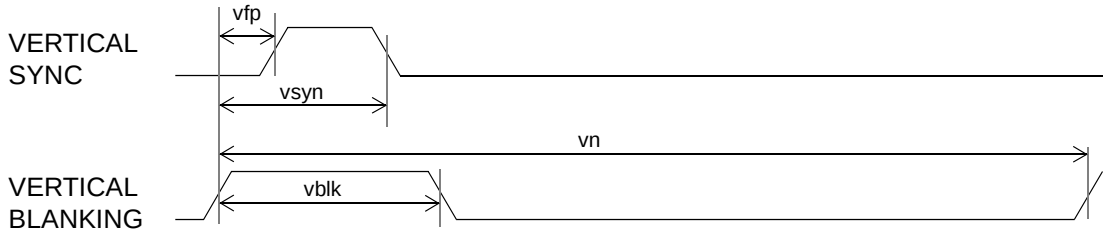


Figure 13. Vertical Timing

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Table 6: Frame Timing Register Value

Register	Parameter	Value
VFP	Vertical Front Porch	Tvfp - 1.
VSYN	Vertical Sync Tip	Tvsyn - 1.
VBLK	Vertical Blanking	Tvblk - 1.
VN	Number of Lines per Frame	Tvn - 1.

5.3. MRQST/MODE and $\overline{F2}$

MRQST/MODE is output during AV low for the active lines. This signal can be used to transfer video data from DRAM to shift registers in the VRAM. $\overline{F2}$ can be used by the external frame buffer controller for interlaced display.

6. COLOR PALETTE RAM, OVERLAY LOOKUP TABLE, AND PIXEL MASK REGISTER

The KS0119 contains a Color Palette RAM, an Overlay Lookup Table, and a Pixel Mask Register. They can be accessed through the host interface.

6.1. Accessing the Color Palette RAM

The Color Palette RAM is organized as 3 256x8 arrays. From the programmer's point of view, there are 256 entries; each entry has 3 bytes. To write to the Color Palette RAM, the entry offset is written to the Color Palette Write Index register, then three bytes, in the order of R, G, and B, are written to the Color Palette Data register. If consecutive entries are to be written, only the first offset address needs to be written to the Color Palette Write Index register. It is important to note that writing to the Color Palette Data register should always consist of multiples of three bytes. Unpredictable result will occur if this is not strictly followed.

Reading the Color Palette RAM is similar to writing the Color Palette RAM except the entry offset is written to the Color Palette Read Index register.

The Color Palette RAM is located at the center of the RGB path. There is no bypass path. Consequently, for 24-bit true color inputs even though the translations are not required the Color Palette RAM still needs to be loaded.

6.2. 6-Bit Color Palette Mode

The KS0119 also supports 6-bit color palette mode. When this mode is selected by setting **Command Register** bit 3 to 0, only the 6 LSB's for each color entry are loaded into the corresponding color palette register. Internally, the 6 LSB's are shifted to the MSB positions with the 2 LSB's padded with 0's. When reading from the palette RAM, the two MSB's must be ignored.

6.3. High Color and Pseudo Color Input Lookup Address.

The high color and pseudo color inputs pass through a formatter, which expands the inputs to a full 24 bits according to Table 7. For inputs with R, G, and B components less than 8 bits, the LSB's are padded with 0's. The outputs of the formatter, after passing through the pixel mask filter, become the color palette table addresses.

Table 7: RGB Input Formatter Conversion Table

Mode	Video Input <msb..lsb>	Color Lookup Table Input <msb..lsb>		
		Byte 2	Byte 1	Byte 0
1	R<7:0>:G<7:0>:B<7:0>	R<7:0>	G<7:0>	B<7:0>
2	R<4:0>:G<5:0>:B<4:0>	R<4:0>000	G<5:0>00	B<4:0>000
3	R<5:0>:G<5:0>:B<3:0>	R<5:0>00	G<5:0>00	B<3:0>0000
4	R<4:0>:G<4:0>:B<4:0>	R<4:0>000	G<4:0>000	B<4:0>000
5 and 6	P<7:0>	P<7:0>	P<7:0>	P<7:0>

6.4. Overlay Lookup Table

Four overlay input bits address the Overlay Lookup Table. If the overlay input is non-zero, overlay data will be displayed. The Overlay Look Up Table contains 15 entries, and each entry has three bytes, in the order of R, G, and B. The entry offset starts from 1 instead of 0. The access method for the Overlay Lookup Table is the same as that for the Color Palette RAM.

6.5. Pixel Mask Register

The Pixel Mask Register is used to filter the pixel data coming out from the RGB Input Formatter. Each R, G, B pixel byte is bit-wise ANDed with the pixel mask register. Special effects can be created by selectively masking out certain bits. This register needs to be initialized after power up.

7. DAC AND EXTERNAL RECONSTRUCTION FILTER

The three DACs on the chip are identical; they are video grade 10 bit current DACs. Figure 14 shows a typical configuration for the DAC portion of the chip. R_{REF} is connected to IREF to adjust the DAC output full scale. The DAC output is designed to drive a doubly terminated 75 Ω load. A 105 Ω resistor connected to R_{REF} can be used to set the output voltage peak to the RS-170A standard of 1 V. The built-in voltage reference has a large variation due to manufacturing technology limitations. For precise control of the DAC, an external voltage reference can be used. A variable resistor may also be used for R_{REF} to adjust the full scale DAC output current. The recommended analog filter circuit and its characteristic are shown in Figure 15 and Figure 16, respectively.

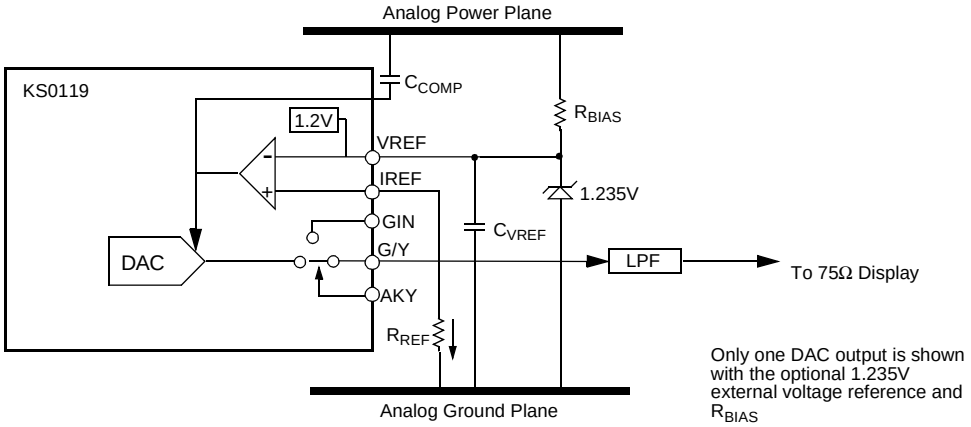


Figure 14. DAC Reference Circuit and Termination

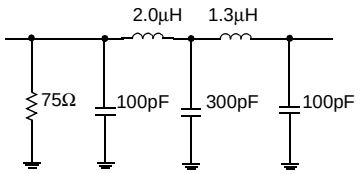


Figure 15. DAC Output Analog Reconstruction Filter

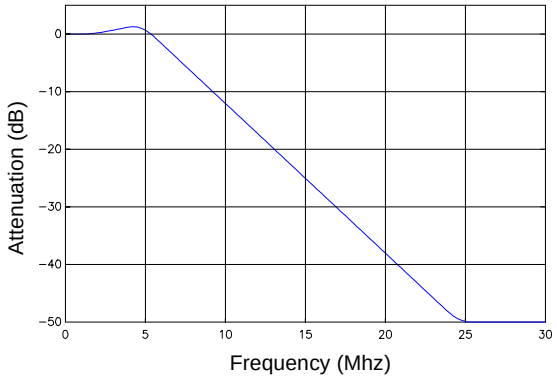


Figure 16. DAC Output Analog Reconstruction Filter Response

8. HOST INTERFACE

The KS0119 contains a conventional parallel microprocessor interface and a proprietary serial interface. The parallel microprocessor interface consists of 11 pins, some of which are shared by the three pin serial bus. The logic sense of the P/$\overline{S}$ control pin defines the host interface mode, parallel or serial. Three of the interface pins serve a dual purpose depending upon the mode selected. The $\overline{CS}$, R/$\overline{W}$, and D7 pins in parallel mode become SFRS, SCLK, and SDAT pins in serial mode, respectively.

8.1. Microprocessor Address Map

The KS0119 contains three groups of registers. The first group is the control registers. The control registers are used for feature/option selection. The second group is the color palette RAM. The third group is the overlay color look up table. Table 8 shows the microprocessor address map for the KS0119.

Table 8: Microprocessor Address Map

Address (Hex)	Description
00	Color Palette Write Index
01	Color Palette Data
02	Pixel Mask Register
03	Color Palette Read Index
04	Overlay CLUT Write Index
05	Overlay CLUT Data
06	Reserved
07	Overlay CLUT Read Index
08	Control Register Index
09	Control Register Data

8.2. Transfer Mode

Both the read and write cycles require that the index be written to the KS0119 first. The index is written to location ADDR = 08. The index is the internal address location for each register. The internal address is indicated by the register number associated with each register. Once the index is written, the selected register can have data read from or written to location ADDR = 09. Non-sequential internal registers are accessed individually by writing an index and then reading or writing one byte of data. Sequential locations can be accessed by writing the index for the first register and then reading or writing multiple bytes of data. The index auto-increments internally by one for each successive byte of data accessed while ADDE = 09. This mode is useful when initializing the device or when accessing word wide or blocks of registers.

The color palette and overlay CLUT operate in a similar fashion, except that separate index locations exist for read and write operations. The color palette write index is written to ADDR=00, and palette data is written to ADDR=01. For read operation, the index is written to ADDR=03. The color palette and overlay exhibit the same auto-increment capability as the control registers. This simplifies loading the color palette.

8.3. Serial Host Interface

The serial interface is selected by connecting the P/$\overline{S}$ pin to ground. This interface uses three signals: SFRS, SDAT,

and SCLK. The SFRS indicates a valid data transfer. Serial data is carried through the SDAT and clocked in or out with the SCLK. The data protocol sends each byte as msb first.

8.3.1. Serial Host Write/Read to KS0119

Each data transfer cycle is called a frame. A valid frame is indicated by a HIGH on the SFRS signal. A frame consists at least three bytes: the first byte contains a 7-bit slave device ID and a R/W bit (bit assignment shown in Figure 17); the second byte indicates the internal address of register the data transfer is intended for (see Table 8); and the third and consequent byte(s) are the data to be transferred to/from the register. If the data transfer is to/from the index register, three bytes are needed each frame. Since the KS0119 features an auto index increment function, consecutive data transfer to/from the data registers can be completed within the same frame.

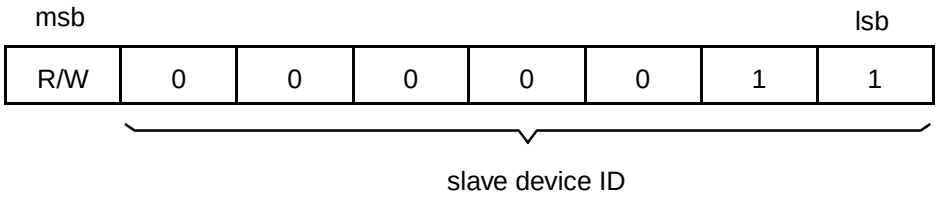


Figure 17. KS0119 Device ID and R/W

Figure 18 shows an example of a write to the index register. Each bit is latched into the device by the rising edge of the SCLK. A write to the data register is similar to a write to the index register except the second byte is 01h and the third and so on byte(s) are the data to be written (Figure 19). When the data is read from the device, the KS0119 outputs each bit is after the falling edge of the SCLK.

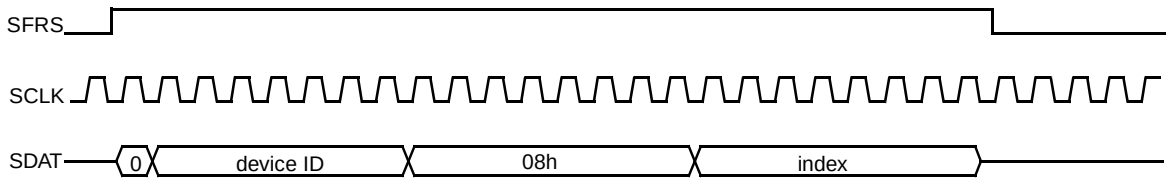


Figure 18. Serial Host Write to Index Register

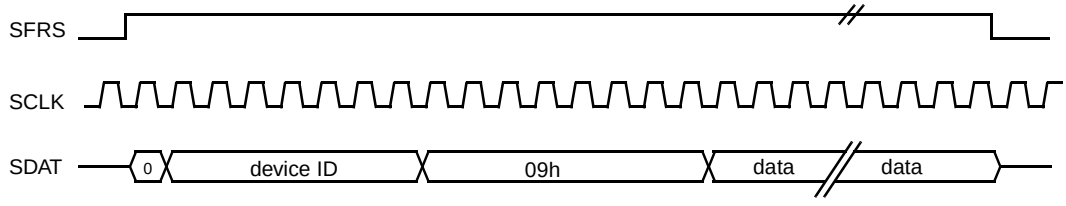


Figure 19. Serial Host Write to Data Register

8.4. Parallel Host Interface

Figure 20 shows the timing relation for a parallel read cycle. Figure 21 shows the timing for a parallel write cycle. The address ADDR and read/write R/$\overline{W}$ are stable before the $\overline{CS}$ signal is lowered. Data written to the KS0119 must be stable before $\overline{CS}$ goes high. Data is read from the KS0119 when $\overline{CS}$ is low.

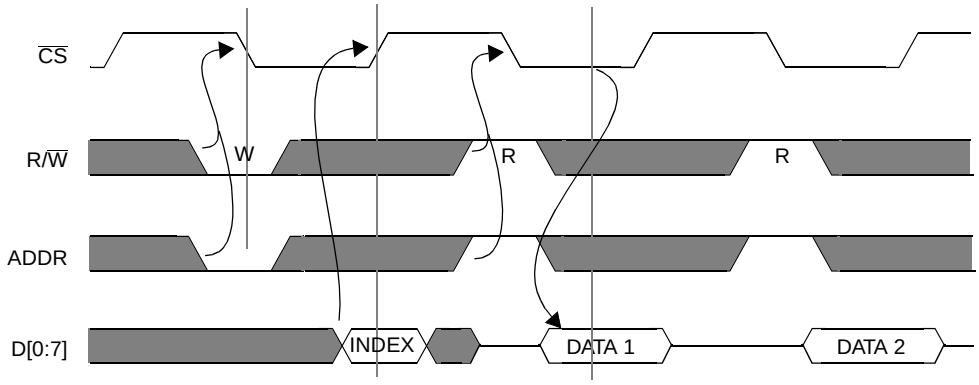


Figure 20. Parallel Host Interface Read Cycle

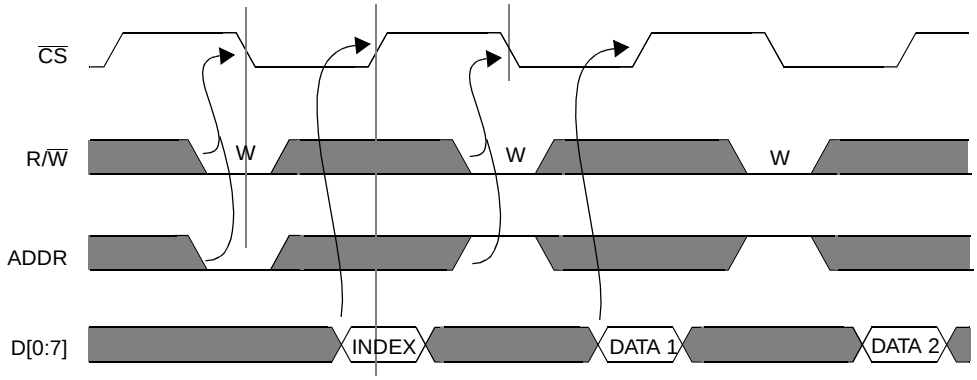


Figure 21. Parallel Host Interface Write Cycle

9. DETAILED CONTROL REGISTER DESCRIPTION

This section contains the detailed description of the control registers. The control registers can be categorized into three functional groups: indexes 60h to 63h are general control registers; indexes 64h to 6Dh are mixing control registers; indexes 70h to 79h are CRT control registers. Table 9 is a register summary, followed by the individual register description. Default values are noted with an asterisk (*) after the value description.

Table 9: Control Registers

Index	Mnemonic	Default	Description
60h	CMD	12h/A2h	Command Register
61h	FMT	90h/60h	Input Format
62h	CMDB	02h	Second Command Register
63h	HUE	00h	Chroma Phase Offset Bits 7..0
64h	MXCTR	00h	Mixing Control
65h	WHS	00h	Window Row Start Address
66h	WHE	00h	Window Row End Address
67h	WVS	00h	Window Column Start Address
68h	WVE	00h	Window Column End Address
69h	WHV	00h	Window Overflow Address(lsbs)
6Ah	TMPLA	00h	Chroma Key TMPLATE Byte 0
6Bh	TMPLB	00h	Chroma Key TMPLATE Byte 1
6Ch	MSKA	00h	Chroma Key MASK Byte 0
6Dh	MSKB	00h	Chroma Key MASK Byte 1
70h	HAVN	33h/B3h	HN and HAV Overflow Bits
71h	HAV	54h	Master Mode's AVout Lead Control
72h	HN	58h	Number of Pixels per Line
73h	HFP	0Bh	Horizontal Front Porch
74h	HSYN	B8h	End of Horizontal Sync
75h	HBLK	87h	End of Horizontal Blanking
76h	VN	00h	Number of Lines per Field
77h	VFP	83h	Vertical Front Porch
78h	VSYN	06h	End of Vertical Sync
79h	VBLK	14h	End of Vertical Blanking

Note: Some registers have two default values. The first number is for **MRQST/MOED** pin pulled low. The second number is for **MRQST/MODE** pin pulled high.

Command Register									
Index	**Mnemonic**	**bit 7**	**bit 6**	**bit 5**	**bit 4**	**bit 3**	**bit 2**	**bit 1**	**bit 0**
60h	**CMD**	RUN	MSTR	RGB	CKSL	8/6*	DKF	CVBS	YC

RUN — Software RUN control. The internal state machine is controlled by the logically ORed software and hardware RUN inputs.

1 Software run enable.

0 Software run disable.

The logic state of the MRQST/MODE is latched into this bit during power-on.

MSTR — Timing generation Master/Slave mode select.

1 Master.

0 Slave.*

RGB — Analog output format select.

1 RGB.

0 Composite and Super video.

The logic state of the MRQST/MODE is latched into this bit during power-on.

CKSL — Clock input and output control.

1 CK27 is selected, and pixel clock CKP's rate is f(CK27) / 2.

0 CKV is selected as the source, and CKP has the same rate as the clock input.

The inverted logic state of the MRQST/MODE is latched into this bit during power-on.

8/6* — 8/6 bit palette select.

1 8 bit palette.

0 6 bit palette.*

DKF — DKY/R pin configuration control.

1 DKY/R is input key for digital mixing.

0 DKY/R is hardware RUN input.*

CVBS — If bit 5 of this register is 0 this bit controls R/CVBS DAC.

1 R/CVBS DAC is on.*

0 R/CVBS DAC is in the power down state.

YC — If bit 5 of this register is 0 this bit controls G/Y and B/C DACs.

1 G/Y and B/C DACs are on.

0 G/Y and B/C DACs are in power down state.*

Input Format Register									
Index	**Mnemonic**	**bit 7**	**bit 6**	**bit 5**	**bit 4**	**bit 3**	**bit 2**	**bit 1**	**bit 0**
61h	**FMT**	FMTA3	FMTA2	FMTA1	FMTA0	FMTB3	FMTB2	FMTB1	FMTB0

FMTA Channel A input format. See Table 3 for supported format on Channel A.
The power-on default is 6 if there is an external pull-up resistor on the MRQST/MODE pin, or 9 otherwise.

FMTB Channel B input format. See Table 4 for supported format on Channel B.

Command Register B									
Index	**Mnemonic**	**bit 7**	**bit 6**	**bit 5**	**bit 4**	**bit 3**	**bit 2**	**bit 1**	**bit 0**
62h	**CMDB**	HUE8	VSP	HSP	CTRAP	MONO	BLKALL	SLT1	SLT0

VSP Vertical sync input (VBLK) polarity control.
- 1 vertical sync input is active low.
- 0 vertical sync input is active high.*

HSP Horizontal sync input (AV) polarity control.
- 1 horizontal sync input is active high.
- 0 horizontal sync input is active low.*

CTRAP Chroma trap filter control. When enabled, the high frequency luminance signals near the color subcarrier are filtered out. This function is available for NTSC output only.
- 1 enables filtering.
- 0 disables filtering.*

MONO Color Killer control. When enabled, the chrominance signal is suppressed. This function is available for NTSC output only.
- 1 Color Killer enable.
- 0 Color Killer disable.*

BLKALL When set, the output from line 1 to the line set by the **VBLK** register is blanked.

SLT[1:0] These two bits control the assertion of the MRQST signal.
- 00 MRQST is asserted for the active lines whose line numbers are greater than or equal to the value contained in the **VBLK** register.
- 01 MRQST is always asserted.
- 10 MRQST is not asserted during the vertical blanking period.*
- 11 Reserved. Do not use.

Hue Control Register									
Index	**Mnemonic**	**bit 7**	**bit 6**	**bit 5**	**bit 4**	**bit 3**	**bit 2**	**bit 1**	**bit 0**
62h	**CMDB**	HUE8	VSP	HSP	CTRAP	MONO	BLKALL	SLT1	SLT0
63h	**HUE**	HUE7	HUE6	HUE5	HUE4	HUE3	HUE2	HUE1	HUE0

HUE[8:0] Hue control. To have a phase shift of k divisions, the 9 bit register should be loaded with the value <83*k> MOD 264. Each division is equal to 360/264 degrees. Hue can be adjusted only for NTSC output mode.

Mixing Control Register									
Index	**Mnemonic**	**bit 7**	**bit 6**	**bit 5**	**bit 4**	**bit 3**	**bit 2**	**bit 1**	**bit 0**
64h	**MXCTR**	MXEN	CMEN	AMEN	WMEN	OUTSD	K2	K1	K0

This register controls the digital mixing function. Please see the "**DIGITAL MIXING**" section for additional information.

MXEN Master mixing control.
- 1 mixing is allowed.
- 0 no mixing is allowed.*

CMEN Index or chroma mixing control.
- 1 Index or Chroma Mixing enable.
- 0 Index or Chroma Mixing disable.*

AMEN Alpha mixing control.
- 1 Alpha Mixing enable.
- 0 Alpha Mixing disable.*

WMEN Window mixing control.
- 1 Window Mixing enable.
- 0 Window Mixing disable.*

OUTSD Channel B inside/outside mixing window control.
- 1 Channel B is outside the Mixing Window.
- 0 Channel B is inside the Mixing Window.*

K[2:0] During linear blend mixing, these bits set the luminance attenuation factors for Channel A and Channel B. For Channel A, the attenuation factor is K/8, and for Channel B, the attenuation factor is 1-K/8, where K = K[2:0].

Window Horizontal Start Address									
Index	**Mnemonic**	**bit 7**	**bit 6**	**bit 5**	**bit 4**	**bit 3**	**bit 2**	**bit 1**	**bit 0**
65h	**WHS**	WHS9	WHS8	WHS7	WHS6	WHS5	WHS4	WHS3	WHS2
69h	**WHV**	WHS1	WHS0	WHE1	WHE0	WVS1	WVS0	WVE1	WVE0

WHS[9:0] This 10-bit register contains the horizontal pixel start location for the Mixing Window.

Window Horizontal End Address									
Index	**Mnemonic**	**bit 7**	**bit 6**	**bit 5**	**bit 4**	**bit 3**	**bit 2**	**bit 1**	**bit 0**
66h	**WHE**	WHE9	WHE8	WHE7	WHE6	WHE5	WHE4	WHE3	WHE2
69h	**WHV**	WHS1	WHS0	WHE1	WHE0	WVS1	WVS0	WVE1	WVE0

WHE[9:0] This 10-bit register contains the horizontal pixel end location for the Mixing Window.

Window Vertical Start Address									
Index	**Mnemonic**	**bit 7**	**bit 6**	**bit 5**	**bit 4**	**bit 3**	**bit 2**	**bit 1**	**bit 0**
67h	**WVS**	WVS9	WVS8	WVS7	WVS6	WVS5	WVS4	WVS3	WVS2
69h	**WHV**	WHS1	WHS0	WHE1	WHE0	WVS1	WVS0	WVE1	WVE0

WVS[9:0] This 10-bit register contains the vertical line start number for the Mixing Window.

Window Vertical End Address									
Index	**Mnemonic**	**bit 7**	**bit 6**	**bit 5**	**bit 4**	**bit 3**	**bit 2**	**bit 1**	**bit 0**
68h	**WVE**	WVE9	WVE8	WVE7	WVE6	WVE5	WVE4	WVE3	WVE2
69h	**WHV**	WHS1	WHS0	WHE1	WHE0	WVS1	WVS0	WVE1	WVE0

WVE[9:0] This 10-bit register contains the vertical line end number for the Mixing Window.

Chroma Key TEMPLATE Byte 0 (A)									
Index	**Mnemonic**	**bit 7**	**bit 6**	**bit 5**	**bit 4**	**bit 3**	**bit 2**	**bit 1**	**bit 0**
6Ah	**TMPLA**	TMPLA 7	TMPLA 6	TMPLA 5	TMPLA 4	TMPLA 3	TMPLA 2	TMPLA 1	TMPLA 0

TMPLA[7:0] For RGB Index Keying, this register is the lower byte of the **TEMPLATE** register. For CbCr Chroma Keying, this register contains the lower limit of the Cb key. See the section "**Digital Mixing**" for a more detailed description of this register.

Chroma Key TEMPLATE Byte 1 (B)									
Index	**Mnemonic**	**bit 7**	**bit 6**	**bit 5**	**bit 4**	**bit 3**	**bit 2**	**bit 1**	**bit 0**
6Bh	**TMPLB**	TMPLB 7	TMPLB 6	TMPLB 5	TMPLB 4	TMPLB 3	TMPLB 2	TMPLB 1	TMPLB 0

TMPLB[7:0] For RGB Index Keying, this register is the higher byte of the **TEMPLATE** register. For CbCr Chroma keying, this register contains the upper limit of the Cb key. See the section "**Digital Mixing**" for a more detailed description of this register.

Chroma Key MASK Byte 0 (A)									
Index	**Mnemonic**	**bit 7**	**bit 6**	**bit 5**	**bit 4**	**bit 3**	**bit 2**	**bit 1**	**bit 0**
6Ch	**MSKA**	MSKA7	MSKA6	MSKA5	MSKA4	MSKA3	MSKA2	MSKA1	MSKA0

MSKA[7:0] For RGB Index Keying, this is the lower byte of the **MASK** register. For CbCr Chroma Keying, this register contains the lower limit of the Cr key. See the section "**Digital Mixing**" for more detail.

Chroma Key MASK Byte 1 (B)									
Index	**Mnemonic**	**bit 7**	**bit 6**	**bit 5**	**bit 4**	**bit 3**	**bit 2**	**bit 1**	**bit 0**
6Dh	**MSKB**	MSKB7	MSKB6	MSKB5	MSKB4	MSKB3	MSKB2	MSKB1	MSKB0

MSKB[7:0] For RGB index keying, this is the upper byte of the **MASK** register. For CbCr keying, this register sets the upper limit of the Cr key. See the section "**Digital Mixing**" for more detail.

Master Mode's AVout Lead Control									
Index	**Mnemonic**	**bit 7**	**bit 6**	**bit 5**	**bit 4**	**bit 3**	**bit 2**	**bit 1**	**bit 0**
70h	**HAVN**	SYNCPT	HN10	HN9	HN8	0	HAV10	HAV9	HAV8
71h	**HAV**	HAV7	HAV6	HAV5	HAV4	HAV3	HAV2	HAV1	HAV0

SYNCPT Sync pass through.

1 $\overline{\text{HSYN}}$ and $\overline{\text{VSYN}}$ are the delayed outputs of AV and VBLK, respectively.

0 $\overline{\text{HSYN}}$ and $\overline{\text{VSYN}}$ are internally generated.

The logic state of the MRQST/MODE is latched into this bit during power-on.

HAV[10:0] In Master Mode, this 11-bit register defines the AVout lead control timing. In Slave Mode, this register has no effect. See the section "**Horizontal Timing**" for detail.

Number of Pixels per Line									
Index	**Mnemonic**	**bit 7**	**bit 6**	**bit 5**	**bit 4**	**bit 3**	**bit 2**	**bit 1**	**bit 0**
70h	**HAVN**	SYNCPT	HN10	HN9	HN8	0	HAV10	HAV9	HAV8
72h	**HN**	HN7	HN6	HN5	HN4	HN3	HN2	HN1	HN0

HN[10:0] This 11-bit register controls the total number of pixels per line, which is equal to HN[10:0]+2.

Horizontal Front Porch									
Index	**Mnemonic**	**bit 7**	**bit 6**	**bit 5**	**bit 4**	**bit 3**	**bit 2**	**bit 1**	**bit 0**
73h	**HFP**	HFP7	HFP6	HFP5	HFPB4	HFP3	HFP2	HFP1	HFP0

HFP[7:0] This register controls the horizontal front porch timing in number of pixels, which is equal to HFP[7:0]-1.

Horizontal Sync End									
Index	**Mnemonic**	**bit 7**	**bit 6**	**bit 5**	**bit 4**	**bit 3**	**bit 2**	**bit 1**	**bit 0**
74h	**HSYN**	HSYN7	HSYN6	HSYN5	HSYN4	HSYN3	HSYN2	HSYN1	HSYN0

HSYN[7:0] This register controls the horizontal sync end timing in number of pixels, which is equal to HSYN[7:0]-1.

Horizontal Blanking End									
Index	**Mnemonic**	**bit 7**	**bit 6**	**bit 5**	**bit 4**	**bit 3**	**bit 2**	**bit 1**	**bit 0**
75h	**HBLK**	HBLK7	HBLK6	HBLK5	HBLK4	HBLK3	HBLK2	HBLK1	HBLK0

HBLK[7:0] This register controls the horizontal blanking end timing in number of pixels, which is equal to HBLK[7:0]+3.

Number of Lines per Field									
Index	**Mnemonic**	**bit 7**	**bit 6**	**bit 5**	**bit 4**	**bit 3**	**bit 2**	**bit 1**	**bit 0**
76h	**VN**	VN7	VN6	VN5	VN4	VN3	VN2	VN1	VN0
77h	**VFP**	VN9	VN8	VFP5	VFP4	VFP3	VFP2	VFP1	VFP0

VN[9:0] This 10-bit register controls the total number of lines per field, which is equal to VN[9:0]+1.

Vertical Front Porch									
Index	**Mnemonic**	**bit 7**	**bit 6**	**bit 5**	**bit 4**	**bit 3**	**bit 2**	**bit 1**	**bit 0**
77h	**VFP**	VN9	VN8	VFP5	VFP4	VFP3	VFP2	VFP1	VFP0

VFP[5:0] This 6-bit register controls the vertical front porch in number of lines, which is equal to VFP[5:0]+1.

Vertical Sync End									
Index	**Mnemonic**	**bit 7**	**bit 6**	**bit 5**	**bit 4**	**bit 3**	**bit 2**	**bit 1**	**bit 0**
78h	**VSYN**	VSYN7	VSYN6	VSYN5	VSYN4	VSYN3	VSYN2	VSYN1	VSYN0

VSYN[7:0] This register controls the end of vertical sync in number of lines, which is equal to VSYN[7:0]+1.

Vertical Blanking End									
Index	**Mnemonic**	**bit 7**	**bit 6**	**bit 5**	**bit 4**	**bit 3**	**bit 2**	**bit 1**	**bit 0**
79h	**VBLK**	VBLK7	VBLK6	VBLK5	VBLK4	VBLK3	VBLK2	VBLK1	VBLK0

VBLK[7:0] This register has three functions:

1. It controls the vertical blank timing for VGA monitors, and for NTSC monitors if the **BLKALL** bit is set in the **Command** register.
2. It defines line zero of the active display.
3. In conjunction with slt[1:0] it controls for which lines the MRQST signal will be asserted for NTSC monitors.

ABSOLUTE MAXIMUM RATINGS

Characteristics	Symbol	Value	Unit
Supply voltage (measured to GND)	V_{DD}	-0.5 to +7.0	V
Digital input voltage	V_I	0.5 to (V_{DD}+0.5)	V
Ambient operating temperature range	Ta	-10 to +100	°C
Storage temperature range	Tstg	-60 to +150	°C
Junction temperature	Tj	150	°C
Soldering temperature (5 sec., 1/4” from pin)	Tsol	300	°C
Vapor phase soldering (1 min.)	Tvsol	220	°C

Notes: 1. Absolute maximum ratings are limiting values applied individually, while all other parameters are within specified operating conditions.
2. Functional operation under any of these conditions is not implied.
3. Applied voltage must be current limited to a specified range.

RECOMMENDED OPERATING CONDITIONS

Characteristics	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{DD}	4.75	5	5.25	V
Reference voltage Internal External	Vref		 1.235 1.235		V
Reference current	Iref		11.56		mA
Analog output load	R_L		37.5		Ω
Ambient operating temperature range	Ta	0		70	°C

DC ELECTRICAL CHARACTERISTICS

Characteristics	Symbol	Min	Typ	Max	Unit
Digital input high voltage	V_{IH}	2.0		V_{DD}+0.5	V
Digital input low voltage	V_{IL}	GND-0.5		0.8	V
Digital input high current(V_{IN}=2.4V)	I_{IH}			1	μA
Digital input low current(V_{IN}=0.4V)	I_{IL}			-1	μA
Digital input capacitance(f=1MHz,V_{IN}=2.4V)	C_{IN}			7	pF
Digital output high voltage(I_{OH}=-400μA)	V_{OH}	2.4			V
Digital output low voltage(I_{OL}=3.2mA)	V_{OL}			0.4	V
Digital three-state current	I_{OZ}			50	μA
Digital output capacitance	CD_{OUT}			7	pF
Supply current	I_{CC}		150		mA
Analog multiplexer ON resistance	RA_{ON}		10		Ω
Analog multiplexer OFF resistance	RA_{OFF}		10		kΩ

AC ELECTRICAL CHARACTERISTICS

Characteristics	Symbol	Min	Typ	Max	Unit
$\overline{CS}$ or SCLK low	t_{pwlC}	50			ns
$\overline{CS}$ or SCLK high	t_{pwhC}	4			CK27/CKV
R/$\overline{W}$ setup time	$t_{sR/\overline{W}}$	10			ns
R/$\overline{W}$ hold time	$t_{hR/\overline{W}}$	10			ns
A[0:3] setup time	t_{sA}	10			ns
A[0:3] hold time	t_{hA}	10			ns
$\overline{CS}$ or SCLK active to data valid	t_{validD}			40	ns
$\overline{CS}$ or SCLK inactive to data 3-state	$t_{3\text{-}stateD}$			20	ns
Data setup time	t_{sD}	10			ns
Data hold time	t_{hD}	10			ns
SFRS setup time	t_{sFRM}	10			ns
SFRS hold time	t_{hFRM}	10			ns
Setup time (P[0:31], DKY/R, AV, VBLK)	t_{sPIX}	-9			ns
Hold time (P[0:31], DKY/R, AV, VBLK)	t_{hPIX}	18.5			ns
CKP to output delay	t_{dPIX}			9	ns
Video pipeline delay (NTSC output)	t_{dNTSC}	53		54	CK27
Video pipeline delay (RGB output)	t_{dRGB}		23		CKV
CK27 clock rate	f_{CK27}	26.9999	27	27.0001	MHz
CKV clock rate	f_{CKV}			Note1	MHz
CK27, CKV to CKP delay	t_{dCKP}	7	9	12.5	ns

32 for KS0119, 45 for KS0119Q2.

Parallel Host Interface Timing

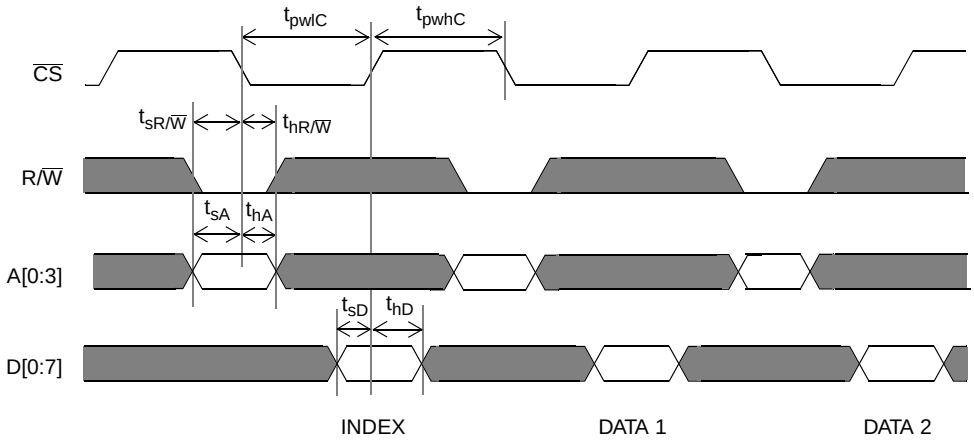


Figure 22. Parallel Host Interface Write Cycle

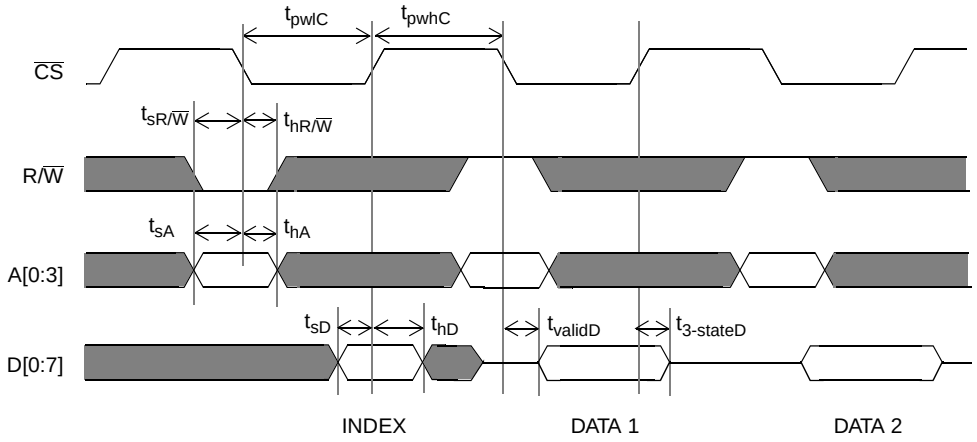


Figure 23. Parallel Host Interface Read Cycle

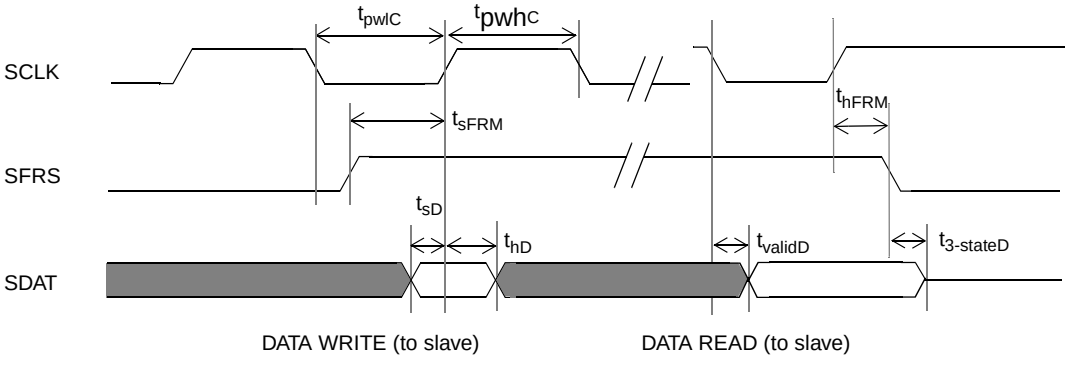


Figure 24. Serial Host Interface Detailed Timing

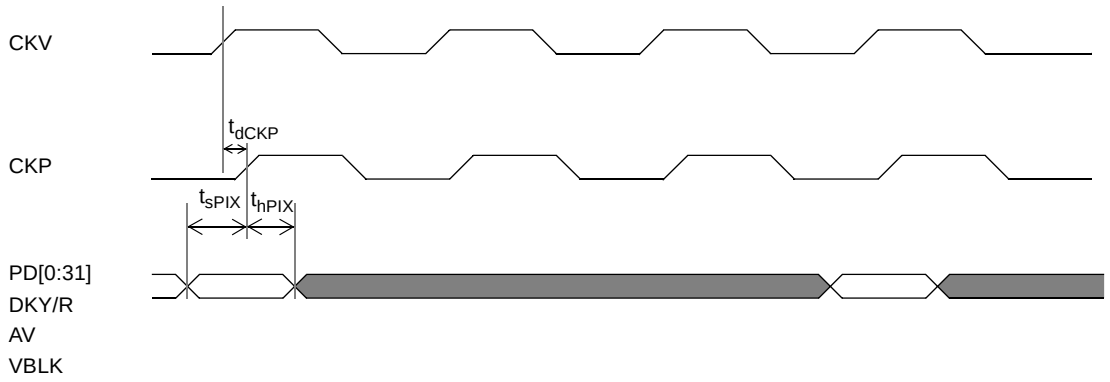


Figure 25. Pixel Data Setup and Hold Time

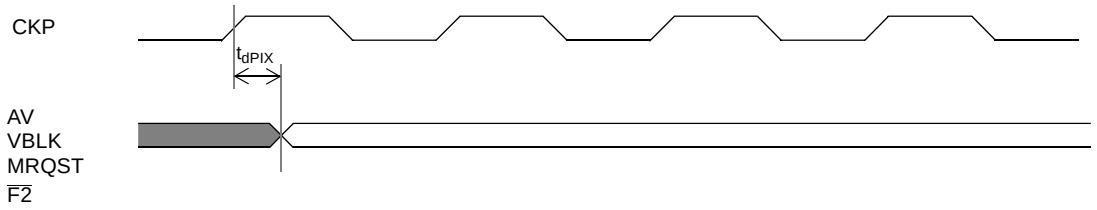


Figure 26. CKP to Output Delay

DAC DC CHARACTERISTICS

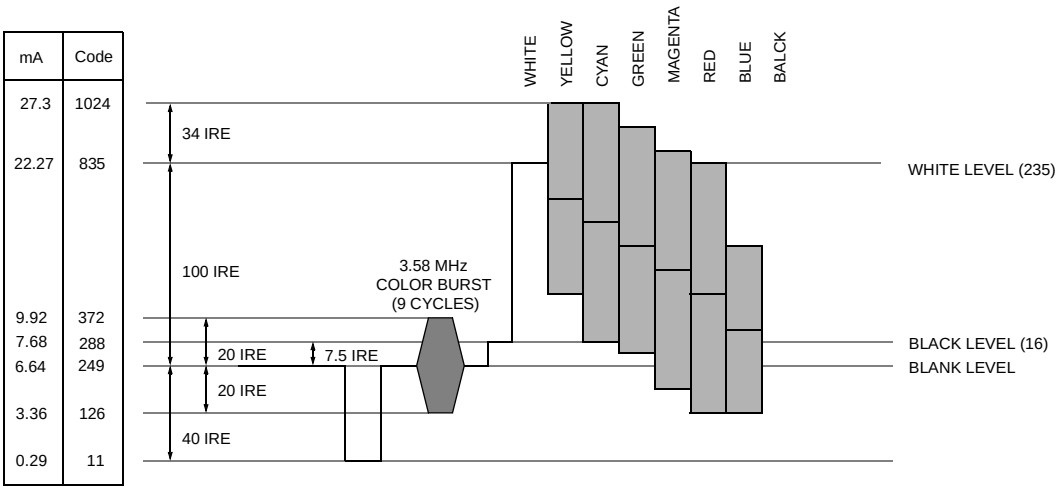
Characteristics	Symbol	Min	Typ	Max	Unit
Resolution					
RGB output			8		Bits
NTSC or Y/C output			10		Bits
Integral non-linearity error	IL			0.15%	
Differential non-linearity error	DL			0.1%	
Gray scale error			0	5%	
Monotonicity			Guaranteed		
Coding					Binary
Analog outputs (NTSC)					
Full scale current range		25.3	26.67	28	mA
Output current					
White level relative to black		16.74	17.62	18.5	mA
Black level relative to blank			1.44		mA
Blank level relative to sync			7.62		mA
LSB size			26.1		μA
DAC to DAC matching			2%	5%	
Output compliance	V_{OC}	-0.3		1.5	V
Output impedance	RA_{OUT}		10		kΩ
Output capacitance (f=1MHz, I_{OUT}=0mA)	CA_{OUT}		15	30	pF
Internal reference voltage	V_{ref}	1.17	1.235	1.296	V
Voltage reference input current	IV_{ref}		10		μA
DAC reference current	I_{REF}	11.14	11.56	12.34	mA
DAC reference resistor (V_{REF}=Typ)	R_{REF}		105		Ω
Power supply rejection ratio (C_{COMP}=0.1 μF, f=1 KHz)	PSRR			0.5	%/ΔV_{DD}

Test conditions: In NTSC operation, with DAC output = 1.0 V_{P-P}, V_{REF} = 1.235 V, R_{REF} = 105 Ω, 75 Ω load.

DAC AC CHARACTERISTICS

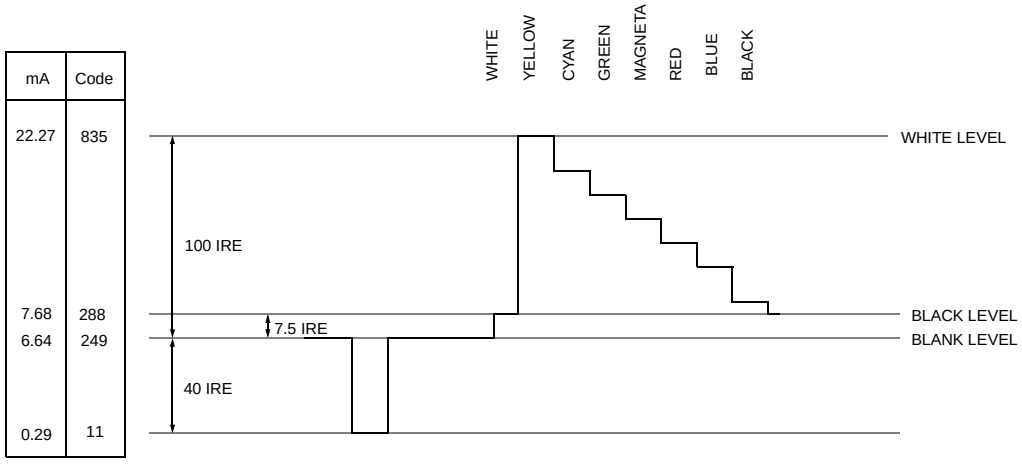
Characteristics	Symbol	Min	Typ	Max	Unit
Differential gain	DG		±0.5%	1.5%	
Differential phase	DP		±0.5	1	Degree
Signal to noise ratio	SNR	48	60		dB
Analog output delay	t_d			30	ns
Analog output rise/fall time	t_r/t_f		3		ns
Analog settling time	t_{set}		20		ns
Clock and data feedthrough	FDTHR		-30		dB
Glitch impulse	GI		75		pV-Sec
Analog output skew	t_{skw}		0	5	ns

NTSC DAC OUTPUT WAVEFORMS



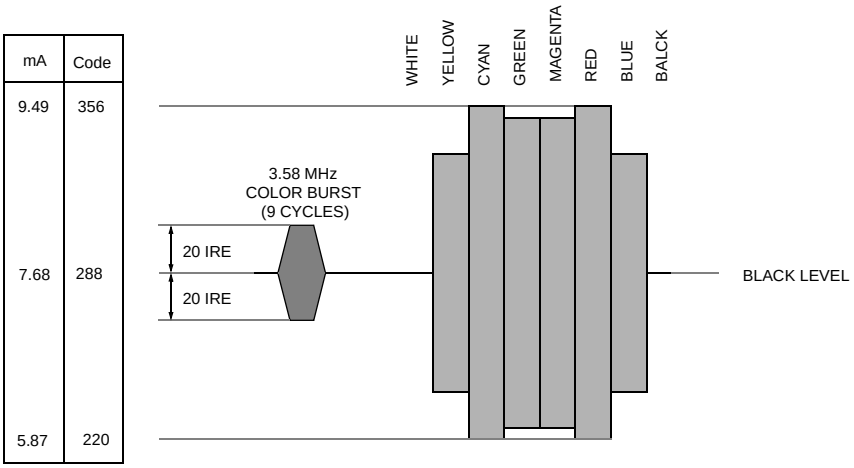
Note: 37.5 Ω load, VREF=1.235 V, and R_{REF}=105 Ω. RS-170A levels and tolerances are assumed.

Figure 27. Composite NTSC Video Output Waveform



Note: 37.5 Ω load, VREF=1.235 V, and R_{REF}=105 Ω. RS-170A levels and tolerances are assumed.

Figure 28. NTSC Y (Luminance) Video Output Waveform



Note: 37.5 Ω load, VREF=1.235 V, and R_{REF}=105 Ω. RS-170A levels and tolerances are assumed.

Figure 29. NTSC C (Chrominance) Video Output Waveform

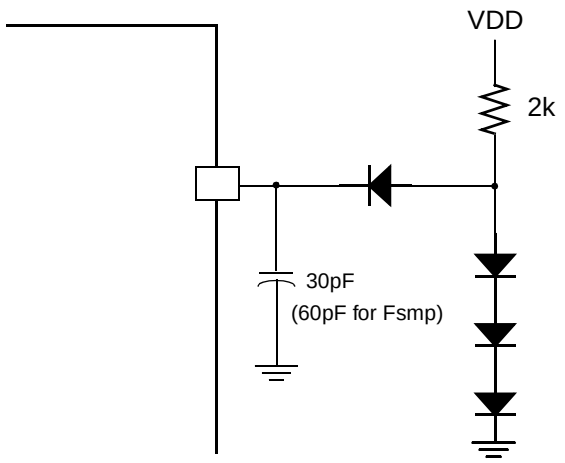


Figure 30. Load Circuit for Timing Measurements. Digital Outputs

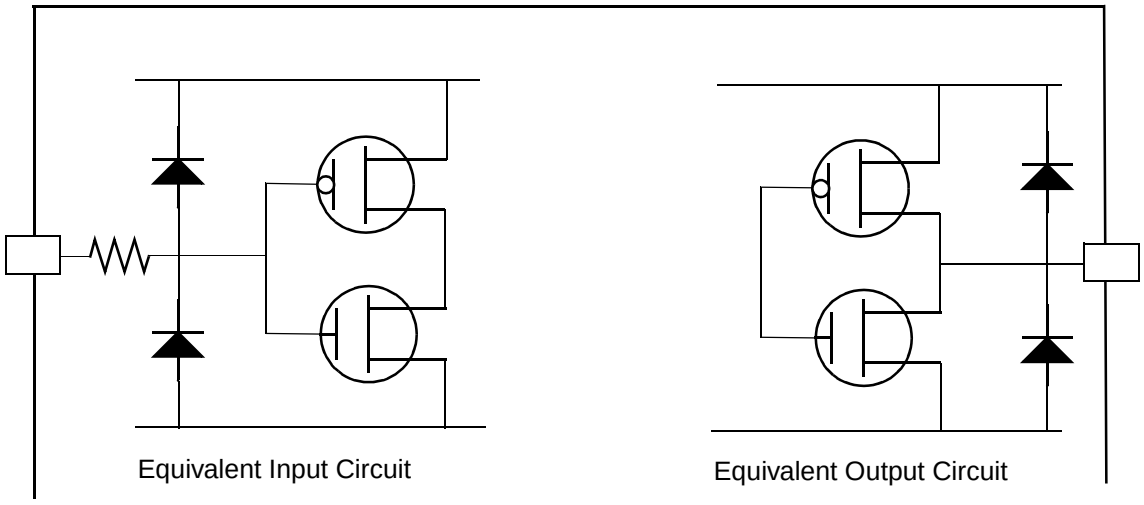
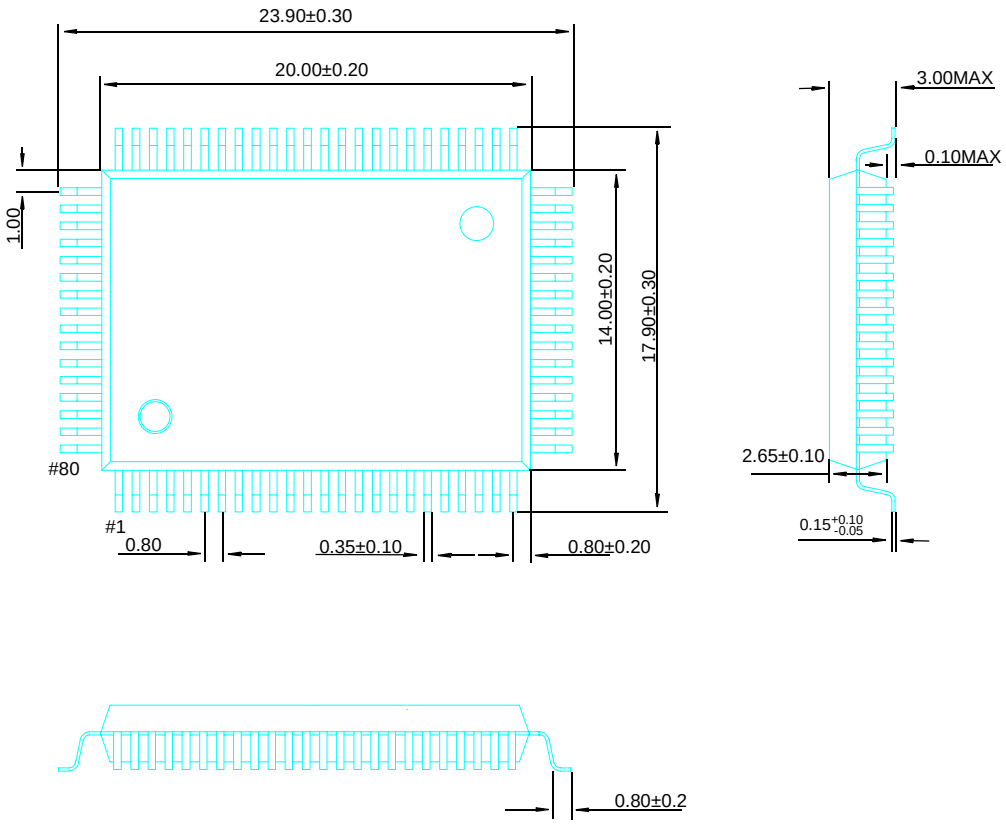


Figure 31. ESD Protection

PACKAGE DIMENSION (Dimensions are in Millimeters)

80-QFP-1420C



PACKAGE DIMENSION (Continued)

100-QPF-1420C