

DUAL 5V REGULATOR WITH RESET AND DISABLE FUNCTIONS

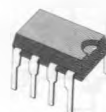
PRELIMINARY DATA

- OUTPUT CURRENTS: $I_{O1} = 50\text{mA}$
 $I_{O2} = 100\text{mA}$
- FIXED PRECISION OUTPUT VOLTAGE $5\text{V} \pm 2\%$
- RESET FUNCTION CONTROLLED BY INPUT VOLTAGE AND OUTPUT 1 VOLTAGE
- RESET FUNCTION EXTERNALLY PROGRAMMABLE TIMING
- RESET OUTPUT LEVEL RELATED TO OUTPUT 2
- OUTPUT 2 INTERNALLY SWITCHED WITH ACTIVE DISCHARGING
- OUTPUT 2 DISABLE LOGICAL INPUT
- LOW LEAKAGE CURRENT, LESS THAN $1\mu\text{A}$ AT OUTPUT 1
- INPUT OVERVOLTAGE PROTECTION UP TO 60V

- RESET OUTPUT NORMALLY LOW
- OUTPUT TRANSISTORS SOA PROTECTION
- SHORT CIRCUIT AND THERMAL OVERLOAD PROTECTION

The L4903 is a monolithic low drop dual 5V regulator designed mainly for supplying micro-processor systems.

Reset, data save functions and remote switch on/off control can be realized.



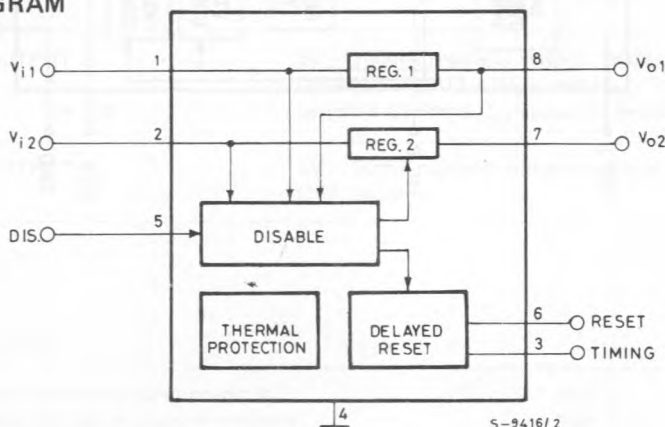
Minidip Plastic

ORDERING NUMBER: L4903

ABSOLUTE MAXIMUM RATINGS

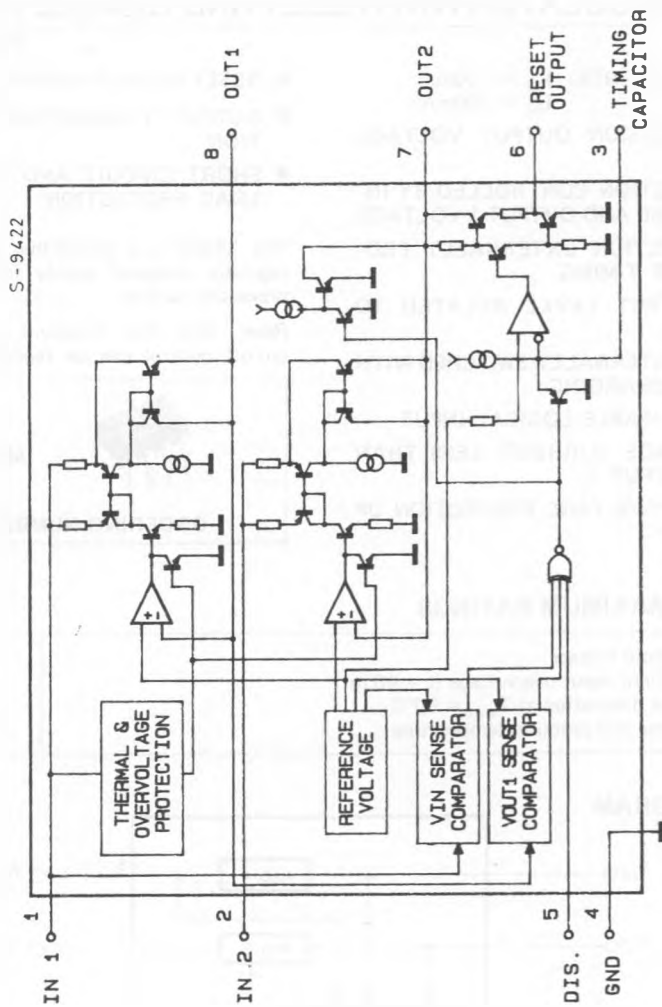
V_{IN}	DC input voltage	24	V
V_t	Transient input overvoltage ($t = 40\text{ ms}$)	60	V
P_{tot}	Power dissipation at $T_{amb} = 50^\circ\text{C}$	1	W
T_{stg}, T_j	Storage and junction temperature	-40 to 150	$^\circ\text{C}$

BLOCK DIAGRAM



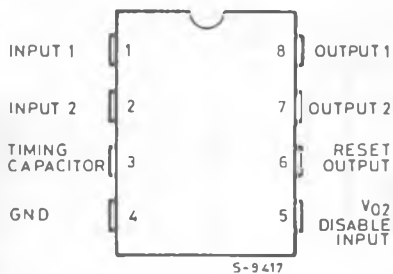
S-9416/2

SCHEMATIC DIAGRAM



CONNECTION DIAGRAM

(Top view)



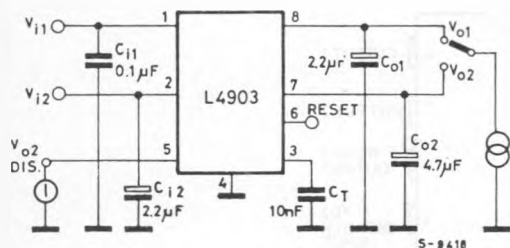
PIN FUNCTIONS

N°	NAME	FUNCTION
1	INPUT 1	Low quiescent current 50mA regulator input.
2	INPUT 2	100mA regulator input.
3	TIMING CAPACITOR	If Reg. 2 is switched-ON the delay capacitor is charged with a 10µA constant current. When Reg. 2 is switched-OFF the delay capacitor is discharged.
4	GND	Common ground.
5	V _{O2} DISABLE INPUT	A high level ($> V_{DT}$) disables output Reg. 2.
6	RESET OUTPUT	When pin 3 reaches 5V the reset output is switched low. Therefore $t_{RD} = C_1 \left(\frac{5V}{10\mu A} \right)$; $t_{RD} \text{ (ms)} = C_t \text{ (nF)}$.
7	OUTPUT 2	5V - 100mA regulator output. Enabled if $V_{O1} > V_{RT}$. $\text{DISABLE INPUT} < V_{DT}$ and $V_{IN2} > V_{IT}$. If Reg. 2 is switched OFF the C _{O2} capacitor is discharged.
8	OUTPUT 1	5V - 50mA regulator output with low leakage in switch-OFF condition.

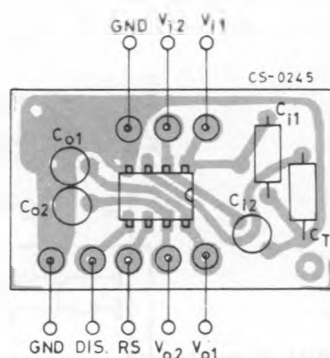
THERMAL DATA

R _{th j-pin}	Thermal resistance junction-pin 4	max	70	°C/W
R _{th j-amb}	Thermal resistance junction-ambient	max	100	°C/W

TEST CIRCUIT



P.C. board and components layout of the test circuit (1 : 1 scale)

ELECTRICAL CHARACTERISTICS ($V_{IN} = 14.4V$, $T_{amb} = 25^{\circ}C$ unless otherwise specified)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_i DC operating input voltage				20	V
V_{O1} Output voltage 1	R load 1K Ω	4.95	5.05	5.15	V
V_{O2H} Output voltage 2 HIGH	R load 1K Ω	$V_{O1} - 0.1$	5	V_{O1}	V
V_{O2L} Output voltage 2 LOW	$I_{O2} = -5mA$		0.1		V
I_{O1} Output current 1 max. (*)	$\Delta V_{O1} = -100mV$	50			mA
I_{LO1} Leakage output 1 current	$V_{IN} = 0$ $V_{O1} \leq 3V$			1	μA
I_{O2} Output current 2 max. (*)	$\Delta V_{O2} = -100mV$	100			mA
V_{IO1} Output 1 dropout voltage (*)	$I_{O1} = 10mA$ $I_{O1} = 50mA$		0.7 0.75	0.8 0.9	V V
V_{IT} Input threshold voltage		$V_{O1} + 1.2$	6.4	$V_{O1} + 1.7$	V
V_{ITH} Input threshold voltage hysteresis			250		mV
ΔV_{O1} Line regulation 1	$7V < V_{IN} < 18V$ $I_{O1} = 5mA$		5	50	mV
ΔV_{O2} Line regulation 2	$I_{O2} = 5mA$		5	50	mV
ΔV_{O1} Load regulation 1	$V_{IN1} = 8V$ $5mA < I_{O1} < 50mA$		5	20	mV
ΔV_{O2} Load regulation 2	$5mA < I_{O2} < 100mA$		10	50	mV
I_Q Quiescent current	$0 < V_{IN} < 13V$ $7V < V_{IN} < 13V$ V_{O2} LOW $7V < V_{IN} < 13V$ V_{O2} HIGH $I_{O1} = I_{O2} \leq 5mA$		4.5 2.7 1.6	6.5 4.5 3.5	mA mA mA
I_{Q1} Quiescent current 1	$6.3V < V_{IN1} < 13V$ $V_{IN2} = 0$ $I_{O1} \leq 5mA$ $I_{O2} = 0$		0.6	0.9	mA

ELECTRICAL CHARACTERISTICS (continued)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{RT} Reset threshold voltage		$V_{O2}-0.4$	4.7	$V_{O2}-0.2$	V
V_{RTH} Reset threshold hysteresis		30	50	80	mV
V_{RH} Reset output voltage HIGH	$I_R = 500\mu A$	$V_{O2}-1$	4.12	V_{O2}	V
V_{RL} Reset output voltage LOW	$I_R = -5mA$		0.25	0.4	V
t_{RD} Reset pulse delay	$C_t = 10nF$	3	5	11	ms
t_d Timing capacitor discharge time	$C_t = 10nF$			20	μs
V_{DT} V_{O2} disable threshold voltage			1.25	2.4	V
I_D V_{O2} disable input current	$V_D \leq 0.4V$ $V_D > 2.4V$		-150 30		μA μA
$\frac{\Delta V_{O1}}{\Delta T}$ Thermal drift	$-20^\circ C < T_{amb} < 125^\circ C$		0.3 -0.8		mV/ $^\circ C$
$\frac{\Delta V_{O2}}{\Delta T}$ Thermal drift	$-20^\circ C < T_{amb} < 125^\circ C$		0.3 -0.8		mV/ $^\circ C$
SVR1 Supply voltage rejection	$f = 100Hz$ $V_R = 0.5V$ $I_O = 50mA$	50	84		dB
SVR2 Supply voltage rejection	$I_O = 100mA$	50	80		dB
T_{JSD} Thermal shut down			150		$^\circ C$

* The dropout voltage is defined as the difference between the input and the output voltage when the output voltage is lowered of 25mV under constant output current conditions.

APPLICATION INFORMATION

In power supplies for μP systems it is necessary to provide power continuously to avoid loss of information in memories and in time of day clocks, or to save data when the primary supply is removed. The L4903 makes it very easy to supply such equipments; it provides two voltage regulators (both 5V high precision) with separate inputs plus a reset output for the data save function and Reg. 2 disable input.

CIRCUIT OPERATION (see Fig. 1)

After switch on Reg. 1 saturates until V_{O1} rises to the nominal value.

When the input 2 reaches V_{IT} and the output 1 is higher than V_{RT} the output 2 (V_{O2} and V_R) switches on and the reset output (V_R) goes low after a programmable time T_{RD} (timing capacitor).

V_{O2} is switched at low level and V_R at high level when one of the following conditions occurs:

- a high level ($> V_{DT}$) is applied on pin 5;
- an input overvoltage;
- an overload on the output 1 ($V_{O1} < V_{RT}$);
- a switch off ($V_{IN} < V_{IT} - V_{ITH}$);

and they start again as before when the condition is removed.

An overload on output 2 does not switch Reg. 2, and does not influence Reg. 1.

The V_{O1} output features:

- 5V internal reference without voltage divider between the output and the error comparator
- very low drop series regulator element utilizing current mirrors

permit high output impedance and then very low leakage current even in power down conditions.

This output may therefore be used to supply circuits continuously, such as volatile RAMs, allowing the use of a back-up battery.

CIRCUIT OPERATION (continued)

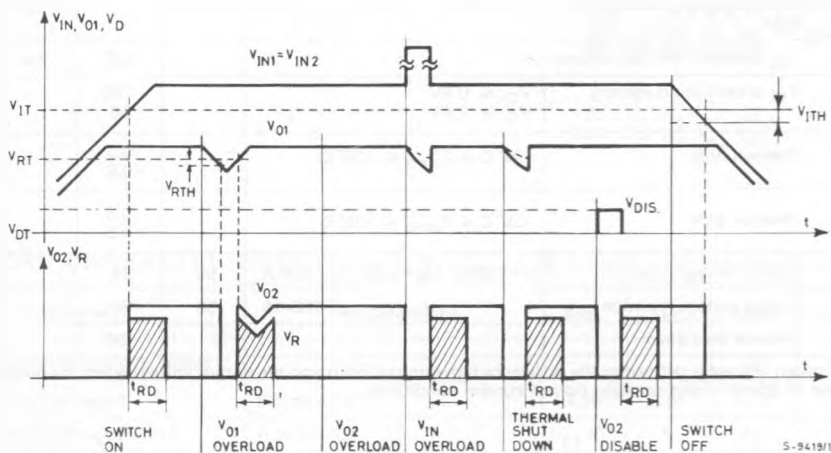
The V_{02} output can supply other non essential 5V circuits which may be powered down when the system is inactive, or that must be powered down to prevent uncorrect operation for supply voltages below the minimum value.

The reset output can be used as a "POWER DOWN INTERRUPT", permitting RAM access

only in correct power conditions, or as a "BACK-UP ENABLE" to transfer data into in a NV SHADOW MEMORY when the supply is interrupted.

The disable function can be used for remote on/off control of circuits connected to the V_{02} output.

Fig. 1



APPLICATION SUGGESTION

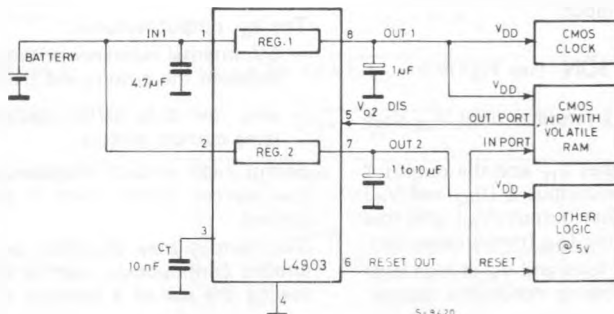
Fig. 2 illustrates how the L4903's disable input may be used in a CMOS μ Computer application.

The V_{01} regulator (low consumption) supply permanently a CMOS time of day clock and a CMOS μ computer chip with volatile memory. V_{02} output, supplying non-essential circuits, is

turned OFF under control of a μ P unit.

Configurations of this type are used in products where the OFF switch is part of a keyboard scanned by a micro which operates continuously even in the OFF state.

Fig. 2



APPLICATION SUGGESTIONS (continued)

Fig. 3 - Quiescent current (Reg. 1) vs. output current

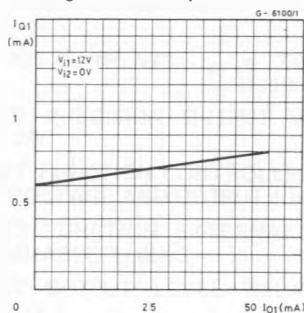


Fig. 4 - Quiescent current (Reg. 1) vs. input voltage

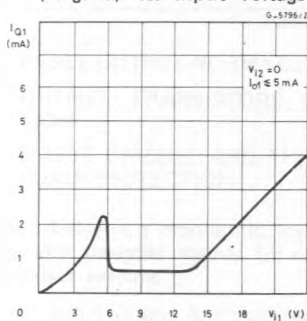


Fig. 5 - Total quiescent current vs. input voltage

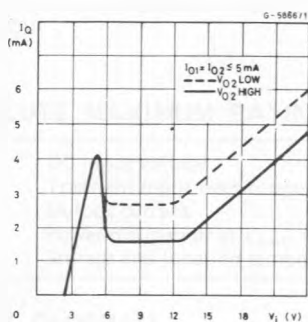


Fig. 6 - Supply voltage rejection regulators 1 and 2 vs. input ripple frequency

