

POWER FACTOR CORRECTOR

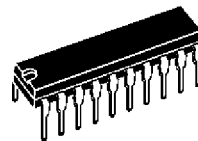
ADVANCE DATA

- CONTROL BOOST PWM UP TO 0.99P.F.
- LIMIT LINE CURRENT DISTORTION TO < 5%
- UNIVERSAL INPUT MAINS
- FEED FORWARD LINE AND LOAD REGULATION
- AVERAGE CURRENT MODE PWM FOR MINIMUM NOISE SENSITIVITY
- HIGH CURRENT BIPOLAR AND DMOS TO-TEM POLE OUTPUT
- LOW START-UP CURRENT (0.3mA TYP.)
- UNDER VOLTAGE LOCKOUT WITH HYSTERESIS AND PROGRAMMABLE TURN ON THRESHOLD
- OVERVOLTAGE, OVERCURRENT PROTECTION
- PRECISE 2% ON CHIP REFERENCE EXTERNALLY AVAILABLE
- SOFT START

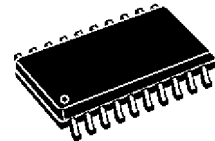
DESCRIPTION

The L4981 I.C. provides the necessary features to achieve a very high power factor up to 0.99. Realized in BCD 60II technology this power factor corrector (PFC) pre-regulator contains all the con-

MULTIPOWER BCD TECHNOLOGY



DIP 20



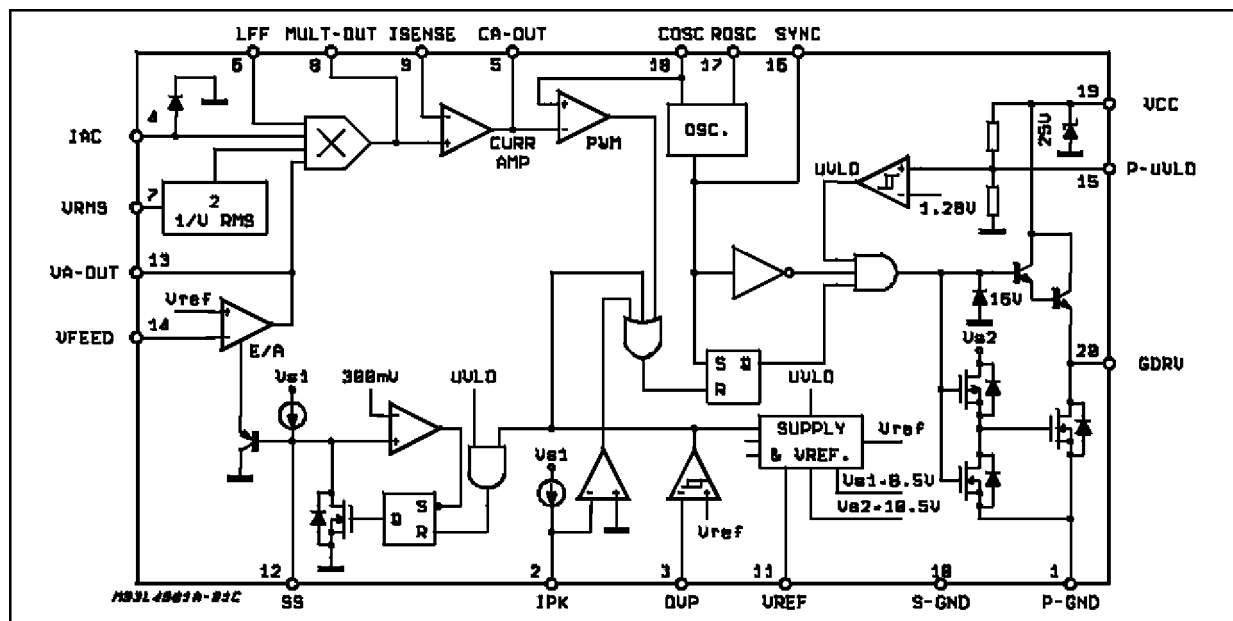
SO 20

ORDERING NUMBERS: L4981X (DIP 20)
L4981XD (SO 20)

rol functions for designing a high efficiency-mode power supply with sinusoidal line current consumption.

The L4981 can be easily used in systems with mains voltages between 85V to 265V without any line switch. This new PFC offers the possibility to work at fixed frequency (L4981A) or modulated frequency (L4981B) optimizing the size of the in-

BLOCK DIAGRAM



L4981A - L4981B

put filter; both the operating frequency modes working with an average current mode PWM controller, maintaining sinusoidal line current without slope compensation.

Besides power MOSFET gate driver, precise voltage reference (externally available), error amplifier, undervoltage lockout, current sense and the

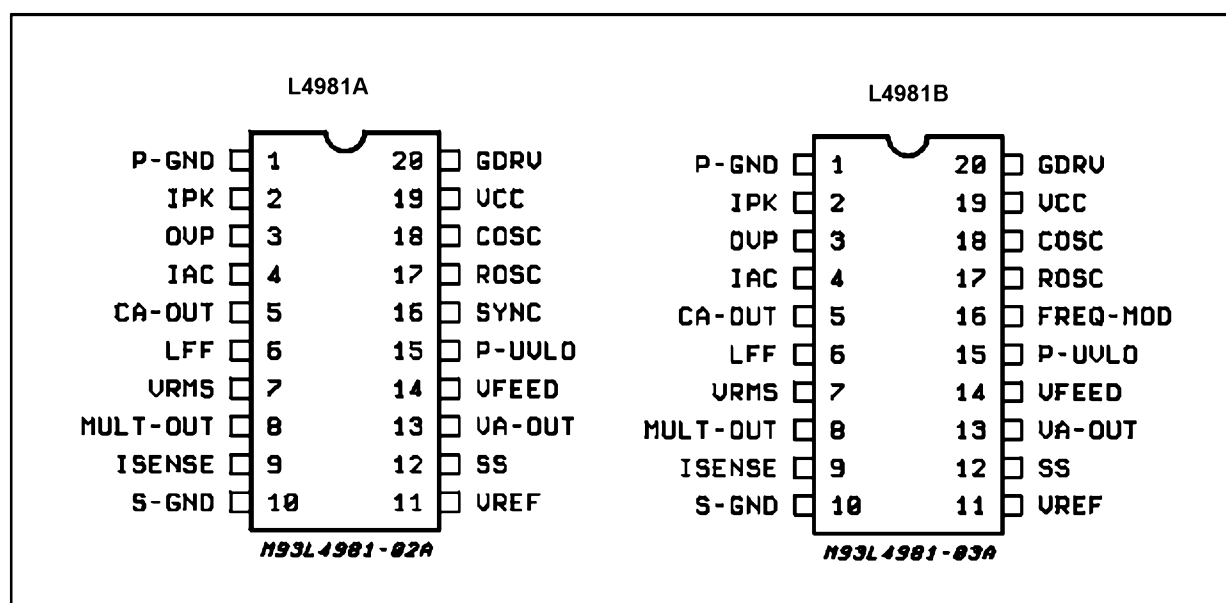
soft start are included. To limit the number of the external components, the device integrates protections as overvoltage and overcurrent. The overcurrent level can be programmed using a simple resistor for L4981A. For a better precision and for L4981B an external divider must be used.

ABSOLUTE MAXIMUM RATINGS

Symbol	Pin	Parameter		Value	Unit
V _{CC}	19	Supply Voltage (I _{CC} ≤ 50mA) (*)		selflimit	V
I _{GDRV}	20	Gate driv. output peak current (t = 1μs)	SINK	2	A
			SOURCE	1.5	A
V _{GDRV}		Gate driv. output voltage t = 0.1μs		-1	V
		Voltages at pins 3, 14, 7, 6, 12, 15		-0.3 to 9	V
V _{VA-OUT}	13	Error Amplifier Voltage		-0.3 to 8.5	V
I _{AC}	4	AC Input Current		5	mA
		Voltages at pin 8, 9		-0.5 to 7	V
V _{CA-OUT}	5	Current Amplifier Volt. (I _{source} = -20mA; I _{sink} = 20mA)		-0.3 to 8.5	V
V _{ROSC}	17	Voltage at pin 17		-0.3 to 3	V
	11, 18	Voltage at pin 11, 18		-0.3 to 7	V
I _{COSC}	18	Input Sink Current		15	mA
I _{FREQ-MOD}	16	Frequency Modulation Sink Current (L4981B)		5	mA
V _{SYNC}	16	Sync. Voltage (L4981A)		-0.3 to 7	V
V _{IPK}	2	Voltage at pin 2		-0.3 to 5.5	V
		Voltage at Pin 2 t = 1μs		-2	V
P _{tot}		Power Dissipation at T _{amb} = 70°C (DIP20)		1	W
		Power Dissipation at T _{amb} = 70°C (SO20)		0.6	W
T _{stg}		Storage Temperature		-55 to 150	°C

(*) Maximum package power dissipation limits must be observed.

PIN CONNECTIONS (Top views)



THERMAL DATA

Symbol	Parameter	DIP 20	SO 20	Unit
R _{th j-amb}	Thermal Resistance Junction-ambient	80	120	°C/W

PIN FUNCTIONS

N.	Name	Description
1	P-GND	Power ground.
2	IPK	L4981A peak current limiting. A current limitation is obtained using a single resistor connected between Pin 2 and the sense resistor. To have a better precision another resistor between Pin 2 and a reference voltage (Pin 11) must be added. L4981B peak current limiting. A precise current limitation is obtained using two external resistor only. These resistors must be connected between the sense resistor, Pin 2 and the reference voltage.
3	OVP	Overvoltage protection. At this input are compared an internal precise 5.1V (typ) voltage reference with a sample of the boost output voltage obtained via a resistive voltage divider in order to limit the maximum output peak voltage.
4	IAC	Input for the AC current. An input current proportional to the rectified mains voltage generates, via a multiplier, the current reference for the current amplifier.
5	CA-OUT	Current amplifier output. An external RC network determinates the loop gain.
6	LFF	Load feedforward; this voltage input pin allows to modify the multiplier output current proportionally to the load, in order to give a faster response versus load transient. The best control is obtained working between 1.5V and 5.3V. If this function is not used, connect this pin to the voltage reference (pin = 11).
7	VRMS	Input for proportional RMS line voltage. the VRMS input compesates the line voltage changes. Connecting a low pass filter between the rectified line and the pin 7, a DC voltage proportional to the input line RMS voltage is obtained. The best control is reached using input voltage between 1.5V and 6.5V. If this function is not used connect this pin to the voltage reference (pin = 11).
8	MULT-OUT	Multiplier output. This pin common to the multiplier output and the current amplifier N.I. input is an high impedance input like I _{SENSE} . The MULT-OUT pin must be taken not below -0.5V.
9	I _{SENSE}	Current amplifier inverting input. Care must be taken to avoid this pin goes down -0.5V.
10	S-GND	Signal ground.
11	V _{REF}	Output reference voltage (typ = 5.1V). Voltage refence at ± 2% of accuracy externally available, it's internally current limited and can deliver an output current up to 10mA.
12	SS	A capacitor connected to ground defines the soft start time. An internal current generator delivering 100μA (typ) charges the external capacitor defining the soft start time constant. An internal MOS discharge, the external soft start capacitor both in overvoltage and UVLO conditions.
13	VA-OUT	Error amplifier output, an RC network fixes the voltage loop gain characteristics.
14	VFEED	Voltage error amplifier inverting input. This feedback input is connected via a voltage divider to the boost output voltage.
15	P-UVLO	Programmable under voltage lock out threshold input. A voltage divider between supply voltage and GND can be connected in order to program the turn on threshold.
16	SYNC (L4981A)	This synchronization input/output pin is CMOS logic compatible. Operating as SYNC in, a rectangular wave must be applied at this pin. Opearting as SYNC out, a rectangular clock pulse train is available to synchronize other devices.
	FREQ-MOD (L4981B)	Frequency modulation current input. An external resistor must be connected between pin 16 and the rectified line voltage in order to modulate the oscillator frequency. Connecting pin 16 to ground a fixed frequency imposed by R _{OSC} and C _{OSC} is obtained.
17	R _{OSC}	An external resistor connected to ground fixes the constant charging current of C _{OSC} .
18	C _{OSC}	An external capacitor connected to GND fixes the switching frequency.
19	V _{CC}	Supply input voltage.
20	GDRV	Output gate driver. Bipolar and DMOS transistors totem pole output stage can deliver peak current in excess 1A useful to drive MOSFET or IGBT power stages.

L4981A - L4981B

ELECTRICAL CHARACTERISTICS (Unless otherwise specified $V_{CC} = 18V$, $C_{OSC} = 1nF$, $R_{OSC} = 24K\Omega$, $C_{SS} = 1\mu F$, $V_{CA-OUT} = 3.5V$, $V_{ISENSE} = 0V$, $V_{LFF} = V_{REF}$, $I_{AC} = 100\mu A$, $V_{RMS} = 1V$, $V_{FEED} = GND$, $V_{IPK} = 1V$, $V_{OVP} = 1V$, $T_J = 25^\circ C$)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
ERROR AMPLIFIER SECTION						
V _{IO}	Input Offset Voltage	-25°C < T _J < 85°C			±8	mV
I _{IB}	Input Bias Current	V _{FEED} = 0V	-500	-50	500	nA
	Open Loop Gain		70	100		dB
V _{13H}	Output High voltage	V _{FEED} = 4.7V I _{VA-OUT} = -0.5mA	5.5	6.5	7.5	V
V _{13L}	Output Low Voltage	V _{FEED} = 5.5V I _{VA-OUT} = 0.5mA		0.4	1	V
-I ₁₃	Output Source Current	V _{FEED} = 4.7V; V _{VA-OUT} = 3.5V	2	10		mA
I ₁₃	Output Sink Current	V _{FEED} = 5.5V; V _{VA-OUT} = 3.5V	4	20		mA
REFERENCE SECTION						
V _{ref}	Reference Output Voltage	-25°C < T _J < 85°C	4.97	5.1	5.23	V
		T _J = 25°C I _{ref} = 0	5.01	5.1	5.19	V
ΔV _{ref}	Load Regulation	1mA ≤ I _{ref} ≤ 10mA -25°C < T _J < 85°C		3	15	mV
ΔV _{ref}	Line Regulation	12V ≤ V _{CC} ≤ 19V -25°C < T _J < 85°C		3	10	mV
I _{ref sc}	Short Circuit Current	V _{ref} = 0V	20	30	50	mA
OSCILLATOR SECTION						
f _{osc}	Initial Accuracy	T _J = 25°C	85	100	115	KHz
	Frequency Stability	12V ≤ V _{CC} ≤ 19V -25°C < T _J < 85°C	80	100	120	KHz
V _{svp}	Ramp Valley to Peak		4.7	5	5.3	V
I _{18C}	Charge Current	V _{COSC} = 3.5V	0.45	0.55	0.65	mA
I _{18D}	Discharge Current	V _{COSC} = 3.5V		11.5		mA
V ₁₈	Ramp Valley Voltage		0.9	1.15	1.4	V
SYNC SECTION (Only for L4981A)						
t _w	Output Pulse Width	50% Amplitude	0.3	0.8		μs
I ₁₆	Sink Current with Low Output Voltage	V _{SYNC} = 0.4V V _{COSC} = 0V	0.4	0.8		mA
-I ₁₆	Source Current with High Output Voltage	V _{SYNC} = 4.5V V _{COSC} = 6.7V	1	6		mA
V _{16L}	Low Input Voltage				0.9	V
V _{16H}	High Input Voltage		3.5			V
t _d	Pulse for Synchronization		800			ns
FREQUENCY MODULATION FUNCTION (Only for L4981B)						
f _{18max}	Maximum Oscillation Frequency	V _{FREQ-MOD} = 0V (Pin 16) I _{freq} = 0	85	100	115	KHz
f _{18min}	Minimum Oscillator Frequency	I _{FREQ-MOD} = 360μA (Pin 16) V _{VRMS} = 4V (Pin 7)		74		KHz
		I _{FREQ-MOD} = 180μA (Pin 16) V _{VRMS} = 2V (Pin 7)		76		KHz
SOFT START SECTION						
I _{SS}	Soft Start Source Current	V _{SS} = 3V	60	100	140	μA
V _{12sat}	Output Saturation Voltage	V ₃ = 6V, I _{SS} = 2mA		0.1	0.25	V

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
SUPPLY VOLTAGE						
V _{CC}	Operating Supply Voltage				19.5	V
OVER VOLTAGE PROTECTION COMPARATOR						
V _{thr}	Rising Threshold Voltage		V _{ref} -20mV	5.1	V _{ref} +20mV	V
V _{3Hys}	Hysteresis		180	250	320	mV
I ₃	Input Bias Current			0.05	1	μA
t _d	Propagation delay to output	V _{OVP} = V _{thr} +100mV		1	2	μs
OVER CURRENT PROTECTION COMPARATOR						
V _{th}	Threshold Voltage				±30	mV
t _d	Propagation delay to Output	V _{OCP} = V _{thr} -0.2V		0.4	0.9	μs
I _{ipk}	Current Source Generator	V _{IPK} = -0.1V only for L4981A	65	85	105	μA
I _L	Leakage Current	V _{IPK} = -0.1V only for L4981B			5	μA
CURRENT AMPLIFIER SECTION						
V _{offset}	Input Offset Voltage	V _{MULT OUT} = V _{SENSE} = 3.5V			±2	mV
I _{gbias}	Input Bias Current	V _{SENSE} = 0V	-500	50	500	nA
	Open Loop Gain	1.1V ≤ V _{CA OUT} ≤ 6V	70	100		dB
SVR	Supply Voltage Rejection	12V ≤ V _{CC} ≤ 19V V _{MULT OUT} = 3.5V V _{SENSE} = 3.5V	68	90		dB
V _{5H}	Output High Voltage	V _{MULT OUT} = 200mV I _{CA OUT} = -0.5mA, V _{IAC} = 0V	6.2			V
V _{5L}	Output Low Voltage	V _{MULT OUT} = -200mV I _{CA OUT} = 0.5mA, V _{IAC} = 0V			0.9	V
-I ₅	Output Source Current	V _{MULT OUT} = 200mV, V _{IAC} = 0V, V _{CA-OUT} = 3.5V	2	10		mA
I ₅	Output Sink Current		2	10		mA
OUTPUT SECTION						
V _{20L}	Output Voltage Low	I _{SINK} = 250mA		0.5	0.8	V
V _{20H}	Output Voltage High	I _{SOURCE} = 250mA V _{CC} = 15V	11.5	12.5		V
t _r	Output Voltage Rise Time	C _{OUT} = 1nF		50	150	ns
t _f	Output Voltage Fall Time	C _{OUT} = 1nF		30	100	ns
V _{GDRV}	Voltage Clamp	I _{SOURCE} = 0mA	13	16	19	V
TOTAL STANDBY CURRENT SECTION						
I _{19start}	Supply Current before start up	V _{CC} = 14V		0.3	0.5	mA
I _{19on}	Supply Current after turn on	V _{IAC} = 0V, V _{COSC} = 0, Pin17 = Open		8	12	mA
I ₁₉	Operating Supply Current	Pin20 = 1nF		12	16	mA
V _{CC}	Zener Voltage	(*)	20	25	30	V
UNDER VOLTAGE LOCKOUT SECTION						
V _{th ON}	Turn on Threshold		14.5	15.5	16.5	V
V _{th OFF}	Turn off Threshold		9	10	11	V
	Programmable Turn-on Threshold	Pin 15 to V _{CC} = 220K Pin15 to GND = 33K	10.6	12	13.4	V
LOAD FEED FORWARD						
I _{LFF}	Bias Current	V ₆ = 1.6V		70	140	μA
		V ₆ = 5.3V		200	300	μA
V _i	Input Voltage Range		1.6		5.3	V

(*) Maximum package power dissipation limits must be observed.

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
MULTIPLIER SECTION						
	Multiplier Output Current	$V_{VA-OUT} = 4V, V_{RMS} = 2V, V_{MULTOUT} = 0, V_{LFF} = 5.1V, I_{AC} = 50\mu A, C_{OSC} = 0V$	20	35	52	μA
		$V_{VA-OUT} = 4V, V_{RMS} = 2V, V_{MULTOUT} = 0, V_{LFF} = 5.1V, I_{AC} = 200\mu A, C_{OSC} = 0V$	100	135	170	μA
		$V_{VA-OUT} = 2V, V_{RMS} = 2V, V_{MULTOUT} = 0, V_{LFF} = 5.1V, I_{AC} = 100\mu A, C_{OSC} = 0V$	10	20	30	μA
		$V_{VA-OUT} = 2V, V_{RMS} = 4V, V_{MULTOUT} = 0, V_{LFF} = 5.1V, I_{AC} = 100\mu A, C_{OSC} = 0V$	2	5.5	11	μA
		$V_{VA-OUT} = 4V, V_{RMS} = 4V, V_{MULTOUT} = 0, V_{LFF} = 5.1V, I_{AC} = 100\mu A, C_{OSC} = 0V$	10	22	34	μA
		$V_{VA-OUT} = 4V, V_{RMS} = 2V, V_{MULTOUT} = 0, V_{LFF} = 2.5V, C_{OSC} = 0V, I_{AC} = 200\mu A$	20	37	54	μA
		$V_{VA-OUT} = 4V, V_{RMS} = 4V, V_{MULTOUT} = 0, V_{LFF} = 5.1V, I_{AC} = 200\mu A, C_{OSC} = 0V$	20	39	54	μA
		$V_{VA-OUT} = 2V, V_{RMS} = 4V, V_{MULTOUT} = 0, V_{LFF} = 5.1V, I_{AC} = 0, C_{OSC} = 0V$	-2	0	2	μA
K	Multiplier Gain			0.37		

$$I_{MULT\pm OUT} = K \cdot I_{AC} \frac{(V_{VA\pm OUT} \pm 1.28) \cdot (0.8 \cdot V_{LFF} \pm 1.28)}{(V_{RMS})^2}$$

$$\text{if } V_{LFF} = V_{REF}; I_{MULT\pm OUT} = I_{AC} \frac{(V_{VA\pm OUT} \pm 1.28)}{(V_{RMS})^2} \cdot K1$$

where: $K1 = 1V$

Figure 1: MULTI-OUT vs. I_{AC} ($V_{RMS} = 1.7V$; $V_{LFFD} = 5.1V$)

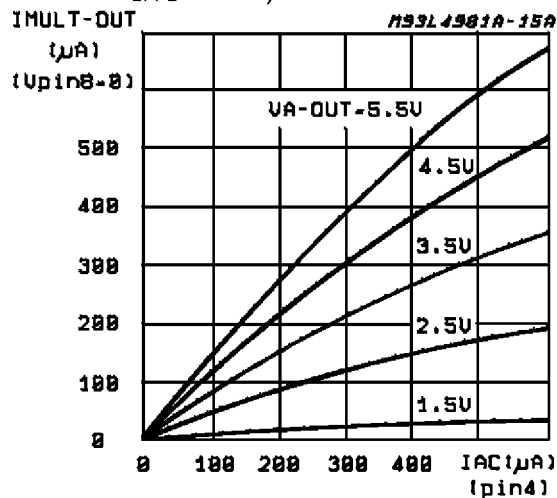


Figure 2: MULTI-OUT vs. I_{AC} ($V_{RMS} = 2.2V$; $V_{LFFD} = 5.1V$)

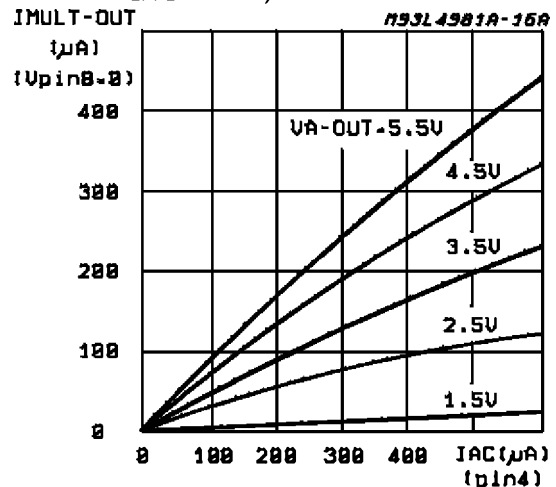


Figure 3: MULTI-OUT vs. I_{AC} ($V_{RMS} = 4.4V$;
 $V_{LFFD} = 5.1V$)

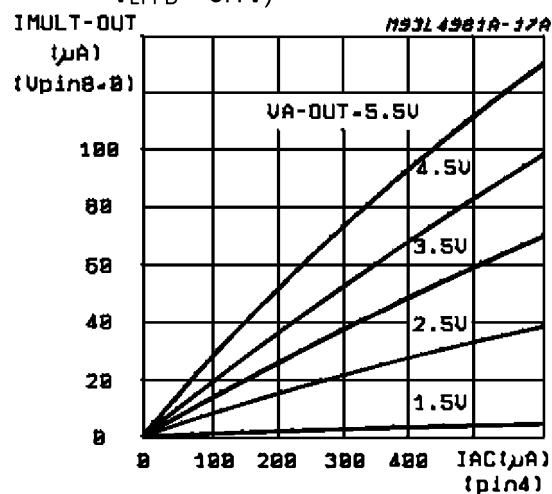


Figure 4: MULTI-OUT vs. I_{AC} ($V_{RMS} = 5.3V$;
 $V_{LFFD} = 5.1V$)

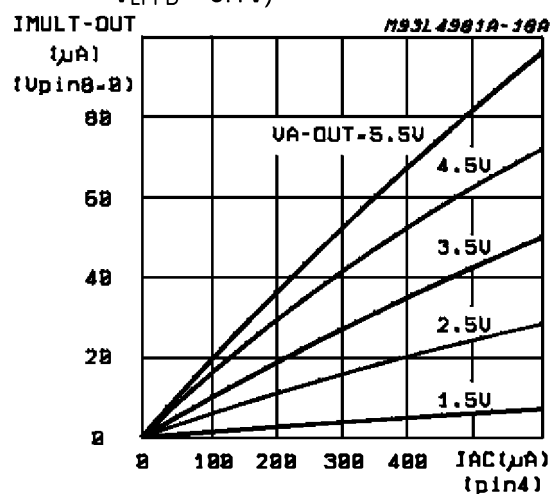


Figure 5: MULTI-OUT vs. I_{AC} ($V_{RMS} = 1.7V$;
 $V_{LFFD} = 2.5V$)

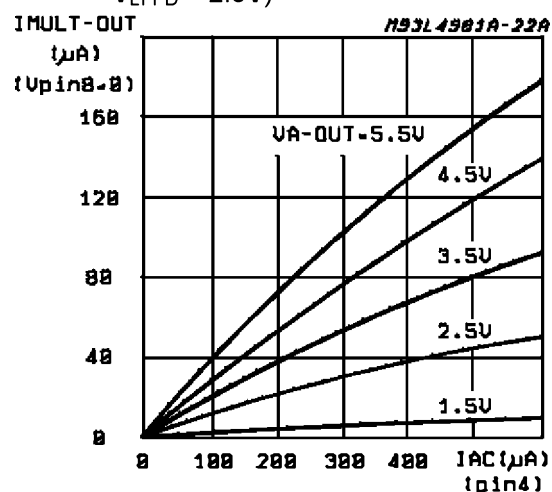


Figure 6: MULTI-OUT vs. I_{AC} ($V_{RMS} = 2.2V$;
 $V_{LFFD} = 2.5V$)

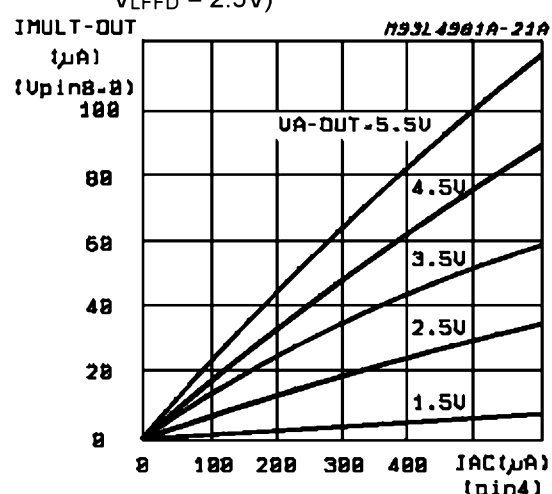


Figure 7: MULTI-OUT vs. I_{AC} ($V_{RMS} = 4.4V$;
 $V_{LFFD} = 2.5V$)

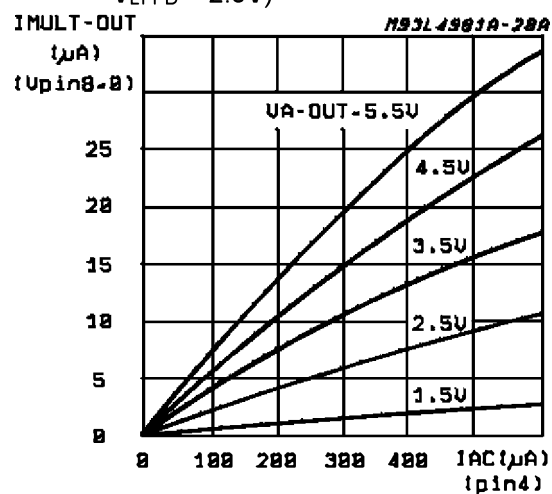
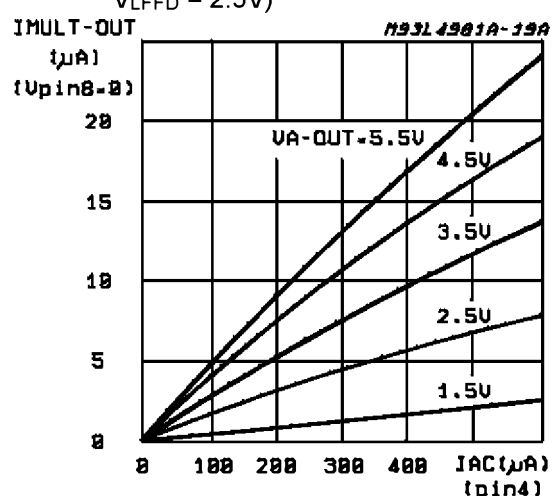
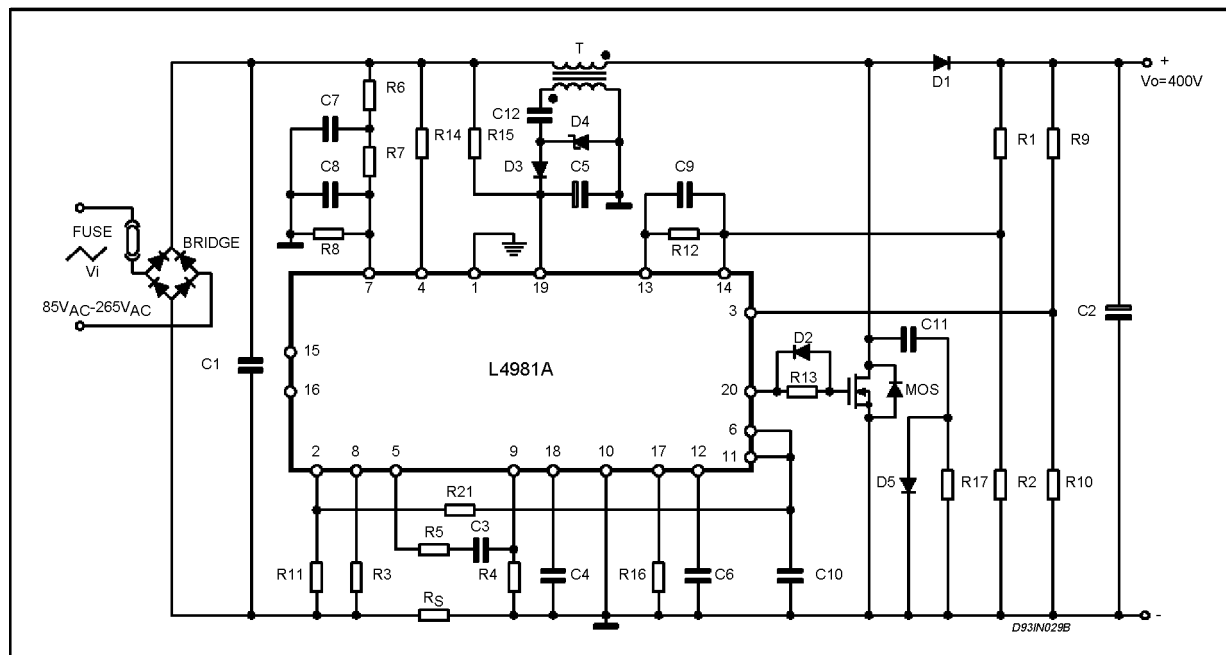


Figure 8: MULTI-OUT vs. I_{AC} ($V_{RMS} = 5.3V$;
 $V_{LFFD} = 2.5V$)



L4981A - L4981B

Figure 9A: L4981A Power Factor Corrector (200W)



PART LIST

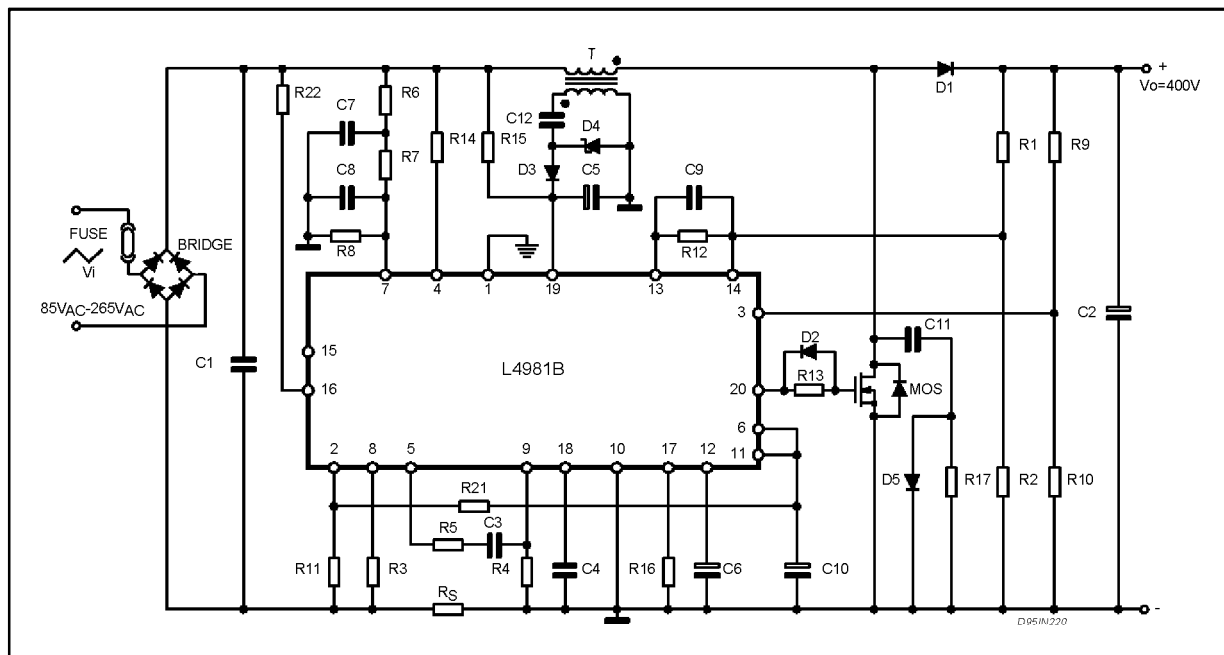
R_S	0.07(3 x .22)	1/2W	5%
R1	820kΩ	1/4W	1%
R2	10kΩ	1/4W	1%
R3	1.8kΩ	1/4W	5%
R4	1.8kΩ	1/4W	5%
R5	18kΩ	1/4W	5%
R6	1.2MΩ	1/4W	5%
R7	360kΩ	1/4W	5%
R8	33kΩ	1/4W	5%
R9	1.8MΩ	1/4W	1%
R10	21kΩ	1/4W	1%
R11	402Ω	1/4W	1%
R12	120kΩ	1/4W	5%
R13	27Ω	1/4W	5%
R14	1MΩ	1/4W	1%
R15	120kΩ	1/2W	5%
R16	30kΩ	1/4W	5%
R17	1.8kΩ	4W	1%
R21	5.1kΩ	1/4W	1%
BRIDGE = 4 x P600M			

C1	470nF	400V
C2	100μF	450V
C3	2.2nF	
C4	1nF	
C5	100μF	25V
C6	1μF	16V
C7	220nF	63V
C8	220nF	63V
C9	330nF	
C10	1μF	16V
C11	270pF	400V
C12	8.2nF	100V
D1	STTA506D	
D2, D3	1N4148	
D4	18V	1/2W
D5	BYT11-600	
MOS	STH15NA50	
FUSE = 4A/250V		

T = primary: 88 turns of 12 x 32 AWG (0.2mm)
 secondary: 9 turns of # 27AWG (0.15mm)
 core: B1ET3411A THOMSON - CSF
 gap: 1,6mm for a total primary inductance of 0.9mH

f_{sw} = 80kHz P_O = 200W
 V_{OUT} = 400V I_{rms max} = 2.53A
 V_{OVP} = 442V I_{PK max} = 6.2A

Figure 9B: L4981B Power Factor Corrector (200W)



PART LIST

R_S	0.07(3 x .22)	1/2W	5%
R1	820k Ω	1/4W	1%
R2	10k Ω	1/4W	1%
R3	1.8k Ω	1/4W	5%
R4	1.8k Ω	1/4W	5%
R5	18k Ω	1/4W	5%
R6	1.2M Ω	1/4W	5%
R7	360k Ω	1/4W	5%
R8	33k Ω	1/4W	5%
R9	1.8M Ω	1/4W	1%
R10	21k Ω	1/4W	1%
R11	402 Ω	1/4W	1%
R12	120k Ω	1/4W	5%
R13	27 Ω	1/4W	5%
R14	1M Ω	1/4W	1%
R15	120k Ω	1/2W	5%
R16	24k Ω	1/4W	5%
R17	1.8k Ω	4W	1%
R21	5.1k Ω	1/4W	1%
R22	1.1M Ω	1/4W	1%
BRIDGE = 4 x P600M			

C1	470nF	400V
C2	100 μ F	450V
C3	2.2nF	
C4	1.1nF	
C5	100 μ F	25V
C6	1 μ F	16V
C7	220nF	63V
C8	220nF	63V
C9	330nF	
C10	1 μ F	16V
C11	270pF	400V
C12	8.2nF	100V
D1	STTA506D	
D2, D3	1N4148	
D4	18V	1/2W
D5	BYT11-600	
MOS	STH15NA50	
FUSE = 4A/250V		

T = primary: 88 turns of 12 x 32 AWG (0.2mm)
 secondary: 9 turns of # 27AWG (0.15mm)
 core: B1ET3411A THOMSON - CSF
 gap: 1,6mm for a total primary inductance of 0.9mH

f_{sw} = 80 to 92kHz P_O = 200W
 V_{OUT} = 400V I_{rms max} = 2.53A
 V_{OV} = 442V I_{PK max} = 6.2A

Figure 10: Reference Voltage vs. Source Reference Current

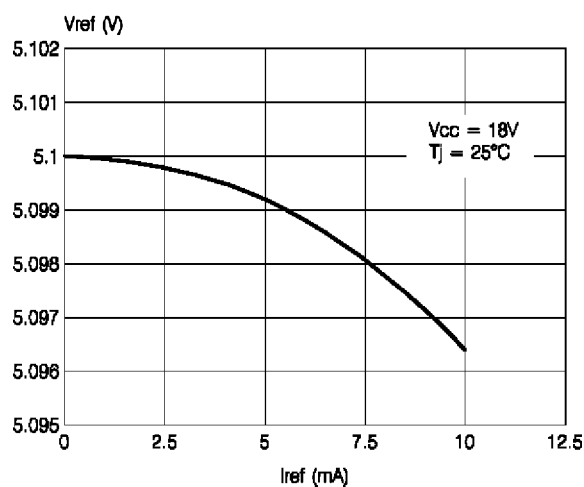


Figure 11: Reference Voltage vs. Supply Voltage

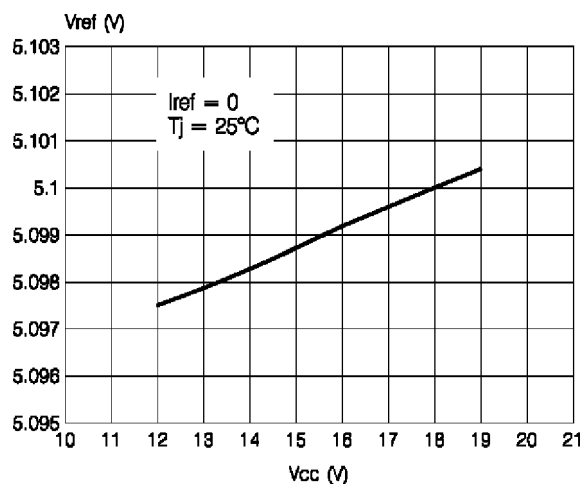


Figure 12: Reference Voltage vs. Junction Temperature

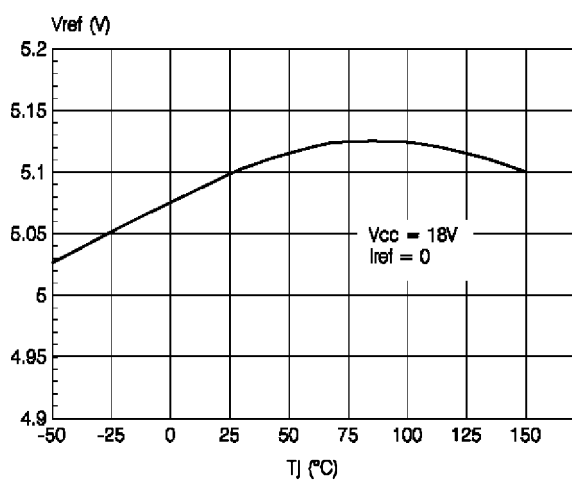


Figure 13: Switching Frequency vs. Junction Temperature

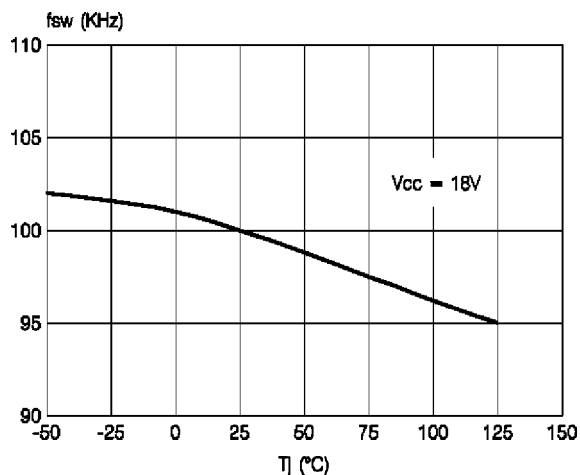


Figure 14: Gate Driver Rise and Fall Time

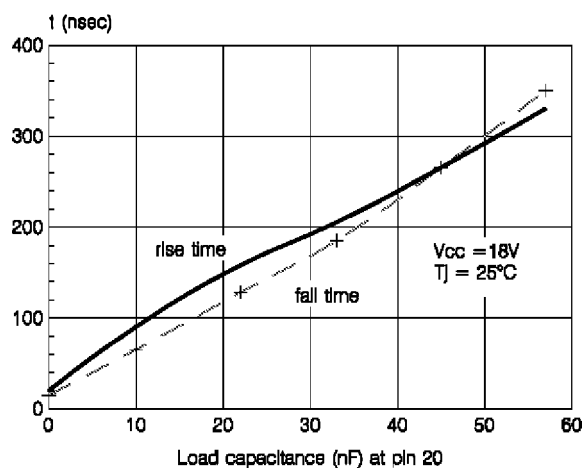


Figure 15: Operating Supply Current vs. Supply Voltage

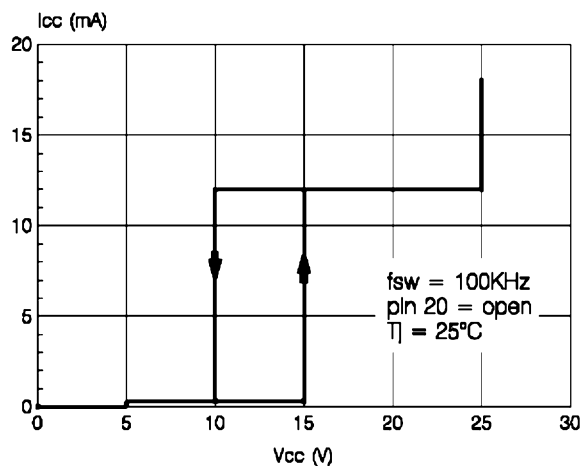
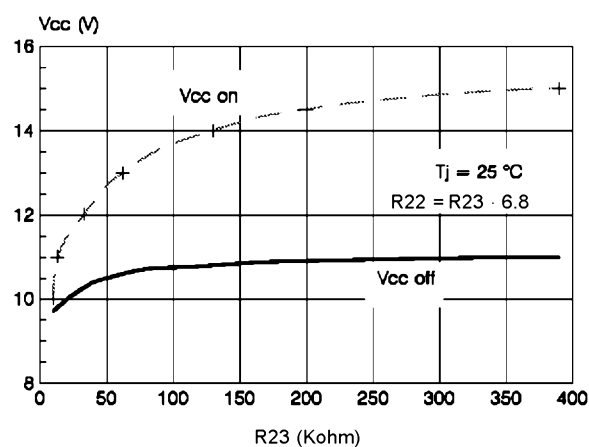
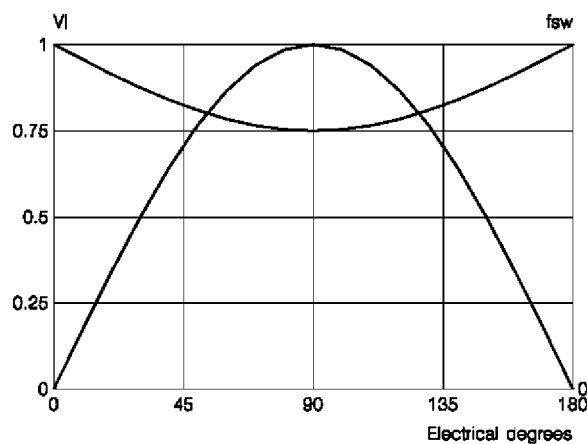


Figure 16: Programmable Under Voltage Lock-out Thresholds**Figure 17:** Modulation Frequency Normalized in an Half Cycle of the Mains Voltage**Table 1:** Programmable Under Voltage Lockout Thresholds.

V _{CC ON}	V _{CC OFF}	R22	R23
11V	10V	82kΩ	12kΩ
12V	10.1V	220kΩ	33kΩ
13V	10.5V	430kΩ	62kΩ
14V	10.8V	909kΩ	133kΩ
14.5V	10.9V	1.36MΩ	200kΩ
15V	11V	2.7MΩ	390kΩ

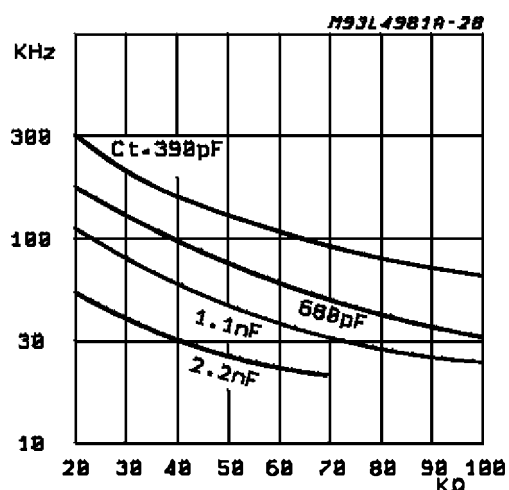
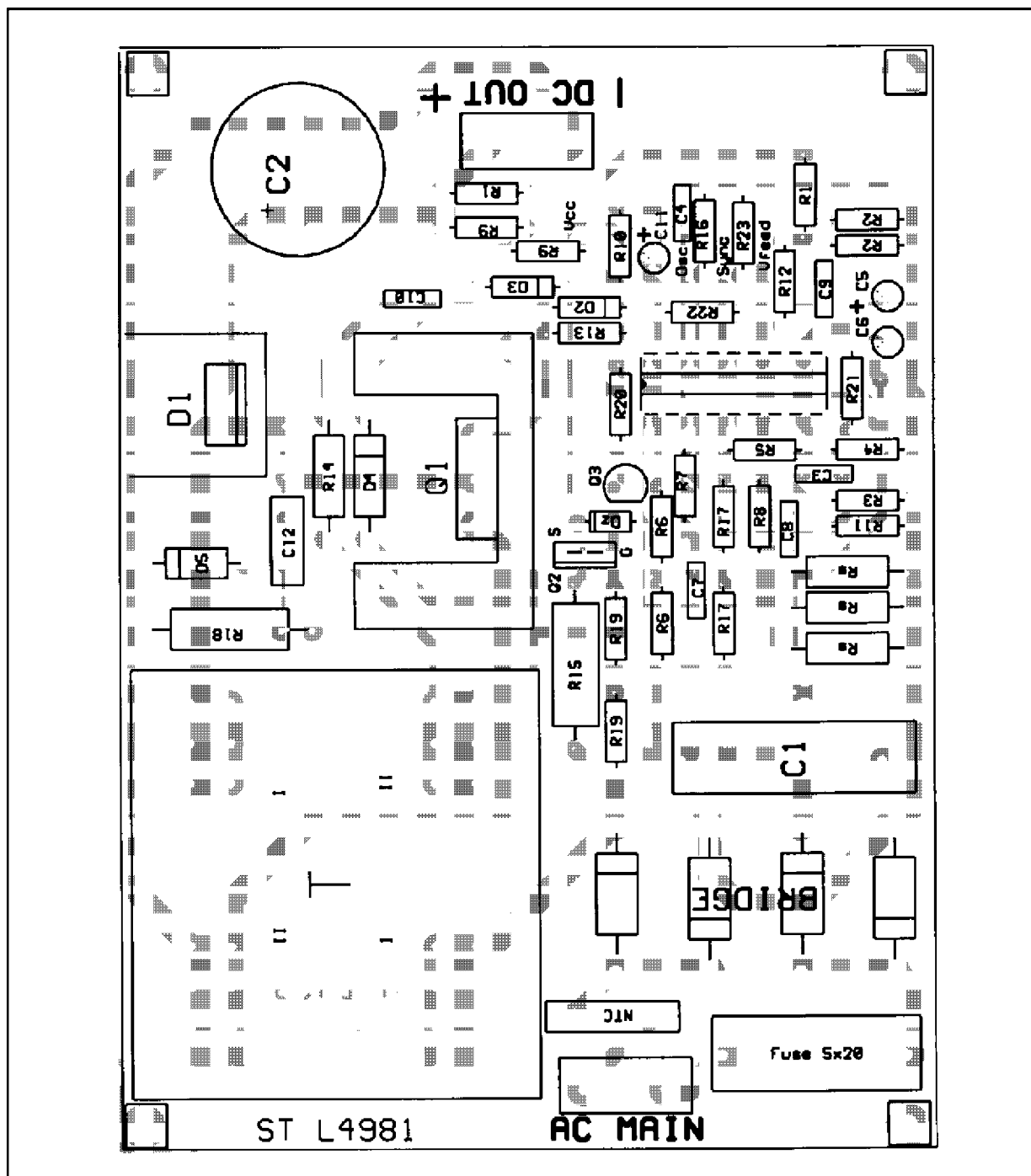
Figure 18: Oscillator Diagram

Figure 20: P.C. Board and Component Layout of Evaluation Board Circuit (1:1 scale).



The evaluation board has been designed using: a faster not dissipative start-up circuit, a diode (D2) to speed-up the MOS start-off time and (even if a single resistor can be used) an external divider to improve the precision of the overcurrent threshold.

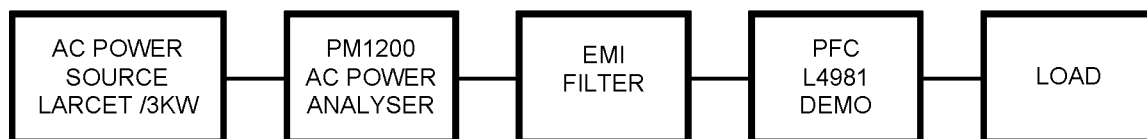
Further there is a possibility to change the input threshold voltage using an external divider (R23 and R22) and if an inrush current problem arises

a NTC resistor can be used.

The PFC demoboard performances has been evaluated testing the following parameters:

PF (power factor), A-THD (percentage of current total harmonic distortion), H3..H9 (percentage of current's n^{th} harmonic amplitude), ΔV_o (output voltage ripple), V_o (output voltage), η (efficiency).

The test configuration, equipments and results are:



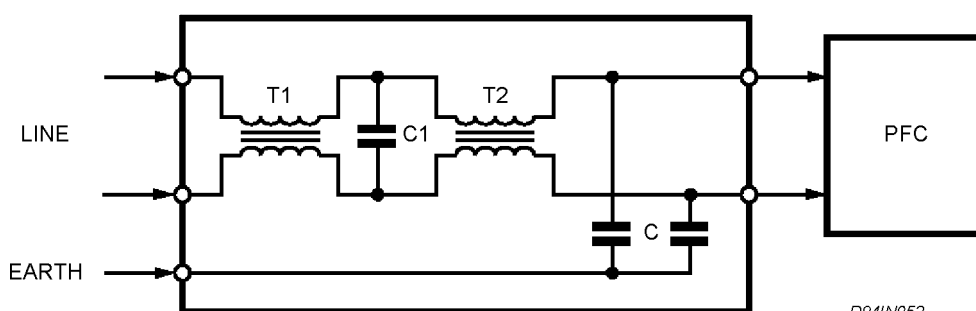
D94IN057

V_i (V _{rms})	f (Hz)	P_i (W)	PF	A-THD (%)	H3 (%)	H5 (%)	H7 (%)	H9 (%)	V_o (V)	ΔV_o (V)	PO (W)	η (%)
88	60	222	0.999	2.94	1.98	0.61	0.55	0.70	390	8	200	90.2
110	60	220	0.999	1.79	1.40	0.40	0.31	0.28	392	8	201	91.6
132	60	218	0.999	1.71	1.16	0.40	0.35	0.31	394	8	202	92.8
180	50	217	0.999	1.88	1.52	0.65	0.40	0.34	396	8	203	93.8
220	50	217	0.997	2.25	1.68	0.83	0.57	0.48	398	8	204	94.2
260	50	216	0.995	3.30	1.84	1.30	0.39	0.73	400	8	205	95.2

EMI/RFI FILTER

The harmonic content measurement has been done using an EMI/RFI filter interposed between

the AC source and the demoboard under test, while the efficiency has been calculated without the filter contribution.



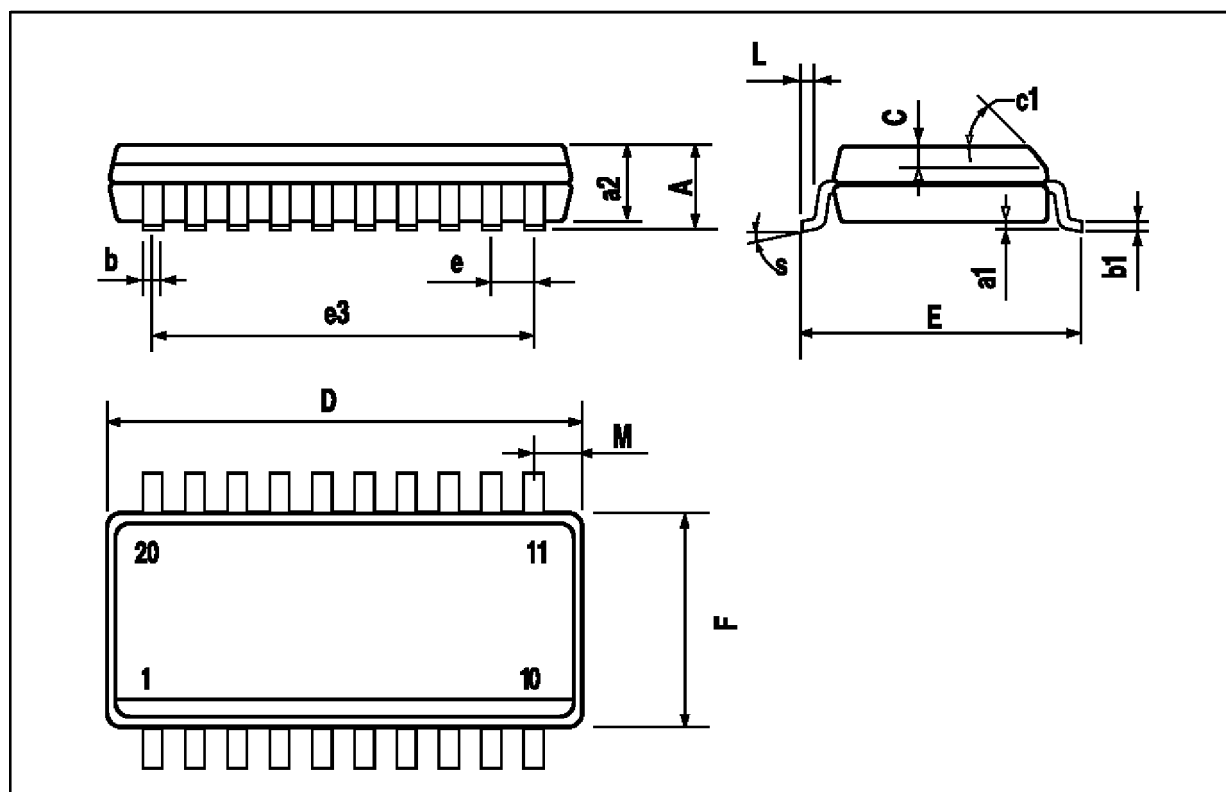
D94IN052

where:

T1 = 1mH C1 = 0.33 μ F, 630V
T2 = 27mH C2 = 2.2nF, 630V

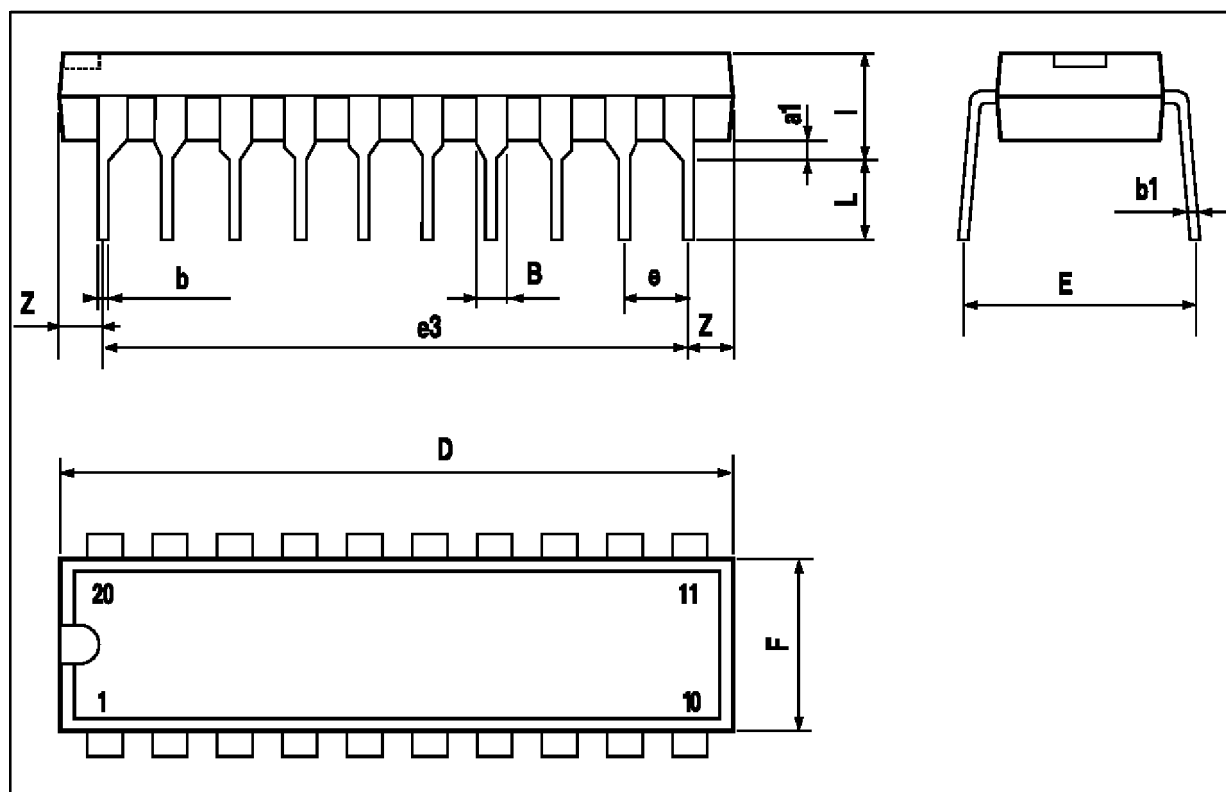
SO20 PACKAGE MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			2.65			0.104
a1	0.1		0.2	0.004		0.008
a2			2.45			0.096
b	0.35		0.49	0.014		0.019
b1	0.23		0.32	0.009		0.013
C		0.5			0.020	
c1	45° (typ.)					
D	12.6		13.0	0.496		0.510
E	10		10.65	0.394		0.419
e		1.27			0.050	
e3		11.43			0.450	
F	7.4		7.6	0.291		0.300
L	0.5		1.27	0.020		0.050
M			0.75			0.030
S	8° (max.)					



DIP20 PACKAGE MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
a1	0.254			0.010		
B	1.39		1.65	0.055		0.065
b		0.45			0.018	
b1		0.25			0.010	
D			25.4			1.000
E		8.5			0.335	
e		2.54			0.100	
e3		22.86			0.900	
F			7.1			0.280
I			3.93			0.155
L		3.3			0.130	
Z			1.34			0.053



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