Ordering number: EN2412A

CMOS LSI

SANYO No. 2412A

LC6568D, 6568H

8K-Byte ROM-Contained Single-Chip 4-Bit Microcomputers with FLT/LED Drivers, Comparator Input

The LC6568D/H are single-chip 4-bit microcomputers that contain an 8K-byte ROM, 1K-bit RAM, and have 64 pins. The LC6568D/H have 57 pins for ports — 28 pins for 7 input/output common ports, 21 pins for 6 output ports, and 8 pins for 2 input ports. The LC6568D/H have specific ports that are used to provide the interrupt function, 4-bit/8-bit serial input/output function and burst pulse output function. Each of the 28 pins for input/output common ports contains a driver with a withstand voltage of 15V max. and a drive current of 15mA max. and each of the 21 pins for output ports contains a high-voltage output driver of the P-channel open drain type. Since the high-voltage output driver can be used as general-purpose high-current driver as well as fluorescent tube driver, the LC6568D/H can be also widely used in applications where no fluorescent display is provided.
The LC6568D/H are the same as our LC6500 series in the basic architecture of the CPU and the instruction set, but are made more powerful in the stack level and also made easier-to-use in the standby function.

Features

- Instruction set with 81 instructions (Common to the LC6500 series)
- On-chip 8192-byte ROM, 1024-bit RAM
- Instruction cycle time: 2.77 μs (D version, V_{DD} = 4 to 6V)
  0.92 μs (H version, V_{DD} = 4.5 to 6V)
- Serial input/output interface x 1 (4 bits/8 bits program-selectable)
- I/O ports: 57 pins in all
  Input ports 8 pins
  Input/output common ports 28 pins: 15V max., 15mA max., LED drivable, pull-up resistance option available
  Output ports 21 pins: V_{DD}−45V withstand voltage, FLT drivable, common with general-purpose output, pull-down resistance option available
  Output level during reset: For ports C, D, output (H or L) during reset may be specified portwise by option.
- Interrupt function
  Timer interrupt: 1 line
  $\overline{\text{INT0 to 3}}$ pin or serial I/O interrupt: 1 line
- Stack level: 8 levels (Common with interrupt)
- Timer: 4-bit prescaler +8-bit programmable timer
- Burst pulse (64 x cycle time, dury 50%) output function
- Oscillator option
  Circuit mode: Ceramic resonator mode, RC mode, external clock mode (384kHz to 4.33MHz)
  Predivider option: 1/1, 1/3, 1/4
- Standby function: Standby function provided by the HALT instruction. Provides the function to absorb the OSC stabilizing time in the ceramic resonator mode.
- Supply Voltage: 4 to 6V (D version)
  4.5 to 6V (H version)
- Package: DIP 64 shrink type, QIP64A
- Evaluation LSI: LC6595 (Evaluation chip) + EVA800-TB6568 (Evaluation chip board),
  LC65PG68 (Piggyback)
- 4-channel comparator input
- 4-channel external interrupt input (1 vector)

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Development Support Tools

The following development tools are available.

1. Document support	·····	(1)	Documentation LC6568 User's Manual
		(2)	Development Tools User's Manual, EVA800-LC6568
2. Software support	·····	(1)	MS-DOS (Note) for the host system and cross-assembler software i. Host processor control program ii. LC65S.EXE cross assembler
3. Hardware support	·····	(1)	Evaluation chip: LC6595
		(2)	Piggyback microcomputer: LC65PG68
		(3)	Emulator: EVA-800 or EVA-850 emulator and evaluation boards

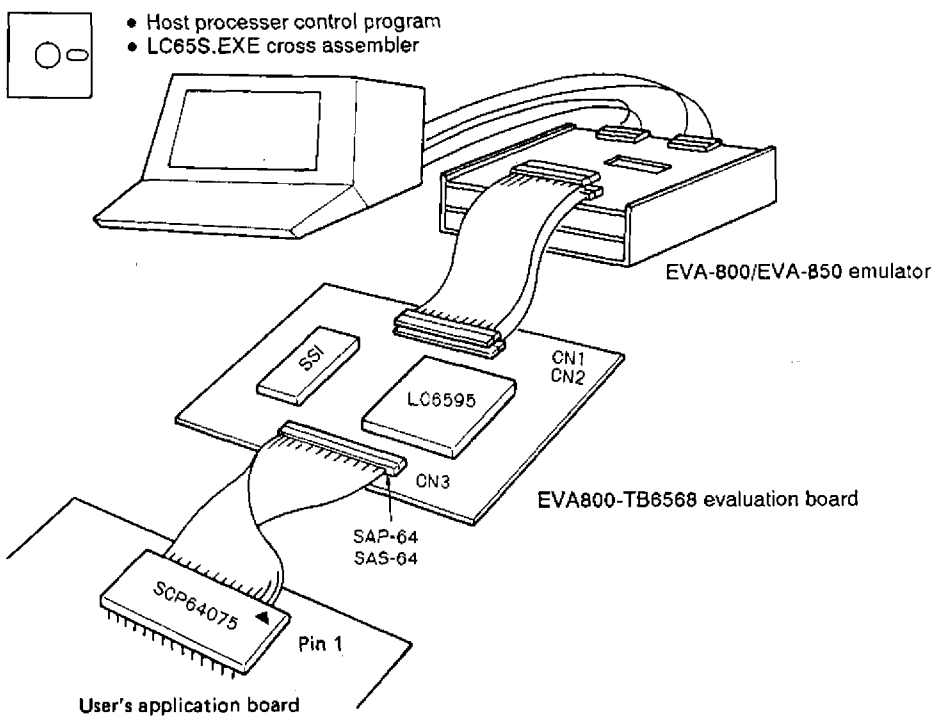


Fig. 1 Appearance of Development Support System

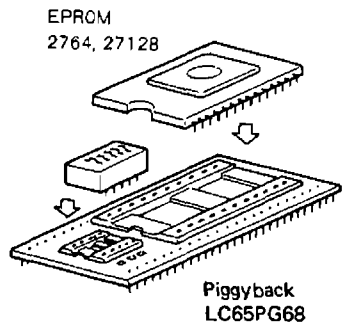
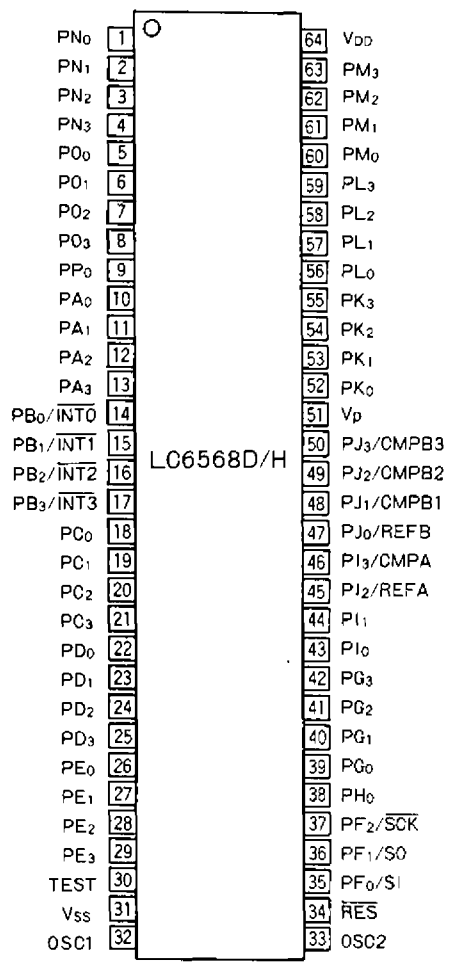
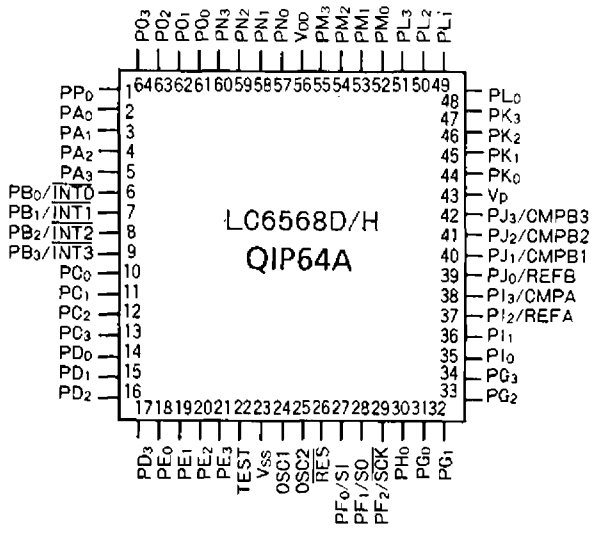


Fig. 2 Piggyback (For Program Evaluation)

(Note) MS-DOS is a registered trademark of Microsoft Corporation

Pin Assignment

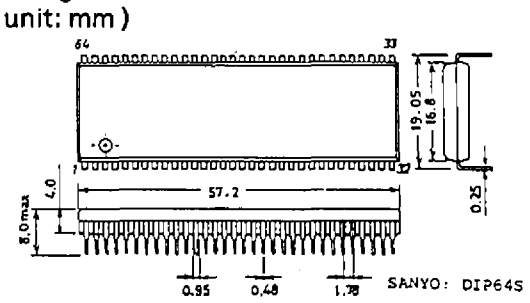




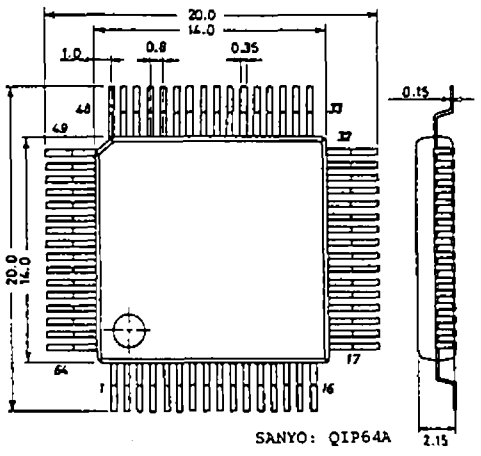
Note: When mounting the QIP version on the board, do not dip it in solder.

OSC1, OSC2	: C, R, or ceramic resonator oscillator for OSC	
PA0 to 3	: Port for input only	A0-3
PB0 to 3	: Port for input only	B0-3
PC0 to 3	: Input/output common port	C0-3
PD0 to 3	: Input/output common port	D0-3
PE0 to 3	: Input/output common port	E0-3
PF0 to 3	: Input/output common port	F0-3
PG0 to 3	: Input/output common port	G0-3
PH0	: Input/output common port	H0
PI0 to 3	: Input/output common port	I0-3
PJ0 to 3	: Input/output common port	J0-3
PK0 to 3	: Port for output only	K0-3
PL0 to 3	: Port for output only	L0-3
PM0 to 3	: Port for output only	M0-3
PN0 to 3	: Port for output only	N0-3
PO0 to 3	: Port for output only	O0-3
PP0	: Port for output only	P0
SI	: 4-bit/8-bit serial input port	
SO	: 4-bit/8-bit serial output port	
SCK	: Input/output for serial clock	
INT0 to 3	: Interrupt request input	
Vp	: Vp pin	
RES	: Reset	
TEST	: Test	
CMPA	: Comparator A input pin	
CMPB1 to 3	: Comparator B1 to 3 input pins	
REFA	: Comparator A reference voltage input pin	
REFB	: Comparator B reference voltage input pin	

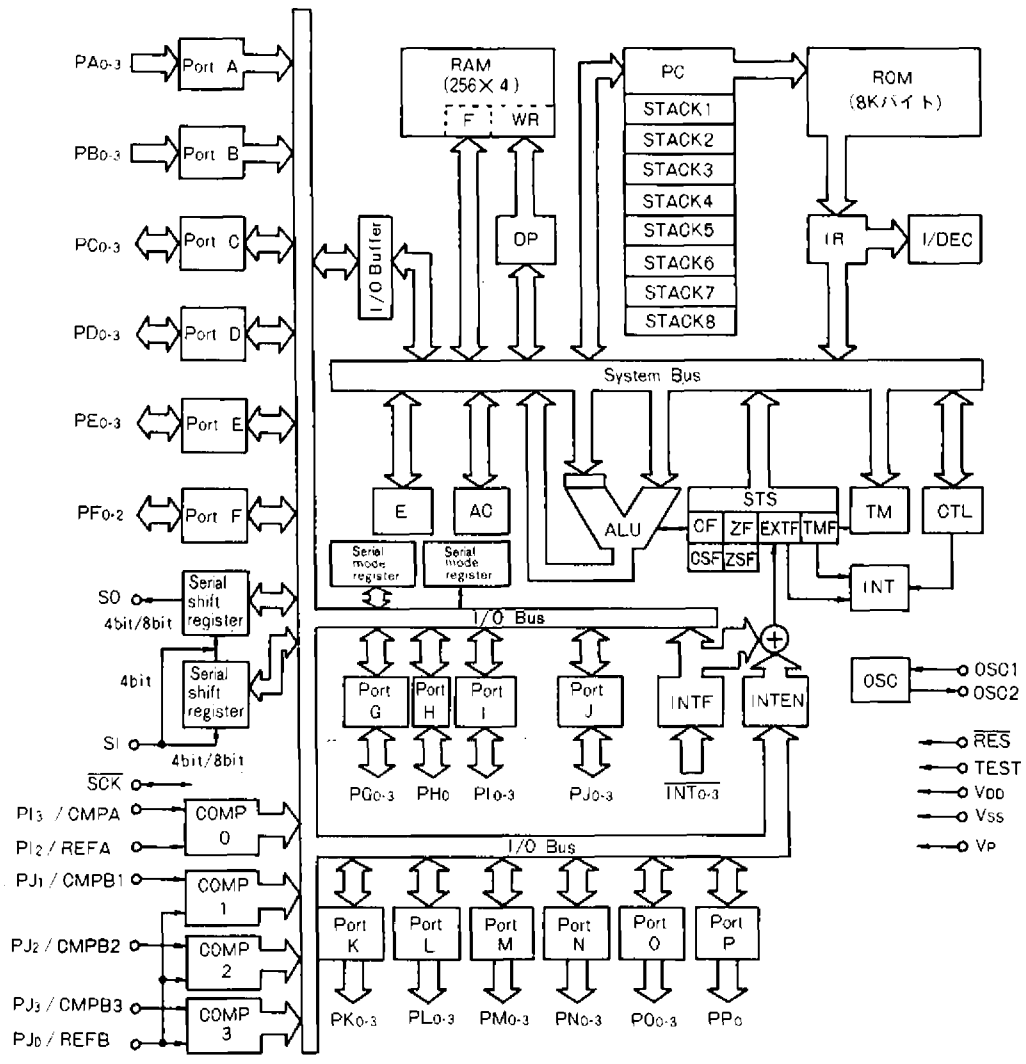
Package Dimensions 3071-D64IC
(unit: mm)



Package Dimensions 3057-Q64AIC
(unit: mm)



System Block Diagram



RAM	: Data memory	ROM	: Program memory
F	: Flag	PC	: Program counter
WR	: Working register	INT	: Interrupt control
AC	: Accumulator	IR	: Instruction register
ALU	: Arithmetic and logic unit	I.DEC	: Instruction decoder
DP	: Data pointer	CF, CSF	: Carry flag, carry save flag
E	: E register	ZF, ZSF	: Zero flag, zero save flag
CTL	: Control register	EXTF	: External interrupt request
OSC	: Oscillator	TMF	: Internal interrupt request
TM	: Timer	INTF	: Interrupt request flag
STS	: Status register	INTEN	: Interrupt enable flag

(Note) SI, SO, $\overline{SCK}$: Common to PF_0 to PF_2
$\overline{INT_0}$ to $\overline{INT_3}$: Common to PB_0 to PB_3
REFA, CMPA or PI_2, PI_3 port: Option-selectable
REFB, $CMPB_1$ to $CMPB_3$ or PJ_0 to PJ_3 port: Option-selectable

Pin Description

Pin Name	Pins	I/O	Functions	Options	During Reset
V_{DD} V_{SS}	1 1	–	Power supply	–	–
OSC1	1	Input	• Pin for externally connecting R, C or a ceramic resonator for system clock generation. • For the external clock mode, the OSC2 pin is open.	(1) External clock input (2) 2-pin RC OSC (3) 2-pin ceramic resonator OSC (4) Predivider option 1: No predivider 2: 1/3 predivider 3: 1/4 predivider	–
OSC2	1	Output			
PA_0 PA_1 PA_2 PA_3	4	Input	• Input port $A_{0 \text{ to } 3}$ (Low-threshold input) 4-bit input (IP instruction) Single-bit decision (BP, BNP instructions)	–	–
$PB_0/\overline{INT_0}$ $PB_1/\overline{INT_1}$ $PB_2/\overline{INT_2}$ $PB_3/\overline{INT_3}$	4	Input	• Input port $B_{0 \text{ to } 3}$ 4-bit input (IP instruction) Single-bit decision (BP, BNP instructions) • Standby is controlled by the PB_3. • The PB_3 pin must be free from chattering during the HALT instruction execution cycle. • $PB_{0 \text{ to } 3}$: Common with $\overline{INT}_{0 \text{ to } 3}$ Program-selectable (1 interrupt vector, 4 senses)	–	• Individual interrupt flag (INT0F to INT3F): Reset • Individual interrupt enable flag (INT0EN to INT3EN): Disable mode
PC_0 PC_1 PC_2 PC_3	4	Input/ Output	• Input/output common port $C_{0 \text{ to } 3}$. 4-bit input (IP instruction) 4-bit output (OP instruction) Single-bit decision (BP, BNP instructions) Single-bit set/reset (SPB, RPB instructions) • Output ("H" or "L") during reset may be specified by option.	(1) Open drain type output (2) With pull-up resistance (3) Output during reset: "H" (4) Output during reset: "L" • (1), (2): Specified bit by bit. • (3), (4): Specified in a group of 4 bits.	• "H" output • "L" output (Option-selectable)
PD_0 PD_1 PD_2 PD_3	4	Input/ Output	• Input/output common port $D_{0 \text{ to } 3}$. The functions, options are the same as for the $PC_{0 \text{ to } 3}$.	Same as for the $PC_{0 \text{ to } 3}$.	Same as for the $PC_{0 \text{ to } 3}$.
PE_0 PE_1 PE_2 PE_3	4	Input/ Output	• Input/output common port $E_{0 \text{ to } 3}$. 4-bit input (IP instruction) 4-bit output (OP instruction) Single-bit decision (BP, BNP instructions) Single-bit set/reset (SPB, RPB instructions) • PE0: With burst pulse (64Tcyc) output function	(1) Open drain type output (2) With pull-up resistance (1), (2): Specified bit by bit.	"H" output

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Pin Name	Pins	I/O	Functions	Options	During Reset
PF_0/SI PF_1/SO PF_2/$\overline{SCK}$	3	Input/ Output	• Input/output port F_0 to 2 The functions, options are the same as for the PE_0 to 3. However, no burst pulse output function is provided. • PF_0 to 2: Also used for serial interface. Program-selectable. SI: Serial input port SO: Serial output port $\overline{SCK}$: Serial clock input/output	Same as for the PE_0 to 3.	Sample as for the PE_0 to 3. Serial port: Disable
PG_0 PG_1 PG_2 PG_3	4	Input/ Output	• Input/output common port G_0 to 3. The functions, options are the same as for the PE_0 to 3. However, no burst pulse output function is provided.	Same as for the PE_0 to 3.	Same as for the PE_0 to 3.
PH_0	1	Input/ Output	• Input/output common port H_0. The functions, options are the same as for the PG_0 to 3. This port consists of a single bit.	Same as for the PG_0 to 3.	Same as for the PG_0 to 3.
PI_0 PI_1 PI_2/REFA PI_3/CMPA	4	Input/ Output	• Input/output common port I_0 to3. (Port input/output option selected mode) The functions, options are the same as for the PG_0 to 3.	Same as for the PG_0 to 3.	Same as for the PG_0 to 3.
	2	Input	• Comparator input option selected mode REFA: Comparator reference voltage input CMPA: Comparator input		
PJ_0/REFB PJ_1/CMPB1 PJ_2/CMPB$_2$ PJ_3/CMPB$_3$	4	Input/ Output	• Input/output common port J_0 to 3. (Port input/output option selected mode) The functions, options are the same as for the PG_0 to 3.	Same as for the PG_0 to 3.	Same as for the PG_0 to 3.
	4	Input	• Comparator input option selected mode REFB: Common reference voltage input for CMPB$_1$ to 3 CMPB$_1$ to 3: Comparator input • 4-bit input together with CMPA (BANK IP) • Single-bit decision (BANK BP, BNP) (at DPL = 9)		

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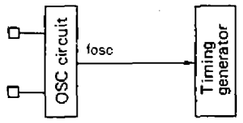
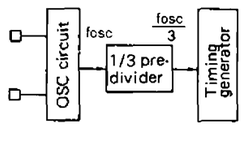
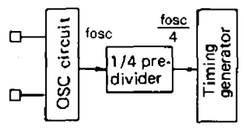
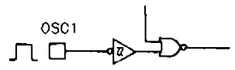
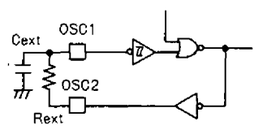
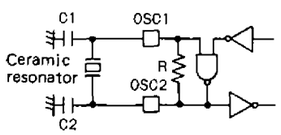
Pin Name	Pins	I/O	Functions	Options	During Reset
PK_0 PK_1 PK_2 PK_3	4	Output	• Output port K_0 to 3 (Segment driver output) • 4-bit output (OP instruction) • Single-bit decision (BP, BNP instructions) • Single-bit set/reset (SPB, RPB instructions)	(1) Open drain type output (2) With pull-down resistance • (1), (2): Specified bit by bit.	"L" output
PL_0 PL_1 PL_2 PL_3	4	Output	• Output port L_0 to 3 (Segment driver output) The functions, options are the same as for the PK_0 to 3.	Same as for the PK_0 to 3.	Same as for the PK_0 to 3.
PM_0 PM_1 PM_2 PM_3	4	Output	• Output port M_0 to 3 (Digit driver Output) The functions, options are the same as for the PK_0 to 3.	Same as for the PK_0 to 3.	Same as for the PK_0 to 3.
PN_0 PN_1 PN_2 PN_3	4	Output	• Output port N_0 to 3 (Digit driver output) The functions, options are the same as for the PK_0 to 3.	Same as for the PK_0 to 3.	Same as for the PK_0 to 3.
PO_0 PO_1 PO_2 PO_3	4	Output	• Output port O_0 to 3 (Digit driver output) The functions, options are the same as for the PK_0 to 3.	Same as for the PK_0 to 3.	Same as for the PK_0 to 3.
PP_0	1	Output	• Output port P_0 (Digit driver output) The functions, options are the same as for the PK_0 to 3. This port consists of a single bit.	Same as for the PK_0 to 3.	Same as for the PK_0 to 3.
$\overline{RES}$	1	Input	• System reset input • For power-up reset, "L" level is applied for 4 clock cycles or more.	—	—
TEST	1	Input	• LSI test pin Normally connected to V_{SS}	—	—
Vp	1	—	• Power supply pin for pull-down resistance	—	—

Predivider Option

Option Name	Circuit	Conditions, etc.
1. No predivider		• Applicable to all of 3 OSC options. • The OSC frequency, external clock do not exceed 1444 kHz. (LC6568D) • The OSC frequency, external clock do not exceed 4330 kHz. (LC6568H) • Refer to Table of OSC, Predivider Option (Table 2).
2. 1/3 predivider		• Applicable to only 2 options of external clock, ceramic resonator OSC. • The OSC frequency, external clock do not exceed 4330 kHz. • Refer to Table of OSC, Predivider Option (Table 2).
3. 1/4 predivider		• Applicable to only 2 options of external clock, ceramic resonator OSC. • The OSC frequency, external clock do not exceed 4330 kHz. • Refer to Table of OSC, Predivider Option (Table 2).

Oscillator Circuit Option

Option Name	Circuit	Conditions, etc.
1. External Clock		• Input: Schmitt type.
2. 2-pin RC OSC		• Input: Schmitt type.
3. Ceramic Resonator OSC		

(Note) High-speed version: Ceramic resonator OSC option or external clock option only

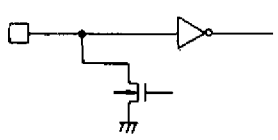
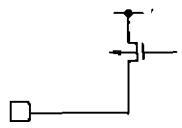
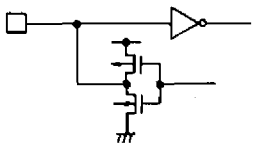
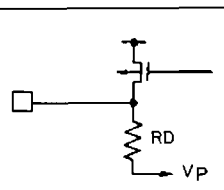
Options of Ports C, D Output Level during Reset

For input/output common ports C, D, either of the following two output levels may be selected in a group of 4 bits during reset by option.

Option Name	Conditions, etc.
1. Output during reset: "H" level	All of 4 bits of ports C, D
2. Output during reset: "L" level	All of 4 bits of ports C, D

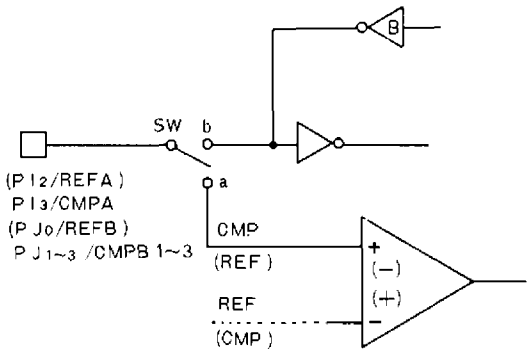
Options of Port Output Configuration

For each input/output common port, either of the following two output configurations may be selected by option (bitwise).

Option Name	Circuit	Applicable Ports
1. Open drain type output		Ports C, D, E, F, G, H, I, J
		Ports K, L, M, N, O, P
2. Output with pull-up resistance		Ports C, D, E, F, G, H, I, J (Note) Not applicable to PI_2/REFA, PI_3/CMPA, PJ_0/REFB, PJ_1 to 3/CMP1 to 3 ports at the comparator input function option selected mode
3. Output with pull-down resistance		Ports K, L, M, N, O, P

Port input/output
Comparator input } **Option**

- For six ports of PI_2/REFA, PI_3/CMPA, PJ_0/REFB, PJ_1/CMPB1, PJ_2/CMPB2, PJ_3/CMPB3, either of the two options – port input/output, comparator input – may be selected. (Note)
- Selection between port input/output and comparator input may be made in bit units.
  (a) Port input/output
  (b) Comparator input

Pin	Circuit Configuration	Conditions, etc.
PI_2/REFA PI_3/CMPA PJ_0/REFB PJ_1/CMPB1 PJ_2/CMPB2 PJ_3/CMPB3		Selection of (b) port input/output option permits either of the two port output type options (OD, PU) to be selected.

Option	SW
Port input/output option	b
Comparator input option	a

(Note) Selection of option for PI_3/CMPA provides automatic selection of option for PI_2/REFA.
Selection of option for PJ1/CMPB1, PJ_2/CMPB2, PJ_3/CMPB3 provides automatic selection of option for PJ_0/REFB.

LC6568D

1. Absolute Maximum Ratings/T_a = 25°C, V_{SS} = 0V

				min	typ	max	unit
Maxumum Supply Voltage	V_{DD} max		V_{DD}	−0.3		+7.0	V
Output Voltage	$V_{O(1)}$		OSC2	Allowable up to voltage generated			V
	$V_{O(2)}$		Port K, L, M, N, O, P0	V_{DD}−45		V_{DD}+0.3	V
Input Voltage	$V_{I(1)}$		OSC1 (Note 1) TEST, $\overline{RES}$	−0.3		V_{DD}+0.3	V
	$V_{I(2)}$		Port A, B	−0.3		+15	V
	$V_{I(3)}$		Vp	V_{DD}−45		V_{DD}+0.3	V
Input/Output Voltage	$V_{IO(1)}$		Port of OD type (Port C, D, E, F_0 to F_2, G, H_0, I, J)	−0.3		+15	V
	$V_{IO(2)}$		Port of PU type (Port C, D, E, F_0 to F_2, G, H_0, I, J)	−0.3		V_{DD}+0.3	V
Peak Output Current	$I_{OP(1)}$		Port C, D, E, F_0 to F_2, G, H_0, I, J	−2		+15	mA
	$I_{OP(2)}$		Port K, L	−10		0	mA
	$I_{OP(3)}$		Port M, N, O, P_0	−30		0	mA
Allowable Power Dissipation	P_d max	T_a = −30 to +70°C	DIP 64S			600	mW
			QIP 64			430	mW
Operating Temperature	Topr			−30		+70	°C
Storage Temperature	T_{stg}			−55		+125	°C
Average Output Current	$I_{OA(1)}$	Per pin over the period of 100msec.	Port C, D, E, F_0 to F_2, G, H_0, I, J	−2		+15	mA
	$I_{OA(2)}$	Per pin over the period of 100msec.	Port K, L	−10		0	mA
	$I_{OA(3)}$	Per pin over the period of 100msec.	Port M, N, O, P_0	−30		0	mA
	$\Sigma I_{OA(1)}$	Total current of PC_0 to 3, PD_0 to 3, PE_0 to 3 (Note 2)		−30		+50	mA
	$\Sigma I_{OA(2)}$	Total current of PF_0 to 2, PG_0 to 3, PH_0, PI_0 to 3, PJ_0 to 3 (Note 2)		−30		+50	mA
	$\Sigma I_{OA(3)}$	Total current of PK_0 to 3, PL_0 to 3, PM_0 to 3 (Note 2)		−50		0	mA
	$\Sigma I_{OA(4)}$	Total current of PN_0 to 3, PO_0 to 3, PP_0 (Note 2)		−50		0	mA

2. Allowable Operating Conditions/T_a = −30 to +70°C, V_{SS} = 0V, V_{DD} = 4.0 to 6.0V unless otherwise specified

				min	typ	max	unit
Operating Supply Voltage	V_{DD}		V_{DD}	4.0		6.0	V
Standby Supply Voltage	V_{ST}	RAM, register hold(Note 3)	V_{DD}	1.8		6.0	V
"H"-Level Input Voltage	$V_{IH(1)}$		Port A	1.9		+13.5	V
	$V_{IH(2)}$	Output Nch Tr OFF	Port of OD type (Port C to J)	0.7V_{DD}		+13.5	V
	$V_{IH(3)}$	Output Nch Tr OFF	Port of PU type (Port C to J)	0.7V_{DD}		V_{DD}	V
	$V_{IH(4)}$	Output Nch Tr OFF	$\overline{SCK}$, SI of OD type	0.8V_{DD}		+13.5	V

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					min	typ	max	unit
"H"-Level Input Voltage	$V_{IH(5)}$	Output Nch Tr OFF		$\overline{SCK}$, SI of PU type	$0.8V_{DD}$		V_{DD}	V
	$V_{IH(6)}$	Fig. 7		High Vt input circuit of Port B_3	$V_{DD}-0.5$		+13.5	V
	$V_{IH(7)}$	Fig. 7		Low Vt input circuit of Port B_3	$0.5V_{DD}$		+13.5	V
	$V_{IH(8)}$	Fig. 3	V_{DD}: 1.8 to 6.0V	$\overline{RES}$	$0.8V_{DD}$		V_{DD}	V
	$V_{IH(9)}$			PB_0 to 2, $\overline{INT_0}$ to 3	$0.8V_{DD}$		+13.5	V
	$V_{IH(10)}$	External clock mode		OSC1	$0.8V_{DD}$		V_{DD}	V
"L"-Level Input Voltage	$V_{IL(1)}$			PA_0 to 3	V_{SS}		+0.5	V
	$V_{IL(2)}$			PC to PJ, TEST	V_{SS}		$0.3V_{DD}$	V
	$V_{IL(3)}$			PB_0 to 2 $\overline{SCK}$, SI, $\overline{INT_0}$ to 3	V_{SS}		$0.25V_{DD}$	V
	$V_{IL(4)}$			$\overline{RES}$	V_{SS}		$0.25V_{DD}$	V
	$V_{IL(5)}$	Fig. 7		PB_3	V_{SS}		0.9	V
	$V_{IL(6)}$	Fig. 7	V_{DD}: 1.8 to 6.0V	PB_3	V_{SS}		0.3	V
	$V_{IL(7)}$	External clock mode		OSC1	V_{SS}		$0.25V_{DD}$	V
Operating Frequency (Cycle Time)	fop (T_{CYC})			OSC1 OSC2	384 (10.4)		1444 (2.77)	kHz (μS)
Ceramic Resonator Oscillation Constants				OSC1 OSC2	See Fig. 1, Table 1.			
External Clock Conditions								
Frequency	f_{EXT}			OSC1 (Fig. 4)	See Table 2.			
"H"-Level/"L"-Level Clock Pulse Width	t_{EXTH}/t_{EXTL}			OSC1 (Fig. 4)	90			ns
Rise/Fall Time	t_{EXTR}/t_{EXTF}			OSC1 (Fig. 4)			30	ns
2-pin RC Oscillation								
External Capacitance	C_{EXT}			OSC1, OSC2 (Fig. 9)	220±5%			pF
External Resistance	R_{EXT}			OSC1, OSC2 (Fig. 9)	6.8±1%			kΩ

3. Electrical Characteristics/T_a = –30 to +70°C, V_{SS} = 0V, V_{DD} = 4.0 to 6.0V unless otherwise specified

				min	typ	max	unit
"H"-Level Input Current	$I_{IH(1)}$	Output Nch Tr OFF (Including OFF leakage current of Nch Tr) V_{IN}=+13.5V	Port of OD type (Port C to J) Port A, B			+5.0	μA
	$I_{IH(2)}$	Output Nch Tr OFF (Including OFF leakage current of Nch Tr) $V_{IN}=V_{DD}$	Port of PU type (Port C to J) OSC1 (External clock mode)			+1.0	μA
"L"-Level Input Current	$I_{IL(1)}$	Output Nch Tr OFF $V_{IN}=V_{SS}$	Port of OD type (Port C to J) Port A, B OSC1 (External clock mode)	–1.0			μA
	$I_{IL(2)}$	Output Nch Tr OFF $V_{IN}=V_{SS}$	Port of PU type (Port C to J)	–1.3	–0.35		mA
	$I_{IL(3)}$	$V_{IN}=V_{SS}$	$\overline{RES}$	–45	–10		μA
"H"-Level Output Voltage	$V_{OH(1)}$	I_{OH}=–50μA	Port of PU type (Port C to J)	$V_{DD}-1.2$			V
	$V_{OH(2)}$	I_{OH}=–3mA	Port K, L	$V_{DD}-1.8$			V
	$V_{OH(3)}$	I_{OH}=–15mA	Port M, N, O, P_0	$V_{DD}-1.8$			V

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				min	typ	max	unit
"L"-Level Output Voltage	$V_{OL(1)}$	I_{OL}=10mA, Other ports: ΣI_{OL}max	Port C, D, E, F_0 to F_2, G, H_0, I, J			1.5	V
	$V_{OL(2)}$	I_{OL}=2mA, Each port: I_{OL}=2mA	Port C, D, E, F_0 to F_2, G, H_0, I, J			0.5	V
	$V_{OL(3)}$	Vp=−35V, Output Pch Tr OFF Output open	Port of PD type (Port K to P)			−33	V
Output OFF Leakage Current	$I_{OFF(1)}$	Output Pch Tr OFF $V_{OUT}=V_{DD}$	Port of OD type (Port K to P)			+30	μA
	$I_{OFF(2)}$	Output Pch Tr OFF $V_{OUT}=V_{DD}$−40V	Port of OD type (Port K to P)	−30			μA
Hysteresis Voltage	V_{HYS}		$\overline{RES}$, $\overline{INT_0}$ to $\overline{3}$ $\overline{SCK}$, SI, OSC1 of Schmitt type (Note 5)		0.1V_{DD}		V
Pull-up Resistance	R_{PP}	V_{DD}: 5.0V	Port of PU type (Port C to J)		14		kΩ
Pull-down Resistance	R_{PD}	V_{DD}: 5.0V	Port of PD type (Port K to P)	50		200	kΩ
Current Dissipation	Operation mode, Output Nch Tr, Pch Tr OFF, $V_{IN}=V_{DD}$						
2-Pin RC Oscillation Mode	$I_{DDOP(1)}$	Fig. 9 f_{osc}=750kHz (typ)	V_{DD}		2.5	8	mA
Ceramic Resonator Oscillation Mode	$I_{DDOP(2)}$	Fig. 1 4MHz, 1/3 predivider	V_{DD}		8	15	mA
	$I_{DDOP(3)}$	Fig. 1 4MHz, 1/4 predivider	V_{DD}		8	15	mA
	$I_{DDOP(4)}$	Fig. 1 3MHz, 1/3 predivider	V_{DD}		6.5	14	mA
	$I_{DDOP(5)}$	Fig. 1 3MHz, 1/4 predivider	V_{DD}		6.5	14	mA
	$I_{DDOP(6)}$	Fig. 1 400kHz	V_{DD}		1.0	4.5	mA
	$I_{DDOP(7)}$	Fig. 1 800kHz	V_{DD}		2.0	6	mA
External Clock Mode	$I_{DDOP(8)}$	384kHz to 1444kHz, 1/1 predivider	V_{DD}		3.5	9	mA
		1152kHz to 4330kHz, 1/3 predivider	V_{DD}		8	15	mA
		1536kHz to 4330kHz, 1/4 predivider	V_{DD}		8	15	mA
Standby Mode	I_{DDST}	$V_{IN}=V_{DD}$ Output Nch Tr OFF Output Pch Tr OFF Output pin open			0.05	10	μA
Ceramic Resonator Oscillation							
Oscillation Frequency	f_{CFOSC} (Note 4)	1/1 (10μs) 400K	OSC1, OS2 (Fig. 1)	392	400	408	kHz
		1/1 (5μs) 800K	OSC1, OSC2 (Fig. 1)	784	800	816	kHz
		1/3 (4μs) 3M 1/4 (5.33μs)	OSC1, OSC2 (Fig. 1)	2.94	3	3.06	MHz
		1/3 (3μs) 4M 1/4 (4μs)	OSC1, OSC2 (Fig. 1)	3.92	4	4.08	MHz
Oscillation Stabilizing Period	t_{CFS}					10	ms
RC Oscillation							
Oscillation Frequency	f_{CRS}	1/1 predivider Cext=220pF±5% Rext=6.8kΩ±1%	OSC1, OSC2 (Fig. 9)	554	750	1235	kHz
Pin Capacitance	CP	f=1MHz Other than pins to be tested: $V_{IN}=V_{SS}$			10		pF

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4. Serial Interface Characteristics/V_{SS} =0V, T_a =−30°C to +70°C, V_{DD} =4.0V to 6.0V unless otherwise sepcified

				min	typ	max	unit
Serial Clock							
Input Clock Cycle Time	$t_{CKCY(1)}$	Fig. 5	$\overline{SCK}$	3.0			μs
Output Clock Cycle Time	$t_{CKCY(2)}$	Fig. 5	$\overline{SCK}$		64 x T_{CYC}		μs
Input Clock "L"-Level Pulse Width	$t_{CKL(1)}$	Fig. 5	$\overline{SCK}$	1.0			μs
Output Clock "L"-Level Pulse Width	$t_{CKL(2)}$	Fig. 5	$\overline{SCK}$		32 x T_{CYC}		μs
Input Clock "H"-Level Pulse Width	$t_{CKH(1)}$	Fig. 5	$\overline{SCK}$	1.0			μs
Output Clock "H"-Level Pulse Width	$t_{CKH(2)}$	Fig. 5	$\overline{SCK}$		32 x T_{CYC}		μs
Serial Input							
Data Setup Time	t_{ICK}	Specified for ↑ of $\overline{SCK}$, Fig. 5	SI	0.5			μs
Data Hold Time	t_{CKI}	Specified for ↑ of $\overline{SCK}$, Fig. 5	SI	0.5			μs
Serial Output							
Output Delay Time	t_{CKO}	Specified for ↓ of $\overline{SCK}$, Nch OD only: External 1kohm, external 50pF Fig. 5	SO			0.5	μs
Pulse Output							
Period	t_{PCY}	Fig. 6	PE0		64 x T_{CYC}		μs
"H"-Level Pulse Width	t_{PH}	T_{CYC}=4 x System clock period, Nch OD only: External 1kohm, external 50pF	PE0		32 x T_{CYC}±10%		μs
"L"-Level Pulse Width	t_{PL}		PE0		32 x T_{CYC}±10%		μs

5. Comparator Characteristics/V_{SS} =0V, T_a =−30°C to +70°C, V_{DD} =4.5V to 6.0V unless otherwise specified

				min	typ	max	unit
Comparator Characteristics							
Input Voltage Range	V_{CMIN}		PI3, PJ1 to 3	V_{SS}+1.0		V_{DD}−1.5	V
Response Speed	T_{RS}	100mV overdrive mode				50	μs
Offset Voltage	V_{OFS}	V_{CMIN}=V_{SS}+1.0V to V_{DD}−1.5V			±20	±100	mV

(Note 1) When oscillated internally under the oscillating conditions in Fig. 1, up to the oscillation amplitude generated is allowable.
(Note 2) Average over the period of 100msec.
(Note 3) Operating supply voltage V_{DD} must be held until the standby mode is entered after the execution of the HALT instruction.
The PB_3 pin must be free from chattering during the HALT instruction execution cycle.
(Note 4) f_{CFOSC} represents an oscillatable frequency.
(Note 5) The OSC1 becomes the Schmitt type when the OSC option is the 2-pin RC OSC or external clock OSC.
(Note 6) When mounting the QIP version on the board, do not dip it in solder.

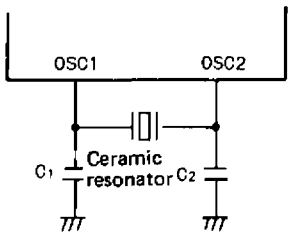


Fig. 1 Ceramic Resonator Oscillation Circuit

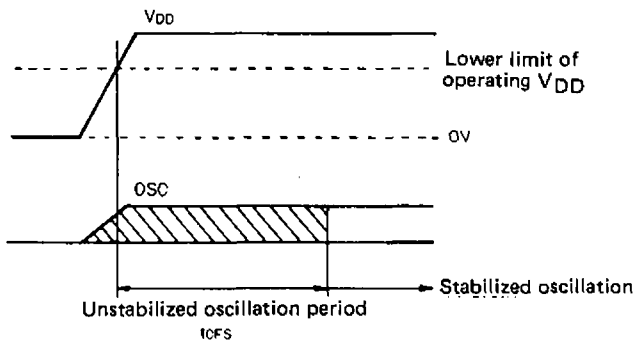
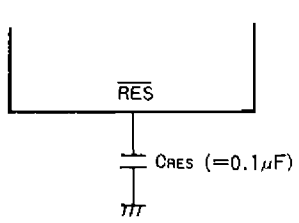


Fig. 2 Oscillation Stabilizing Period

Table 1 Constants Guaranteed for LC6568D Ceramic Resonator Oscillation

4 MHz (Murata) CSA4.00MG	C1	33pF ± 10%
	C2	33pF ± 10%
4 MHz (Kyocera) KBR4.0MS	C1	33pF ± 10%
	C2	33pF ± 10%
3 MHz (Murata) CSA3.00MG	C1	33pF ± 10%
	C2	33pF ± 10%
3 MHz (Kyocera) KBR3.0MS	C1	33pF ± 10%
	C2	33pF ± 10%

800 kHz (Murata) CSB800D CSB800K	C1	220pF ± 10%
	C2	220pF ± 10%
800 kHz (Kyocera) KBR800H	C1	220pF ± 10%
	C2	220pF ± 10%
400 kHz (Murata) CSB400P	C1	330pF ± 10%
	C2	330pF ± 10%
400 kHz (Kyocera) KBR400B	C1	330pF ± 10%
	C2	330pF ± 10%



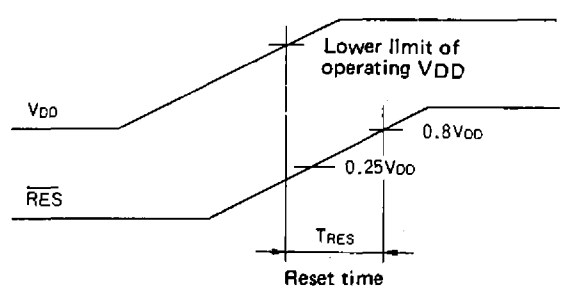


Fig. 3 Reset Circuit and Reset Time

(Note 7) When the rise time of the power supply is 0, the reset time becomes 10ms to 100ms at C_{RES}=0.1μF. If the rise time of the power supply is long, the value of C_{RES} must be increased so that the reset time becomes 10ms or greater.

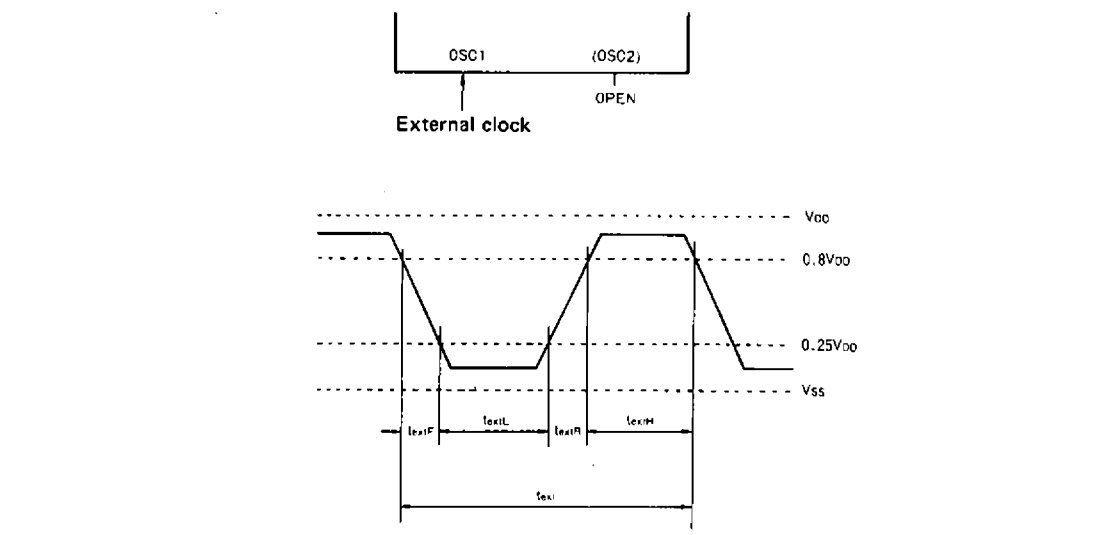


Fig. 1 External Clock Input Waveform

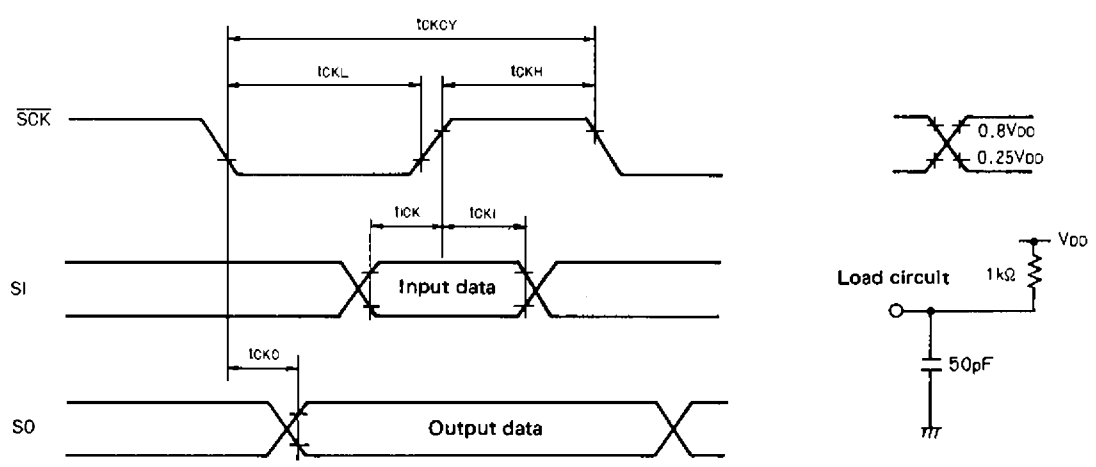
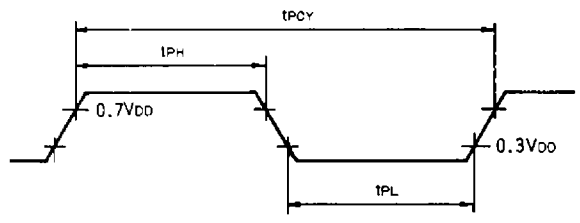


Fig. 5 Serial Input/Output Timing



The load conditions are the same as in Fig. 5.

Fig. 6 Pulse Output Timing at Port E_0

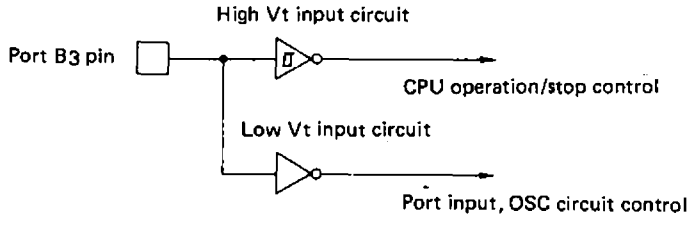


Fig. 7 Port B_3 High Vt/Low Vt Input Circuit

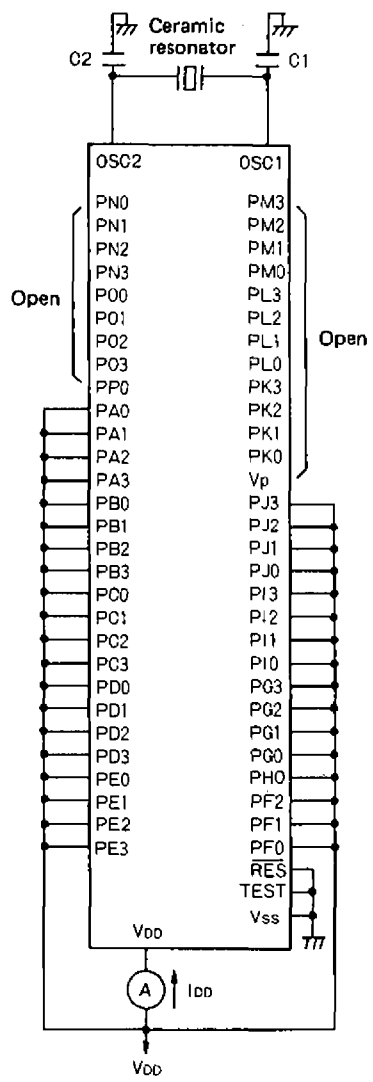


Fig. 8 I_{DDOP} Test Circuit (f=4MHz)

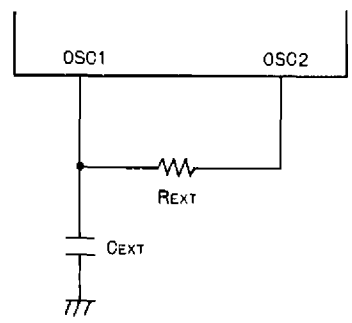


Fig. 9 RC Oscillation Circuit

Table 2 LC6568D

Table of Oscillation, Predivider Option (All selectable combinations are shown. Do not use any other combinations than shown below.) V_{DD} = 4 to 6V

Circuit Configuration	Frequency	Predivider Option (Cycle Time)	Remarks
Ceramic Resonator Option	400 kHz	1/1 (10 μs)	Unusable with 1/3, 1/4 predivider
	800 kHz	1/1 (5 μs)	Unusable with 1/3, 1/4 predivider
	3 MHz	1/3 (4 μs) 1/4 (5.33 μs)	Unusable with 1/1 predivider
	4 MHz	1/3 (3 μs) 1/4 (4 μs)	Unusable with 1/1 predivider
External Clock Option or External Clock Drive by RC OSC Option	384 to 1444 kHz 1152 to 4330 kHz 1536 to 4330 kHz	1/1 (10.4 to 2.77 μs) 1/3 (10.4 to 2.77 μs) 1/4 (10.4 to 3.70 μs)	
External Clock Drive by Ceramic Resonator OSC Option	The external clock drive is impossible. When using the external clock drive, specify the external clock option or CR OSC option.		
RC OSC Option	Used with 1/1 predivider, recommended constants. If used with other than recommended constants, the predivider option, frequency, V_{DD} range must be the same as for the external clock option.		

RC Oscillation Characteristic of the LC6568D

Fig. 10 shows the RC oscillation characteristic of the LC6568D. For the variation range of RC OSC frequency of the LC6568D, the following are guaranteed at the external constants only shown below.

External constants Cext = 220pF, Rext = 6.8kohms

$554\text{kHz} \leqq f_{CRS} \leqq 1235\text{kHz}$ ($T_a = -30°C$ to $+70°C$, V_{DD} = 4.0 to 6.0V)

If any other constants than specified above are used, the range of Rext = 4kohms to 20kohms, Cext = 150pF to 390pF must be observed. (See Fig. 10.)

(Note 8) The oscillation frequency at V_{DD} = 5.0V, $T_a = 25°C$ must not exceed 750kHz.
(Note 9) The oscillation frequency at V_{DD} = 4 to 6V, $T_a = -30$ to $+70°C$ must be within the operation clock frequency range (384kHz to 1444kHz).

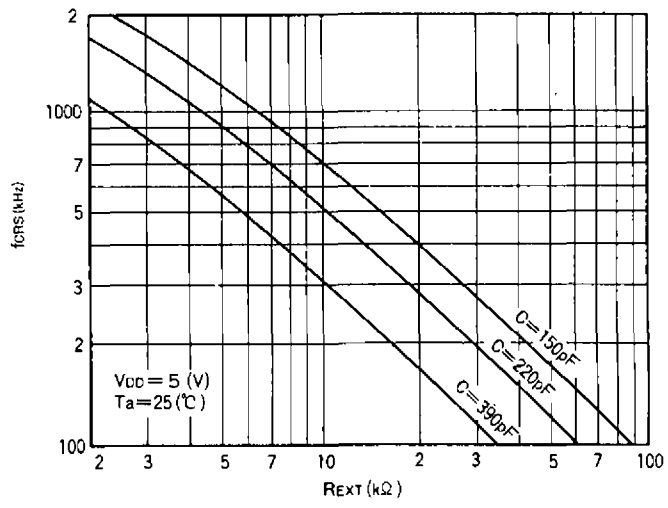


Fig. 10 RC Oscillation Frequency Data (Typ.)

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1. Absolute Maximum Ratings/T_a = 25°C, V_{SS} = 0V

				min	typ	max	unit
Maxumum Supply Voltage	V_{DD} max		V_{DD}	−0.3		+7.0	V
Output Voltage	$V_{O(1)}$		OSC2	Allowable up to voltage generated			V
	$V_{O(2)}$		Port K, L, M, N, O, P0	V_{DD}−45		V_{DD}+0.3	V
Input Voltage	$V_{I(1)}$		OSC1 (Note 1) TEST, $\overline{RES}$	−0.3		V_{DD}+0.3	V
	$V_{I(2)}$		Port A, B	−0.3		+15	V
	$V_{I(3)}$		Vp	V_{DD}−45		V_{DD}+0.3	V
Input/Output Voltage	$V_{IO(1)}$		Port of OD type (Port C, D, E, F_0 to F_2, G, H_0, I, J)	−0.3		+15	V
	$V_{IO(2)}$		Port of PU type (Port C, D, E, F_0 to F_2, G, H_0, I, J)	−0.3		V_{DD}+0.3	V
Peak Output Current	$I_{OP(1)}$		Port C, D, E, F_0 to F_2, G, H_0, I, J)	−2		+15	mA
	$I_{OP(2)}$		Port K, L	−10		0	mA
	$I_{OP(3)}$		Port M, N, O, P_0	−30		0	mA
Allowable Power Dissipation	P_d max	T_a = −30 to +70°C	DIP64S			600	mW
			QIP 64			430	mW
Operating Temperature	Topr			−30		+70	°C
Storage Temperature	T_{stg}			−55		+125	°C
Average Output Current	$I_{OA(1)}$	Per pin over the period of 100msec.	Port C, D, E, F_0 to F_2, G, H_0, I, J)	−2		+15	mA
	$I_{OA(2)}$	Per pin over the period of 100msec.	Port K, L	−10		0	mA
	$I_{OA(3)}$	Per pin over the period of 100msec.	Port M, N, O, P_0	−30		0	mA
	$\Sigma I_{OA(1)}$	Total current of PC_0 to 3, PD_0 to 3, PE_0 to 3 (Note 2)		−30		+50	mA
	$\Sigma I_{OA(2)}$	Total current of PF_0 to 2, PG_0 to 3, PH_0, PI_0 to 3, PJ_0 to 3 (Note 2)		−30		+50	mA
	$\Sigma I_{OA(3)}$	Total current of PK_0 to 3, PL_0 to 3, PM_0 to 3 (Note 2)		−50		0	mA
	$\Sigma I_{OA(4)}$	Total current of PN_0 to 3, PO_0 to 3, PP_0 (Note 2)		−50		0	mA

2. Allowable Operating Conditions/T_a = −30 to +70°C, V_{SS} = 0V, V_{DD} = 4.5 to 6.0V unless otherwise specified

				min	typ	max	unit
Operating Supply Voltage	V_{DD}		V_{DD}	4.5		6.0	V
Standby Supply Voltage	V_{ST}	RAM, register hold(Note 3)	V_{DD}	1.8		6.0	V
"H"-Level Input Voltage	$V_{IH(1)}$		Port A	1.9		+13.5	V
	$V_{IH(2)}$	Output Nch Tr OFF	Port of OD type (Port C to J)	0.7V_{DD}		+13.5	V
	$V_{IH(3)}$	Output Nch Tr OFF	Port of PU type (Port C to J)	0.7V_{DD}		V_{DD}	V

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				min	typ	max	unit
	$V_{IH(4)}$	Output Nch Tr OFF	$\overline{SCK}$, SI of OD type	$0.8V_{DD}$		+13.5	V
	$V_{IH(5)}$	Output Nch Tr OFF	$\overline{SCK}$, SI of PU type	$0.8V_{DD}$		V_{DD}	V
	$V_{IH(6)}$	Fig. 7	High Vt input circuit of PB_3	$V_{DD}-0.5$		+13.5	V
	$V_{IH(7)}$	Fig. 7	Low Vt input circuit of PB_3	$0.5V_{DD}$		+13.5	V
	$V_{IH(8)}$	Fig. 3 V_{DD}: 1.8 to 6.0V	$\overline{RES}$	$0.8V_{DD}$		V_{DD}	V
	$V_{IH(9)}$		PB_0 to 2, $\overline{INT_0}$ to 3	$0.8V_{DD}$		+13.5	V
	$V_{IH(10)}$	External clock mode	OSC1	$0.8V_{DD}$		V_{DD}	V
"L"-Level Input Voltage	$V_{IL(1)}$		PA_0 to 3	V_{SS}		+0.5	V
	$V_{IL(2)}$		PCto PJ TEST	V_{SS}		$0.3V_{DD}$	V
	$V_{IL(3)}$		PB_0 to 2 $\overline{SCK}$, SI' $\overline{INT_0}$ to 3	V_{SS}		$0.25V_{DD}$	V
	$V_{IL(4)}$		$\overline{RES}$	V_{SS}		$0.25V_{DD}$	V
	$V_{IL(5)}$	Fig. 7	PB_3	V_{SS}		0.9	V
	$V_{IL(6)}$	Fig. 7 V_{DD}: 1.8 to 6.0V	PB_3	V_{SS}		0.3	V
	$V_{IL(7)}$	External clock mode	OSC1	V_{SS}		$0.25V_{DD}$	V
Operating Frequency (Cycle Time)	fop (T_{CYC})		OSC1 OSC2	384 (10.4)		4330 (0.92)	kHz (μS)
Ceramic Resonator Oscillation Constants			OSC1 OSC2	See Fig. 1, Table 1.			
External Clock Conditions							
Frequency	f_{EXT}	1/1 predivider	OSC1 (Fig. 4)	See Table 2.			
"H"-Level/"L"-Level Clock Pulse Width	t_{EXH}, t_{EXTL}		OSC1 (Fig. 4)	90			ns
Rise/Fall Time	t_{EXTR}, t_{EXTF}		OSC1 (Fig. 4)			30	ns

3. Electrical Characteristics/T_a = −30 to +70°C, V_{SS} = 0V, V_{DD} = 4.5 to 6.0V unless otherwise specified

				min	typ	max	unit
"H"-Level Input Current	$I_{IH(1)}$	Output Nch Tr OFF (Including OFF leakage current of Nch Tr) V_{IN}=+13.5V	Port of OD type (Port C to J) Port A, B			+5.0	μA
	$I_{IH(2)}$	Output Nch Tr OFF (Including OFF leakage current of Nch Tr) $V_{IN}=V_{DD}$	Port of PU type (Port C to J) OSC1 (External clock mode)			+1.0	μA
"L"-Level Input Current	$I_{IL(1)}$	Output Nch Tr OFF $V_{IN}=V_{SS}$	Port of OD type (Port C to J) Port A, B OSC1 (External clock mode)	−1.0			μA
	$I_{IL(2)}$	Output Nch Tr OFF $V_{IN}=V_{SS}$	Port of PU type (Port C to J)	−1.3	−0.35		mA
	$I_{IL(3)}$	$V_{IN}=V_{SS}$	$\overline{RES}$	−45	−10		μA
"H"-Level Output Voltage	$V_{OH(1)}$	I_{OH}=−50μA	Port of PU type (Port C to J)	$V_{DD}-1.2$			V
	$V_{OH(2)}$	I_{OH}=−3mA	Port K, L	$V_{DD}-1.8$			V
	$V_{OH(3)}$	I_{OH}=−15mA	Port M, N, O, P_0	$V_{DD}-1.8$			V

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				min	typ	max	unit
"L"-Level Output Voltage	$V_{OL(1)}$	I_{OL}=10mA, Other ports: ΣI_{OL}max	Port C, D, E, F_0 to F_2 G, H_0, I, J)			1.5	V
	$V_{OL(2)}$	I_{OL}=2mA, Each port: I_{OL}=2mA	Port C, D, E, F_0 to F_2, G, H_0, I, J)			0.5	V
	$V_{OL(3)}$	Vp=–35V, Output Pch Tr OFF Output open	Port of PD type (Port K to P)			–33	V
Output OFF Leakage Current	$I_{OFF(1)}$	Output Pch Tr OFF $V_{OUT}=V_{DD}$	Port of OD type (Port K to P)			+30	μA
	$I_{OFF(2)}$	Output Pch Tr OFF $V_{OUT}=V_{DD}$–40V	Port of OD type (Port K to P)	–30			μA
Hysteresis Voltage	V_{HYS}		$\overline{RES}$, $\overline{INT_0}$ to 3, $\overline{SCK}$, SI, OSC1 of Schmitt type (Note 5)		0.1V_{DD}		V
Pull-up Resistance	R_{PP}	V_{DD}: 5.0V	Port of PU type (Port C to J)		14		kΩ
Pull-down Resistance	R_{PD}	V_{DD}: 5.0V	Port of PD type (Port K to P)	50		200	kΩ
Current Dissipation	Operation mode, Output Nch Tr, Pch Tr OFF, $V_{IN}=V_{DD}$						
	$I_{DDOP(1)}$	4MHz OSC (Fig. 8)	V_{DD}		8	15	mA
	$I_{DDOP(2)}$	External Clock mode 384kHz to 4330kHz	V_{DD}		8	15	mA
	I_{DDST}	Standby mode Output Nch, Pch Tr OFF Output pin open $V_{IN}=V_{DD}$	V_{DD}		0.05	10	μA
Ceramic Resonator Oscillation							
Oscillation Frequency	f_{CFOSC} (Note 4)	1/1 (1μs) 4MHz	OSC1 OSC2 (Fig. 1)	3.92	4.00	4.08	MHz
Oscillation Stabilizing Period	t_{CFS}	Fig. 2				10	ms
Pin Capacitance	CP	f=1MHz Other than pins to be tested: $V_{IN}=V_{SS}$			10		pF

4. Serial Interface Characteristics/V_{SS} =0V, T_a = –30°C to +70°C, V_{DD} = 4.5V to 6.0V unless otherwise specified

				min	typ	max	unit
Serial Clock							
Input Clock Cycle Time	$t_{CKCY(1)}$	Fig. 5	$\overline{SCK}$	3.0			μs
Output Clock Cycle Time	$t_{CKCY(2)}$	Fig. 5	$\overline{SCK}$		64 x T_{CYC}		μs
Input Clock "L"-Level Pulse Width	$t_{CKL(1)}$	Fig. 5	$\overline{SCK}$	1.0			μs
Output Clock "L"-Level Pulse Width	$t_{CKL(2)}$	Fig. 5	$\overline{SCK}$		32 x T_{CYC}		μs
Input Clock "H"-Level Pulse Width	$t_{CKH(1)}$	Fig. 5	$\overline{SCK}$	1.0			μs
Output Clock "H"-Level Pulse Width	$t_{CKH(2)}$	Fig. 5	$\overline{SCK}$		32 x T_{CYC}		μs

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LC6568H				min	typ	max	unit
Serial Input							
Data Setup Time	t_{ICK}	Specified for ↑ of $\overline{SCK}$, Fig. 5	SI	0.5			μs
Data Hold Time	t_{CKI}	Specified for ↑ of $\overline{SCK}$, Fig. 5	SI	0.5			μs
Serial Output							
Output Delay Time	t_{CKO}	Specified for ↓ of $\overline{SCK}$, Nch OD only: External 1kohm, external 50pF Fig. 5	SO			0.5	μs
Pulse Output							
Period	t_{PCY}	Fig. 6 T_{CYC}=4 x System clock period, Nch OD only: External 1kohm, external 50pF	PE0	64 x T_{CYC}			μs
"H"-Level Pulse Width	t_{PH}		PE0	32 x T_{CYC}±10%			μs
"L"-Level Pulse Width	t_{PL}		PE0	32 x T_{CYC}±10%			μs

5. Comparator Characterisitcs/V_{SS} =0V, T_a =−30°C to +70°C V_{DD} =4.5V to 6.0V unless otherwise specified

				min	typ	max	unit
Comparator Characteristics							
Input Voltage Range	V_{CMIN}		PI3, PJ1 to 3	V_{SS}+1.0		V_{DD}−1.5	V
Response Speed	T_{RS}	100mV overdrive mode				50	μs
Offset Voltage	V_{OFS}	V_{CMIN}=V_{SS}+1.0V to V_{DD}−1.5V			±20	±100	mV

(Note 1) When oscillated internally under the oscillating conditions in Fig. 1, up to the oscillation amplitude generated is allowable.
(Note 2) Average over the period of 100msec.
(Note 3) Operating supply voltage V_{DD} must be held until the standby mode is entered after the execution of the HALT instruction.
The PB_3 pin must be free from chattering during the HALT instruction execution cycle.
(Note 4) f_{CFOSC} represents an oscillatable frequency.
(Note 5) The OSC1 becomes the Schmitt type when the OSC option is the 2-pin RC OSC or external clock OSC.
(Note 6) When mounting the QIP version on the board, do not dip it in solder.

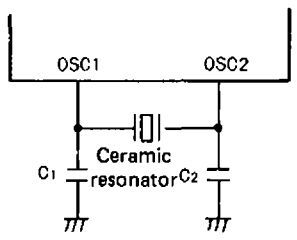


Fig. 1 Ceramic Resonator Oscillation Circuit

Table 1 Constants Guaranteed for LC6568H Ceramic Resonator Oscillation

4 MHz (Murata) CSA4.00MG	C1	33pF ± 10%
	C2	33pF ± 10%
4 MHz (Kyocera) KBR4.0MS	C1	33pF ± 10%
	C2	33pF ± 10%
3 MHz (Murata) CSA3.00MG	C1	33pF ± 10%
	C2	33pF ± 10%
3 MHz (Kyocera) KBR3.0MS	C1	33pF ± 10%
	C2	33pF ± 10%

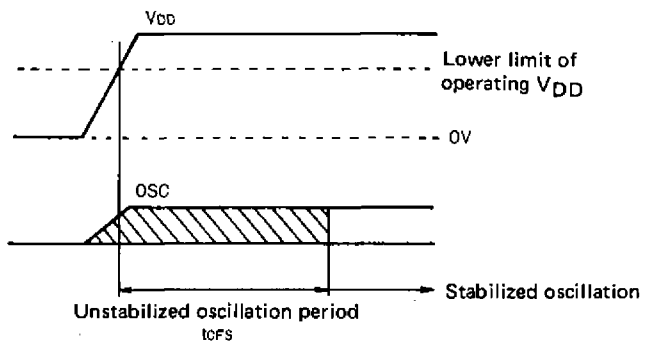


Fig. 2 Oscillation Stabilizing Period

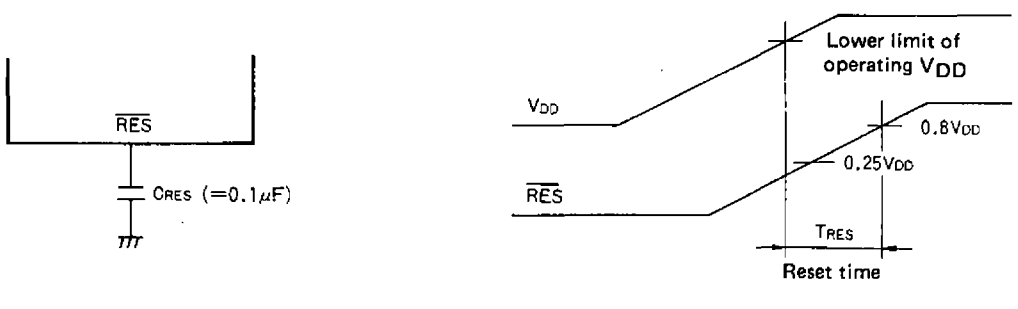
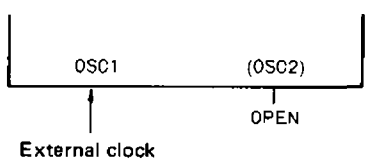


Fig. 3 Reset Circuit and Reset Time

(Note 7) When the rise time of the power supply is 0, the reset time becomes 10ms to 100ms at C_{RES} = 0.1μF. If the rise time of the power supply is long, the value of C_{RES} must be increased so that the reset time becomes 10ms or greater.



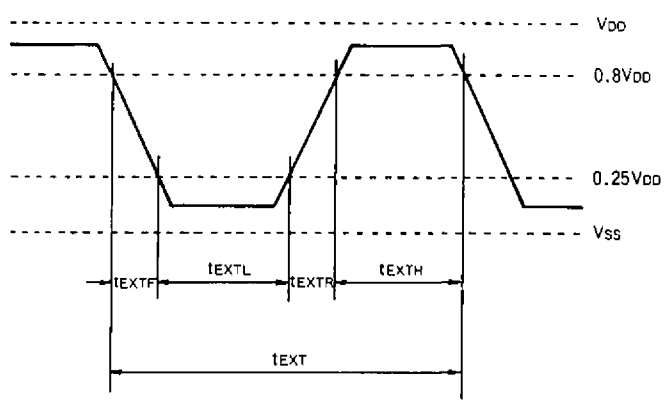


Fig. 4 External Clock Input Waveform

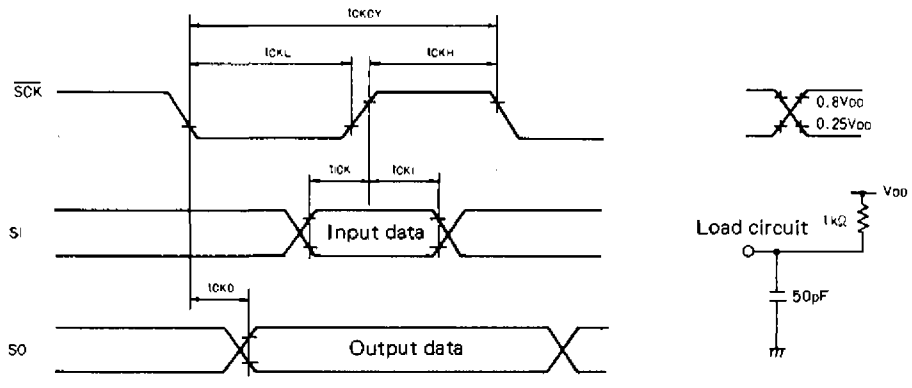
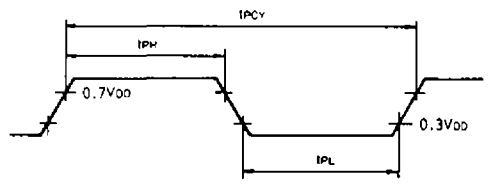


Fig. 5 Serial Input/Output Timing



The load conditions are the same as in Fig. 5.

Fig. 6 Pulse Output Timing at Port E_0

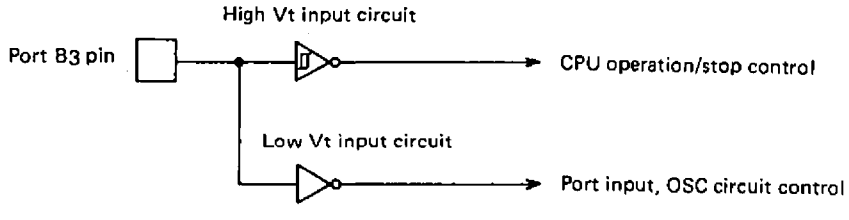


Fig. 7 Port B_3 High Vt/Low Vt Input Circuit

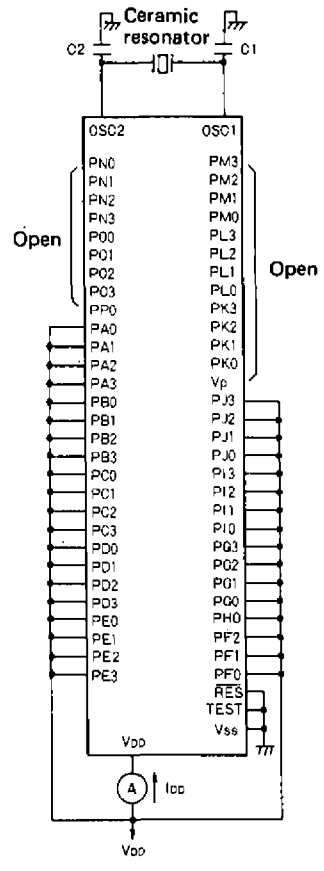


Fig. 8 I_{DDOP} Test Circuit (f =4MHz)

Table 2 LC6568H

Table of Oscillation, Predivider Option (All selectable combinations are shown. Do not use any other combinations than shown below.) V_{DD} = 4.5 to 6V

Circuit Configuration	Frequency	Predivider Option (Cycle Time)	Remarks
Ceramic Resonator OSC Option	4 MHz	1/1 (1 μs)	
External Clock Option	384 to 4330 kHz	1/1 (10.4 to 0.92 μs)	
External Clock Drive by Ceramic Resonator OSC Option	The external clock drive is impossible. When using the external clock drive, specify the external clock option.		

Notes for Program Evaluation

- When evaluating the LC6568D/H with the evaluation chip (LC6595, LC65PG68), the following must be observed.

Classi-fication	Item	Function	
		Mass-production chip	Evaluation chip
Notes for option	OSC divider	3 selections (1/1, 1/3, 1/4) by option (Note) For H version, 1/1 divider only is available.	3 selections (1/1, 1/3, 1/4) available by 2 pins of DIV pin, 3OR4 pin. DIV pin, 3OR4 pin must be set according to option specified for mass-production chip.
	Ports C, D output level at reset mode	Ports C, D can be brought to "H" or "L" in a group of 4 bits.	Port C and Port D can be brought to "H" and "L" by CHL pin and DHL pin respectively. CHL pin and DHL pin must be set according to option specified for mass-production chip.
	Port output configuration PU/OD	PU or OD can be selected bitwise.	Only Nch OD without PU. [Evaluation chip-applied evaluation] External resistor (10kohms) on evaluation board must be connected to necessary port. [Simulation chip-applied evaluation] Resistor must be connected to necessary port on application board.
	PU resistor configuration	PU resistor brought to Hi-Z at "L" output mode (Pch Tr is turned OFF).	PU resistor, being external resistor, whose impedance remains unchanged at "L" output mode. For mass-production chip, leakage current only flows in Pch Tr at "L" output mode; for evaluation chip, current continues flowing in PU resistor at "L" output mode.
	Port output configuration PD/OD	PD or OD can be selected bitwise.	Only Pch OD without PD. [Evaluation chip-applied evaluation] External resistor (100kohms) on evaluation board must be connected to necessary port. [Simulation chip-applied evaluation] Resistor must be connected to necessary port on application board. In this case, load power source must be also supplied on application board.
	Port function, port input/output or comparator input	If the input instruction (IP, BP) is executed with port input/output or comparator input function not option-selected, "0" is input from the port bits not specified as port input/output or comparator input.	The input pins with options not selected are in floating state. That is, the data input from such pins are indeterminate. If the input instruction (IP, BP, BNP) for these input pins, unpredictable data is input from them. Do not use any input instruction for such input pins.
Notes for OSC	OSC constants —1	[2-pin RC OSC] Catalog-guaranteed constants in catalog.	[2-pin RC OSC] Different from mass-production chip in circuit design and characteristic. Frequency must be adjusted to OSC frequency of mass-production chip by adjusting variable resistor.
		[2-pin ceramic resonator OSC] Catalog-guaranteed constants provide OSC at frequency specified in catalog.	[2-pin ceramic resonator OSC] Different from mass-production chip in circuit design and characteristic. Wiring capacitance may provide unstable OSC. External constants must be fine-adjusted according to service conditions.

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Classi-fication	Item	Function	
		Mass-production chip	Evaluation chip
Notes for OSC	OSC constants −2	[2-pin ceramic resonator OSC] Feedback resistor is contained.	[2-pin ceramic resonator OSC] No feedback resistor is contained. Feedback resistor of 1 Mohm must be connected externally.
Notes for electrical characteristics	OSC frequency	OSC frequency characteristic as indicated in catalog.	Different from mass-production chip in circuit design, and characteristic. ES, CS must be used to evaluate characteristic in detail.
	Operating current, standby current	Current characteristic as indicated in catalog.	Different from mass-production chip in cirucit design, characteristic. The standby current cannot be evaluated in detail. However, the standby current can be confirmed roughly in the manner discussed later. Be sure to confirm the standby current. ES, CS must be used to evaluate characteristic in detail.
	Operating voltage	Supply voltage range as indicated in catalog.	Evaluation chip must be also used at V_{DD}=5V±5% at which EPROM, other LSI are used. Therefore, V_{DD}=5V±5% only can be used for evaluation of mass-production microcomputers.
	Operating temper-ature	Temperature range as indicated in catalog.	Evaluation chip and simulation chip must be used at 10°C to 40°C for evaluation.
Notes for I/O port circuit configuration	Port A	Input-only port	Port A is an input/output common port. Do not use the output instructions (OP, SPB, RPB). When performing evaluation, do not fail to turn OFF the pull-up resistance option switch for port A on the evaluation chip board.
	Port F3	The PF3 is not available. Even when the output instruction (OP, SPB, RPB) is executed, no operation is performed.	The PF3 exists. However, do not use the output instruction (OP, SPB, RPB) for this pin. When the output instruction is executed and "0" is output to the pin, the interrupt circuit is affected.
		When the IP instruction is executed "0" is always input to AC from pin PF3.	When the IP instruction is executed, "1" is always input to AC from pin PF3. However, "0" is input if "0" has been output to pin PF3 by the OP instruction.

The EVA800-TB6568 board and LC65PG68 incorporates an LC6568 evaluation IC and a gate array.
Actual performance may differ from evaluation performance because of the gate array which is used to emulate interrupts and control bidirectional port, PH_0.

1. Operation

The gate array can go out of sync with the LC6586D/H due to slight variations in the reset rise time. If this occurs, the LC6568 evaluation IC will not accept interrupts or PH_0 port instructions for several ms after program startup.
When running programs, always ensure that interrupts or PH_0 port instructions are processed correctly.

2. Characteristics

When output driver options have been selected, ports PB_{0to3} and PH_0 have a breakdown voltage of 15V in the case of volume fabrication devices. In the LC6568 evaluation IC, however, these ports have a withstanding voltage equal to V_{DD}. Take care that test circuit designs do not exceed this limit.

<Confirmation methods for the standby function>

The standby current at the standby mode of the simulation chip can be evaluated not exactly but approximately. Then, do the following steps.

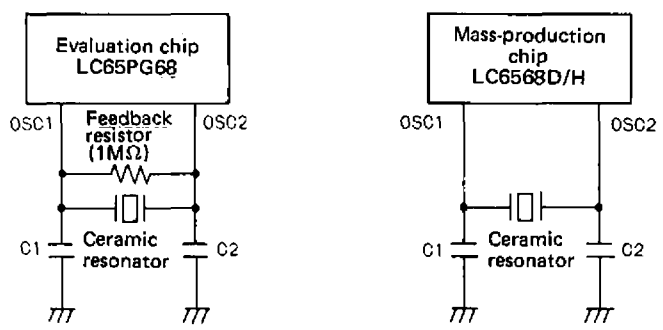
(a) Confirmation of the standby state
Be sure to confirm whether or not the LSI enters the standby mode when the standby conditions are satisfied.
(i) When the OSC1 and OSC2 oscillation option is selected, confirm on an oscilloscope that the oscillation stops in the standby mode.
(ii) Confirmation by the current dissipation
Remove the EPROM when confirming whether or not the LSI enters the standby mode. The I_{DD} of the LSI can determine whether or not the LSI is now in the standby mode.
When the LSI is in the operating mode, more than some 100μA current is transmitted. When in the standby mode, the current of the I_{DD} is 150μA or less if the DIV, 3OR4, CHL, DHL are all set to "H" (excluding the load current). If the DIV, 3OR4, CHL, DHL, ———, etc. are all set to "L", the current of the I_{DD} is approximately 20μA.

(b) Confirmation by the load current
Your program must be designed so that the current is not transmitted to the input/output ports prior to the execution of the HALT instruction. This can reduce the useless dissipation of the load current at the standby mode and be confirmed on an oscilloscope.
(i) Design your program so that the current is not transmitted to the output ports prior to the execution of the HALT instruction.
(ii) Design your program and peripherals so that the input ports and input/output ports are not brought to the floating state at the standby mode.
If brought to the floating state, current flows in the microcomputer input circuit section, causing more current dissipation. Therefore, the backup enable time is shortened extremely in applications where the capacitor backup is used. (For the evaluation chip, there is appreciable current because the option circuit section to select the port input/output or comparator input is partly in the floating state.)

Ceramic resonator oscillation constants when the EVA800-TB6568 is used

When developing your program using the eva-chip board EVA800-TB6568, adjust the capacitor value according to the stray capacitance of the circuit because the ceramic resonator oscillation constants depend on the conditions for evaluation and the cable length, etc.

Note) When the evaluation chip is used in the 2-pin ceramic resonator oscillation mode, no feedback resistor is contained unlike the mass-production chip.
Connect a feedback resistor of 1Mohm externally as shown below.
Since constants R, C are also differ from those for the mass-production chip, adjust the capacitor value according to the stray capacitance of the circuit.



2-pin Ceramic Resonator Oscillation Circuit for Evaluation Chip and Mass-production Chip

LC6568 INSTRUCTION SET

Symbol	Description				
AC	: Accumulator	M(DP)	: Memory addressed by DP	( ), [ ]	: Contents
ACt	: Accumulator bit t	P(DP_L)	: Input/output port addressed by DP_L	←	: Transfer and direction
CF	: Carry flag	PC	: Program counter	+	: Addition
CTL	: Control register	STACK	: Stack register	−	: Subtraction
DP	: Data pointer	TM	: Timer	∧	: AND
E	: E register	TMF	: Timer (internal) interrupt request flag	∨	: OR
EXTF	: External interrupt request flag	At, Ha, La	: Working register	∀	: Exclusive OR
Fn	: Flag bit n	ZF	: Zero flag		
M	: Memory	P($\overline{DP_L}$)	: Pseudo input/output port specified by DP_L		

Instruction group	Mnemonic		Instruction code $D_7D_6D_5D_4$	Instruction code $D_3D_2D_1D_0$	Bytes	Cycles	Function	Description	Status flag affected	Remarks
Accumulator manipulation instructions	CLA	Clear AC	1 1 0 0	0 0 0 0	1	1	AC ← 0	The AC contents are cleared.	ZF	* 1
	CLC	Clear CF	1 1 1 0	0 0 0 1	1	1	CF ← 0	The CF contents are cleared.	CF	
	STC	Set CF	1 1 1 1	0 0 0 1	1	1	CF ← 1	The CF is set.	CF	
	CMA	Complement AC	1 1 1 0	1 0 1 1	1	1	AC ← $\overline{(AC)}$	The AC contents are complemented.	ZF	
	INC	Increment AC	0 0 0 0	1 1 1 0	1	1	AC ← (AC) + 1	The AC contents are incremented +1.	ZF CF	
	DEC	Decrement AC	0 0 0 0	1 1 1 1	1	1	AC ← (AC) − 1	The AC contents are decremented −1.	ZF CF	
	RAL	Rotate AC left through CF	0 0 0 0	0 0 0 1	1	1	AC_0 ← (CF), AC_{n+1} ← (AC_n), CF ← (AC_3)	The AC contents are shifted left through the CF.	ZF CF	
	TAE	Transfer AC to E	0 0 0 0	0 0 1 1	1	1	E ← (AC)	The AC contents are transferred to the E.		
	XAE	Exchange AC with E	0 0 0 0	1 1 0 1	1	1	(AC) ⇆ (E)	The AC contents and the E conents are exchanged.		
Memory manipulation instructions	INM	Increment M	0 0 1 0	1 1 1 0	1	1	M(DP) ← [M(DP)] + 1	The M(DP) contents are incremented +1.	ZF CF	
	DEM	Decrement M	0 0 1 0	1 1 1 1	1	1	M(DP) ← [M(DP)] − 1	The M(DP) contents are decremented −1.	ZF CF	
	SMB bit	Set M data bit	0 0 0 0	1 0 B_1B_0	1	1	M(DP, B_1B_0) ← 1	A single bit of the M(DP) specified with B_1B_0 is set.		
	RMB bit	Reset M data bit	0 0 1 0	1 0 B_1B_0	1	1	M(DP, B_1B_0) ← 0	A single bit of the M(DP) specified with B_1B_0 is reset.	ZF	
Arithmetic operation/comparison instructions	AD	Add M to AC	0 1 1 0	0 0 0 0	1	1	AC ← (AC) + (M(DP))	Binary addition of the AC contents and the M(DP) contents is performed and the result is stored in the AC.	ZF CF	
	ADC	Add M to AC with CF	0 0 1 0	0 0 0 0	1	1	AC ← (AC) + (M(DP)) + (CF)	Binary addition of the AC, CF contents and the M(DP) contents is performed and the result is stored in the AC.	ZF CF	
	DAA	Decimal adjust AC in addition	1 1 1 0	0 1 1 0	1	1	AC ← (AC) + 6	6 is added to the AC contents.	ZF	
	DAS	Decimal adjust AC in subtraction	1 1 1 0	1 0 1 0	1	1	AC ← (AC) + 10	10 is added to the AC contents.	ZF	
	EXL	Exclusive or M to AC	1 1 1 1	0 1 0 1	1	1	AC ← (AC) ∀ (M(DP))	The AC contents and the M(DP) contents are exclusive-ORed and the result is stored in the AC.	ZF	
	AND	And M to AC	1 1 1 0	0 1 1 1	1	1	AC ← (AC) ∧ (M(DP))	The AC contents and the M(DP) contents are ANDed and the result is stored in the AC.	ZF	
	OR	Or M to AC	1 1 1 0	0 1 0 1	1	1	AC ← (AC) ∨ (M(DP))	The AC contents and the M(DP) contents are ORed and the result is stored in the AC.	ZF	
	CM	Compare AC with M	1 1 1 1	1 0 1 1	1	1	$\overline{(M(DP))}$ + (AC) + 1	The AC contents and the M(DP) contents are compared and the CF and ZF are set/reset. (Comparison result: (M(DP)) > (AC): CF 0, ZF 0; (M(DP)) = (AC): CF 1, ZF 1; (M(DP)) < (AC): CF 1, ZF 0)	ZF CF	
	CI data	Compare AC with immediate data	0 0 1 0 0 1 0 0	1 1 0 0 $I_3I_2I_1I_0$	2	2	$\overline{I_3I_2I_1I_0}$ + (AC) + 1	The AC contents and the immediate data $I_3I_2I_1I_0$ are compared and the ZF and CF are set/reset. (Comparison result: $I_3I_2I_1I_0$ > (AC): CF 0, ZF 0; $I_3I_2I_1I_0$ = (AC): CF 1, ZF 1; $I_3I_2I_1I_0$ < (AC): CF 1, ZF 0)	ZF CF	
	CLI data	Compare DP_L with immediate data	0 0 1 0 0 1 0 1	1 1 0 0 $I_3I_2I_1I_0$	2	2	(DP_L) ∀ $I_3I_2I_1I_0$	The DP_L contents and the immediate data $I_3I_2I_1I_0$ are compared.	ZF	
Load/store instructions	LI data	Load AC with immediate data	1 1 0 0	$I_3I_2I_1I_0$	1	1	AC ← $I_3I_2I_1I_0$	The immediate data $I_3I_2I_1I_0$ is loaded in the AC.	ZF	* 1
	S	Store AC to M	0 0 0 0	0 0 1 0	1	1	M(DP) ← (AC)	The AC contents are stored in the M(DP).		
	L	Load AC from M	0 0 1 0	0 0 0 1	1	1	AC ← (M(DP))	The M(DP) contents are loaded in the AC.	ZF	
	XM data	Exchange AC with M, then modify DP_H with immediate data	1 0 1 0	0 $M_2M_1M_0$	1	2	(AC) ⇆ (M(DP)) DP_H ← (DP_H) ∀ 0 $M_2M_1M_0$	The AC contents and the M(DP) contents are exchanged and then the DP_H contents are modified with the contents of (DP_H) ∀ 0$M_2M_1M_0$.	ZF	The ZF is set/reset according to the result of (DP_H) ∀ 0$M_2M_1M_0$.
	X	Exchange AC with M	1 0 1 0	0 0 0 0	1	2	(AC) ⇆ (M(DP))	The AC contents and the M(DP) contents are exchanged.	ZF	The ZF is set/reset according to the DP_H contents at the time of instruction execution.
	XI	Exchange AC with M, then increment DP_L	1 1 1 1	1 1 1 0	1	2	(AC) ⇆ (M(DP)) DP_L ← (DP_L) + 1	The AC contents and the M(DP) contents are exchanged and then the DP_L contents are incremented +1.	ZF	The ZF is set/reset according to the result of (DP_L + 1).
	XD	Exchange AC with M, then decrement DP_L	1 1 1 1	1 1 1 1	1	2	(AC) ⇆ (M(DP)) DP_L ← (DP_L) − 1	The AC contents and the M(DP) contents are exchanged and then the DP_L contents are decremented −1.	ZF	The ZF is set/reset according to the result of (DP_L − 1).
	RTBL	Read table data from program ROM	0 1 1 0	0 0 1 1	1	2	AC, E ← ROM (PCh, E, AC)	The contents of ROM addressed by the PC whose low-order 8 bits are replaced with the E and AC contents are loaded in the AC and E.		

Instruction group	Mnemonic		Instruction code		Bytes	Cycles	Function	Description	Status flag affected	Remarks
			$O_7 D_6 D_5 D_4$	$D_3 D_2 D_1 D_0$						
Data pointer manipulation instructions	LDZ data	Load DP_H with Zero and DP_L with immediate data respectively	1 0 0 0	$I_3 I_2 I_1 I_0$	1	1	$DP_H \leftarrow 0$ $DP_L \leftarrow I_3 I_2 I_1 I_0$	The DP_H and DP_L are loaded with 0 and the immediate data $I_3 I_2 I_1 I_0$ respectively.		
	LHI data	Load DP_H with immediate data	0 1 0 0	$I_3 I_2 I_1 I_0$	1	1	$DP_H \leftarrow I_3 I_2 I_1 I_0$	The DP_H is loaded with the immediate data $I_3 I_2 I_1 I_0$.		
	IND	Increment DP_L	1 1 1 0	1 1 1 0	1	1	$DP_L \leftarrow (DP_L) + 1$	The DP_L contents are incremented +1.	ZF	
	DED	Decrement DP_L	1 1 1 0	1 1 1 1	1	1	$DP_L \leftarrow (DP_L) - 1$	The DP_L contents are decremented −1.	ZF	
	TAL	Transfer AC to DP_L	1 1 1 1	0 1 1 1	1	1	$DP_L \leftarrow (AC)$	The AC contents are transferred to the DP_L		
	TLA	Transfer DP_L to AC	1 1 1 0	1 0 0 1	1	1	$AC \leftarrow (DP_L)$	The DP_L contents are transferred to the AC	ZF	
	XAH	Exchange AC with DP_H	0 0 1 0	0 0 1 1	1	1	$(AC) \rightleftarrows (DP_H)$	The AC contents and the DP_H contents are exchanged.		
Working register manipulation instructions	XAt XA0 XA1 XA2 XA3	Exchange AC with working register At		$t_1 t_0$ 0 0 0 0 0 1 0 0 1 0 0 0 1 1 0 0	1 1 1 1 1	1 1 1 1 1	$(AC) \rightleftarrows (A0)$ $(AC) \rightleftarrows (A1)$ $(AC) \rightleftarrows (A2)$ $(AC) \rightleftarrows (A3)$	The AC contents and the contents of working register At are exchanged. At is assigned one of A_0, A_1, A_2, A_3 according to $t_1 t_0$.		
	XHa XH0 XH1	Exchange DP_H with working register Ha	1 1 1 1 1 1 1 1	a 1 0 0 0 1 1 0 0	1 1	1 1	$(DP_H) \rightleftarrows (H0)$ $(DP_H) \rightleftarrows (H1)$	The DP_H contents and the contents of working register Ha are exchanged. Ha is assigned either of H0 or H1 according to a.		
	XLa XL0 XL1	Exchange DP_L with working register La	1 1 1 1 1 1 1 1	a 0 0 0 0 0 1 0 0	1 1	1 1	$(DP_L) \rightleftarrows (L0)$ $(DP_L) \rightleftarrows (L1)$	The DP_L contents and the contents of working register La are exchanged. La is assigned either of L0 or L1 according to a.		
Flag manipulation instructions	SFB flag	Set flag bit	0 1 0 1	$B_3 B_2 B_1 B_0$	1	1	$Fn \leftarrow 1$	The flag specified with $B_3 B_2 B_1 B_0$ is set.		
	RFB flag	Reset flag bit	0 0 0 1	$B_3 B_2 B_1 B_0$	1	1	$Fn \leftarrow 0$	The flag specified with $B_3 B_2 B_1 B_0$ is reset.	ZF	The flags are divided into 4 groups of F_0 to F_3, F_4 to F_7, F_8 to F_{11}, F_{12} to F_{15}. The ZF is set/reset according to the 4 bits including a single bit specified with the immediate data $B_3 B_2 B_1 B_0$
Jump/subroutine instructions	JMP addr	Jump in the current bank	0 1 1 0 $P_7 P_6 P_5 P_4$	1 $P_{10} P_9 P_8$ $P_3 P_2 P_1 P_0$	2	2	$PC \leftarrow PC_{11}$ (or $\overline{PC_{11}}$) $P_{10} P_9 P_8 P_7 P_6 P_5$ $P_4 P_3 P_2 P_1 P_0$	A jump to the address specified with the PC_{12} PC_{11} (or PC_{11}) and immediate data $P_{10} P_9 P_8 P_7 P_6 P_5$ $P_4 P_3 P_2 P_1 P_0$ occurs.		If the BANK and SB instructions are executed consecutively, the bank is changed.
	JPEA	Jump in the current page modified by E and AC	1 1 1 1	1 0 1 0	1	1	$PC_{7 \sim 0} \leftarrow (E, AC)$	A jump to the address specified with the contents of the PC whose low-order 8 bits are replaced by the E and AC contents occurs.		
	CZP addr	Call subroutine in the zero page	1 0 1 1	$P_3 P_2 P_1 P_0$	1	1	$STACK \leftarrow (PC) + 1$ $PC_{11 \sim 6}, PC_{1 \sim 0} \leftarrow 0$ $PC_{5 \sim 2} \leftarrow P_3 P_2 P_1 P_0$	A subroutine in page 0 of bank 0 is called.		
	CAL addr	Call subroutine in the zero bank	1 0 1 0 $P_7 P_6 P_5 P_4$	1 $P_{10} P_9 P_8$ $P_3 P_2 P_1 P_0$	2	2	$STACK \leftarrow (PC) + 2$ $PC_{11 \sim 0} \leftarrow 0 P_{10} P_9 P_8 P_7$ $P_6 P_5 P_4 P_3 P_2 P_1 P_0$	A subroutine in bank 0 is called.		
	RT	Return from subroutine	0 1 1 0	0 0 1 0	1	1	$PC \leftarrow (STACK)$	A return from a subroutine occurs.		
	RTI	Return from interrupt routine	0 0 1 0	0 0 1 0	1	1	$PC \leftarrow (STACK)$ $CF\ ZF \leftarrow CSF, ZSF$	A return from an interrupt service routine occurs.	ZF CF	
	BANK	Change bank	1 1 1 1	1 1 0 1	1	1	$PC_{11} \leftarrow (\overline{PC_{11}})$	The bank is changed. (Effective only when immediately followed by the JMP instruction) The pseudo I/O port is specified. (Effective when immediately followed by the IP, OP, SPB, RPB, BP, BNP instruction)		
	SB	Set bank	0 1 1 0	0 1 I_1 I_0	1	1	PC_{12} $PC_{11} \leftarrow I_1, I_0$	The bank is changed. Effective only when used immediately before the JMP instruction.		
Branch instructions	BAt addr	Branch on AC bit	0 1 1 1 $P_7 P_6 P_5 P_4$	0 0 $t_1 t_0$ $P_3 P_2 P_1 P_0$	2	2	$PC_{7 \sim 0} \leftarrow P_7 P_6 P_5 P_4$ $P_3 P_2 P_1 P_0$ if $ACt = 1$	If a single bit of the AC specified with the immediate data $t_1 t_0$ is 1, a branch to the address specified with the immediate data $P_7 P_6 P_5 P_4 P_3 P_2 P_1 P_0$ within the same page occurs.		Mnemonic is BA0 to BA3 according to the value of t.
	BNAt addr	Branch on no AC bit	0 0 1 1 $P_7 P_6 P_5 P_4$	0 0 $t_1 t_0$ $P_3 P_2 P_1 P_0$	2	2	$PC_{7 \sim 0} \leftarrow P_7 P_6 P_5 P_4$ $P_3 P_2 P_1 P_0$ if $ACt = 0$	If a single bit of the AC specified with the immediate data $t_1 t_0$ is 0, a branch to the address specified with the immediate data $P_7 P_6 P_5 P_4 P_3 P_2 P_1 P_0$ within the same page occurs.		Mnemonic is BNA0 to BNA3 according to the value of t.
	BMt addr	Branch on M bit	0 1 1 1 $P_7 P_6 P_5 P_4$	0 1 $t_1 t_0$ $P_3 P_2 P_1 P_0$	2	2	$PC_{7 \sim 0} \leftarrow P_7 P_6 P_5 P_4$ $P_3 P_2 P_1 P_0$ if $(M(DP).t_1 t_0) = 1$	If a single bit of the M(DP) specified with the immediate data $t_1 t_0$ is 1, a branch to the address specified with the immediate data $P_7 P_6 P_5 P_4 P_3 P_2 P_1 P_0$ within the same page occurs.		Mnemonic is BM0 to BM3 according to the value of t.
	BNMt addr	Branch on no M bit	0 0 1 1 $P_7 P_6 P_5 P_4$	0 1 $t_1 t_0$ $P_3 P_2 P_1 P_0$	2	2	$PC_{7 \sim 0} \leftarrow P_7 P_6 P_5 P_4$ $P_3 P_2 P_1 P_0$ if $(M(DP).t_1 t_0) = 0$	If a single bit of the M(DP) specified with the immediate data $t_1 t_0$ is 0, a branch to the address specified with the immediate data $P_7 P_6 P_5 P_4 P_3 P_2 P_1 P_0$ within the same page occurs.		Mnemonic is BNM0 to BNM3 according to the value of t.
	BPt addr	Branch on Port bit	0 1 1 1 $P_7 P_6 P_5 P_4$	1 0 $t_1 t_0$ $P_3 P_2 P_1 P_0$	2	2	$PC_{7 \sim 0} \leftarrow P_7 P_6 P_5 P_4$ $P_3 P_2 P_1 P_0$ if $(P(DP_L).t_1 t_0) = 1$	If a single bit of port $P(DP_L)$ specified with the immediate data $t_1 t_0$ is 1, a branch to the address specified with the immediate data $P_7 P_6 P_5 P_4 P_3 P_2 P_1 P_0$ within the same page occurs.		Mnemonic is BP0 to BP3 according to the value of t.

Instruction group	Mnemonic		Instruction code		Bytes	Cycles	Function	Description	Status flag affected	Remarks
			$D_7 D_6 D_5 D_4$	$D_3 D_2 D_1 D_0$						
Branch instructions	BNPt addr	Branch on no Port bit	0 0 1 1 $P_7 P_6 P_5 P_4$	1 0 $t_1 t_0$ $P_3 P_2 P_1 P_0$	2	2	$PC_{7\sim0} \leftarrow P_7 P_6 P_5 P_4 P_3 P_2 P_1 P_0$ if $(P(DP_L).t_1 t_0) = 0$	If a single bit of port $P(DP_L)$ specified with the immediate data $t_1 t_0$ is 0, a branch to the address specified with the immediate data $P_7P_6P_5P_4P_3P_2P_1P_0$ within the same page occurs.		Mnemonic is BNP0 to BNP3 according to the value of t.
	BTM addr	Branch on timer	0 1 1 1 $P_7 P_6 P_5 P_4$	1 1 0 0 $P_3 P_2 P_1 P_0$	2	2	$PC_{7\sim0} \leftarrow P_7 P_6 P_5 P_4 P_3 P_2 P_1 P_0$ if TMF = 1 then TMF ← 0	If the TMF is 1, a branch to the address specified with the immediate data $P_7P_6P_5P_4P_3P_2P_1P_0$ within the same page occurs. The TMF is reset.	TMF	
	BNTM addr	Branch on no timer	0 0 1 1 $P_7 P_6 P_5 P_4$	1 1 0 0 $P_3 P_2 P_1 P_0$	2	2	$PC_{7\sim0} \leftarrow P_7 P_6 P_5 P_4 P_3 P_2 P_1 P_0$ if TMF = 0 then TMF ← 0	If the TMF is 0, a branch to the address specified with the immediate data $P_7P_6P_5P_4P_3P_2P_1P_0$ within the same page occurs. The TMF is reset.	TMF	
	BI addr	Branch on interrupt	0 1 1 1 $P_7 P_6 P_5 P_4$	1 1 0 1 $P_3 P_2 P_1 P_0$	2	2	$PC_{7\sim0} \leftarrow P_7 P_6 P_5 P_4 P_3 P_2 P_1 P_0$ if EXTF = 1 then EXTF ← 0	If the EXTF is 1, a branch to the address specified with the immediate data $P_7P_6P_5P_4P_3P_2P_1P_0$ within the same page occurs. The EXTF is reset.	EXTF	
	BNI addr	Branch on no interrupt	0 0 1 1 $P_7 P_6 P_5 P_4$	1 1 0 1 $P_3 P_2 P_1 P_0$	2	2	$PC_{7\sim0} \leftarrow P_7 P_6 P_5 P_4 P_3 P_2 P_1 P_0$ if EXTF = 0 then EXTF ← 0	If the EXTF is 0, a branch to the address specified with the immediate data $P_7P_6P_5P_4P_3P_2P_1P_0$ within the same page occurs. The EXTF is reset.	EXTF	
	BC addr	Branch on CF	0 1 1 1 $P_7 P_6 P_5 P_4$	1 1 1 1 $P_3 P_2 P_1 P_0$	2	2	$PC_{7\sim0} \leftarrow P_7 P_6 P_5 P_4 P_3 P_2 P_1 P_0$ if CF = 1	If the CF is 1, a branch to the address specified with the immediate data $P_7P_6P_5P_4P_3P_2P_1P_0$ within the same page occurs.		
	BNC addr	Branch on no CF	0 0 1 1 $P_7 P_6 P_5 P_4$	1 1 1 1 $P_3 P_2 P_1 P_0$	2	2	$PC_{7\sim0} \leftarrow P_7 P_6 P_5 P_4 P_3 P_2 P_1 P_0$ if CF = 0	If the CF is 0, a branch to the address specified with the immediate data $P_7P_6P_5P_4P_3P_2P_1P_0$ within the same page occurs.		
	BZ addr	Branch on ZF	0 1 1 1 $P_7 P_6 P_5 P_4$	1 1 1 0 $P_3 P_2 P_1 P_0$	2	2	$PC_{7\sim0} \sim P_7 P_6 P_5 P_4 P_3 P_2 P_1 P_0$ if ZF = 1	If the ZF is 1, a branch to the address specified with the immediate data $P_7P_6P_5P_4P_3P_2P_1P_0$ within the same page occurs.		
	BNZ addr	Branch on no ZF	0 0 1 1 $P_7 P_6 P_5 P_4$	1 1 1 0 $P_3 P_2 P_1 P_0$	2	2	$PC_{7\sim0} \leftarrow P_7 P_6 P_5 P_4 P_3 P_2 P_1 P_0$ if ZF = 0	If the ZF is 0, a branch to the address specified with the immediate data $P_7P_6P_5P_4P_3P_2P_1P_0$ within the same page occurs.		
	BFn addr	Branch on flag bit	1 1 0 1 $P_7 P_6 P_5 P_4$	$n_3 n_2 n_1 n_0$ $P_3 P_2 P_1 P_0$	2	2	$PC_{7\sim0} \leftarrow P_7 P_6 P_5 P_4 P_3 P_2 P_1 P_0$ if Fn = 1	If the flag bit of the 16 flags specified with the immediate data $n_3n_2n_1n_0$ is 1, a branch to the address specified with the immediate data $P_7P_6P_5P_4P_3P_2P_1P_0$ within the same page occurs.		Mnemonic is BF0 to BF15 according to the value of n.
	BNFn addr	Branch on no flag bit	1 0 0 1 $P_7 P_6 P_5 P_4$	$n_3 n_2 n_1 n_0$ $P_3 P_2 P_1 P_0$	2	2	$PC_{7\sim0} \leftarrow P_7 P_6 P_5 P_4 P_3 P_2 P_1 P_0$ if Fn = 0	If the flag bit of the 16 flags specified with the immediate data $n_3n_2n_1n_0$ is 0, a branch to the address specified with the immediate data $P_7P_6P_5P_4P_3P_2P_1P_0$ within the same page occurs.		Mnemonic is BNF0 to BNF15 according to the value of n.
Input/Output instructions	IP	Input port to AC	0 0 0 0	1 1 0 0	1	1	$AC \leftarrow (P(DP_L))$	Port $P(DP_L)$ contents are loaded in the AC.	ZF	
	OP	Output AC to port	0 1 1 0	0 0 0 1	1	1	$P(DP_L) \leftarrow (AC)$	The AC contents are outputted to port $P(DP_L)$.		
	SPB bit	Set port bit	0 0 0 0	0 1 $B_1 B_0$	1	2	$P(DP_L.B_1B_0) \leftarrow 1$	A single bit in port $P(DP_L)$ specified with the immediate data B_1B_0 is set.		When this instruction is executed, the E contents are destroyed.
	RPB bit	Reset port bit	0 0 1 0	0 1 $B_1 B_0$	1	2	$P(DP_L.B_1B_0) \leftarrow 0$	A single bit in port $P(DP_L)$ specified with the immediate data B_1B_0 is reset.	ZF	When this instruction is executed, the E contents are destroyed.
Other instructions	SCTL bit	Set control register bit(S)	0 0 1 0 1 0 0 0	1 1 0 0 $B_3 B_2 B_1 B_0$	2	2	$CTL \leftarrow (CTL) \vee B_3 B_2 B_1 B_0$	The bits of the control register specified with the immediate data $B_3B_2B_1B_0$ are set.		
	RCTL bit	Reset control register bit(S)	0 0 1 0 1 0 0 1	1 1 0 0 $B_3 B_2 B_1 B_0$	2	2	$CTL \leftarrow (CTL) \wedge \overline{B_3 B_2 B_1 B_0}$	The bits of the control register specified with the immediate data $B_3B_2B_1B_0$ are reset.	ZF	
	WTTM	Write timer	1 1 1 1	1 0 0 1	1	1	$TM \leftarrow (E).(AC)$ $TMF \leftarrow 0$	The E and AC contents are loaded in the timer. The TMF is reset.	TMF	
	HALT	Halt	1 1 1 1	0 1 1 0	1	1	Halt	All operations stop.		
	NOP	No operation	0 0 0 0	0 0 0 0	1	1	No operation	No operation is performed, but 1 machine cycle is consumed.		

*1 If the CLA instruction is used consecutively in such a manner as CLA, CLA, ——, the first CLA instruction only is effective and the following CLA instructions are changed to the NOP instructions. This is also true of the LI instruction.