


Ordering number : EN4929A

CMOS LSI

	No. 4929A	LC75366, 75366M
	Two-Channel Electronic Volume Control	



Overview

The LC75366 (DIP20) and the LC75366M (MFP20) are electronic volume controls that can be controlled by serial input data and provide volume, balance and loudness functions.

Features

- Silicon gate CMOS process for low switching noise

Functions

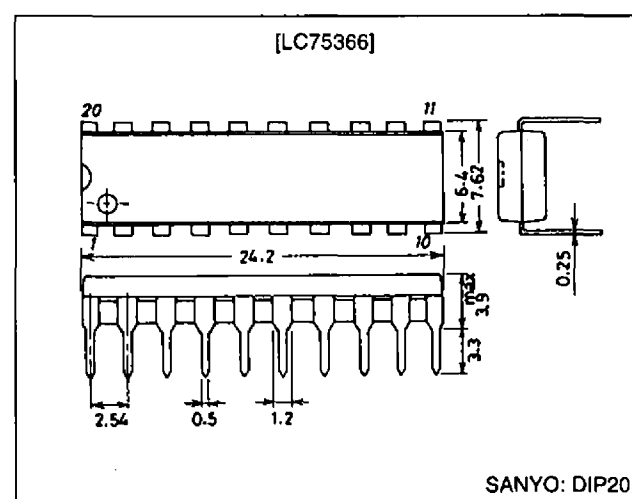
- Volume: 0 dB to -68 dB (in 2 dB steps) and $-\infty$; 36 positions.
A balance function can be implemented by controlling the left and right channel volume settings independently.
- Loudness: Taps are provided at the -20 dB positions in the 10 dB step resistor ladder used by the volume control function. A loudness function can be implemented by attaching external RC circuits at these tap points.
- An address selection pin (the S pin) allows two LC75366 chips to be used on the same bus.
- Serial data input: Supports CCB* format communication with the system controller.

- CCB is a trademark of SANYO ELECTRIC CO., LTD.
- CCB is SANYO's original bus format and all the bus addresses are controlled by SANYO.

Package Dimensions

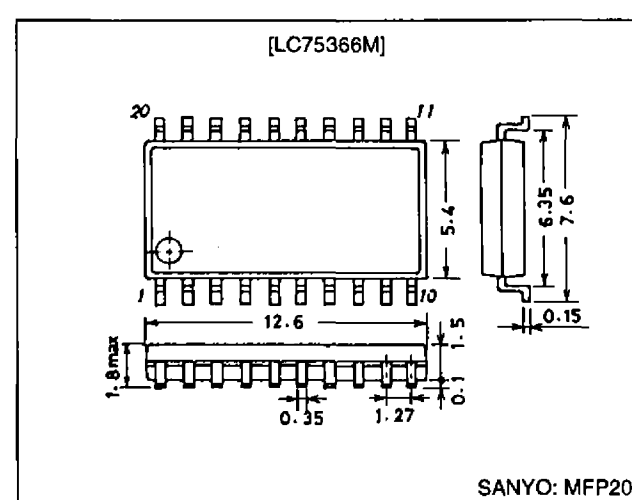
unit: mm

3021B-DIP20



unit: mm

3036B-MFP20



Specifications

Absolute Maximum Ratings at $T_a = 25^\circ\text{C}$, $V_{SS} = 0\text{ V}$

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	$V_{DD\text{ max}}$	V_{DD}	12	V
Maximum input voltage	$V_{IN\text{ max1}}$	CL, DI, CE, S	$V_{SS} - 0.3$ to $V_{DD} + 0.3$	V
	$V_{IN\text{ max2}}$	L10dBIN, L2dBIN, R10dBIN, R2dBIN	$V_{SS} - 0.3$ to $V_{DD} + 0.3$	V
Allowable power dissipation	$P_d\text{ max}$	$T_a \leq 85^\circ\text{C}$	140	mW
Operating temperature	T_{opr}		-40 to +85	$^\circ\text{C}$
Storage temperature	T_{stg}		-50 to +125	$^\circ\text{C}$

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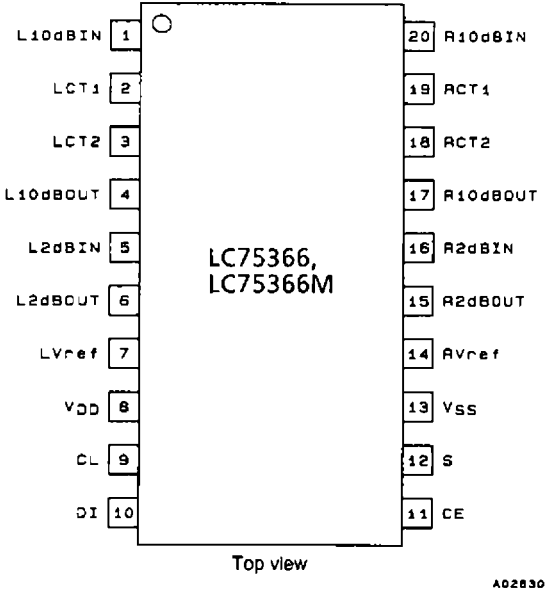
Allowable Operating Ranges at Ta = 25°C, VSS = 0 V

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	VDD	VDD	4.0 to 11.0	V
Input high level voltage	VIH (1)	CL, DI, CE	0.3 VDD + 1 to VDD	V
	VIH (2)	S	0.8 VDD to VDD	V
Input low level voltage	VIL (1)	CL, DI, CE	VSS to 0.2 VDD	V
	VIL (2)	S	VSS to 0.2 VDD	V
Input voltage amplitude	VIN	L10dBIN, L2dBIN, R10dBIN, R2dBIN	VSS to VDD	Vp-p
Input pulse width	tPW	CL	1 or longer	μs
Setup time	tSETUP	CL, DI, CE	1 or longer	μs
Hold time	tHOLD	CL, DI, CE	1 or longer	μs
Operating frequency	fOP	CL	Up to 500	kHz

Electrical Characteristics at Ta = 25°C, VSS = 0 V

Parameter	Symbol	Conditions	min	typ	max	Unit
Total harmonic distortion	THD (1)	VIN = 1 Vrms, f = 1 kHz, all settings flat overall, VDD = 9 V		0.006		%
	THD (2)	VIN = 1 Vrms, f = 20 kHz, all settings flat overall, VDD = 9 V		0.015		%
Crosstalk	CT	VIN = 1 Vrms, f = 20 kHz, all settings flat overall, Rg = 1 kΩ		85		dB
Output at maximum attenuation	VO min	VIN = 1 Vrms, f = 20 kHz, volume setting: -∞, with a 470 μF capacitor between L/R Vref and VSS		-80		dB
Total resistance	RVOL (1)	10 dB steps	28.2	47	65.8	kΩ
	RVOL (2)	2 dB steps	12	20	28	kΩ
Output off leakage current	Ioff	L10dBIN, R10dBIN, LCT1, L2dBIN, R2dBIN, RCT1, L10dBOUT, R10dBOUT, LCT2, L2dBOUT, R2dBOUT, RCT2, LVref, RVref	-10		+10	μA
Input high level current	IiH	VI = VDD (CL, CE and DI pins)			10	μA
Input low level current	IiL	VI = VSS (CL, CE and DI pins)	-10			μA
Output noise voltage	VN	All settings flat overall (IHF-A), VDD = 9 V, Rg = 1 kΩ		2	10	μV
Current drain	IDD	VDD - VSS = 11 V			1	mA
Analog switch on resistance (Design target value)	RON	CT1	180	300	420	Ω
		For use between CT2 and Vref	90	150	210	Ω
		0 dB, -∞	0.6	1.0	1.4	kΩ
		Other than the above	6.0	10.0	14.0	kΩ

Pin Assignment



Equivalent Circuit Block Diagram

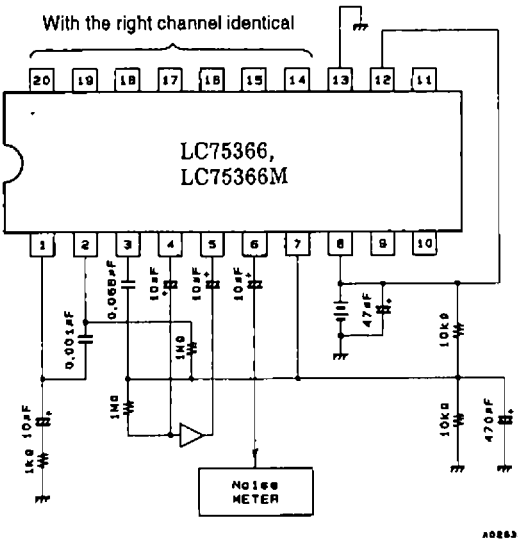


1. Total harmonic distortion

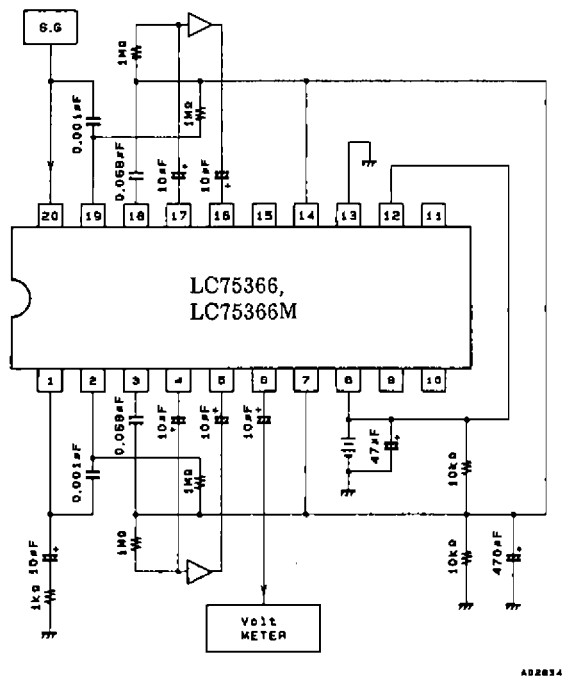


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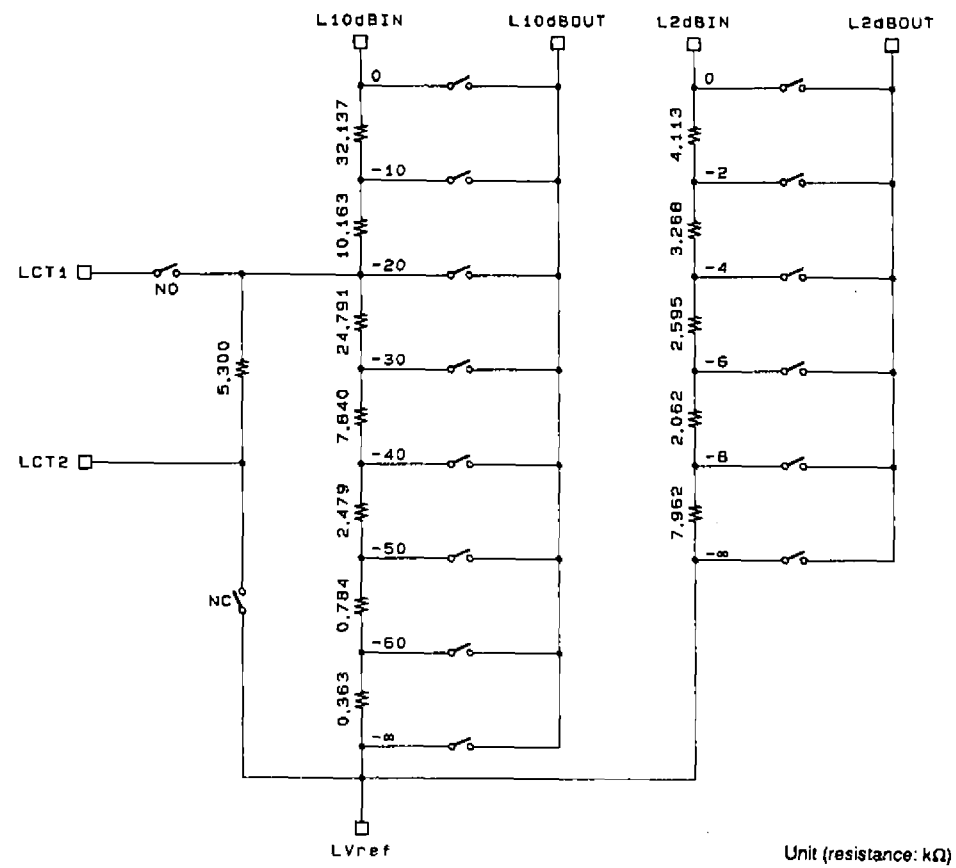
2. Output noise voltage



3. Crosstalk



Volume Block Equivalent Circuit

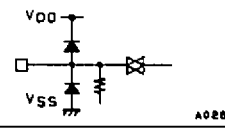
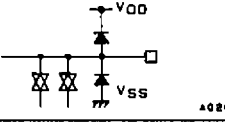
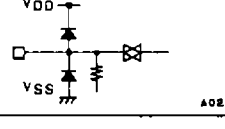
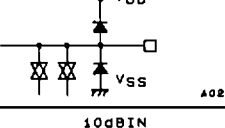
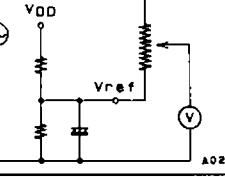
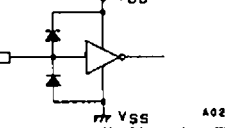
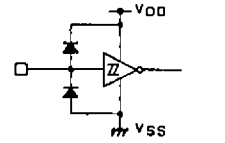
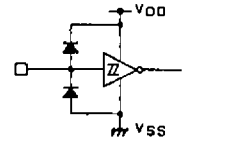


The right channel is identical.

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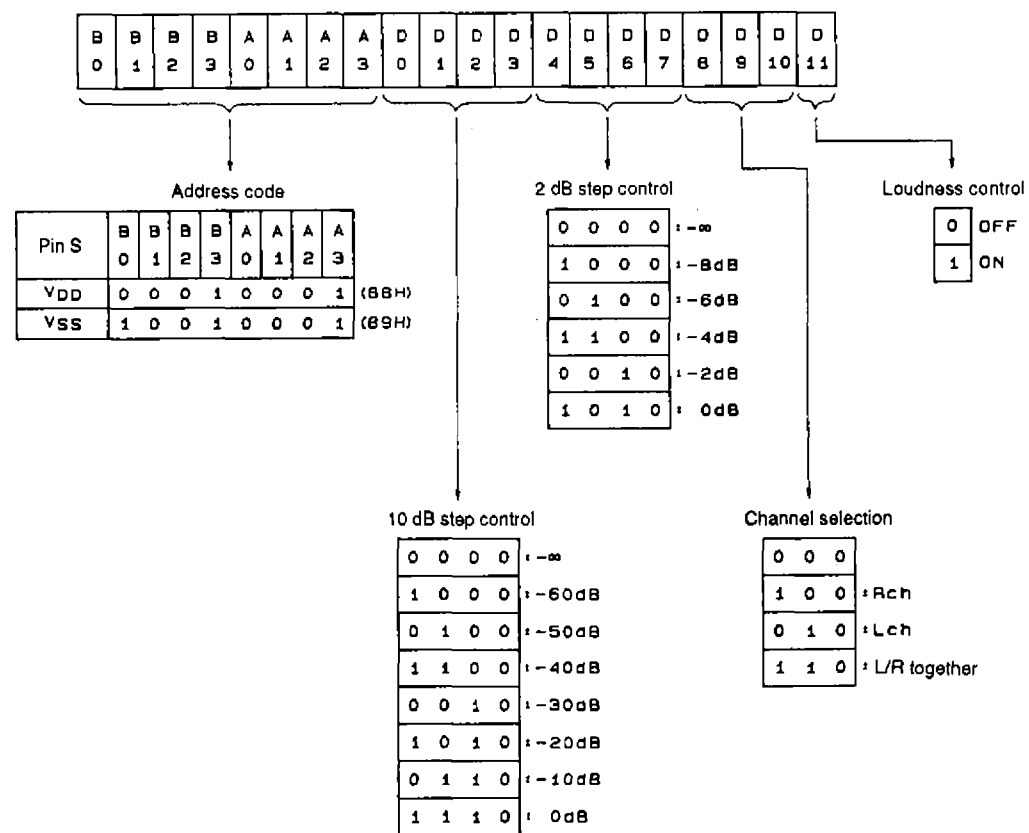
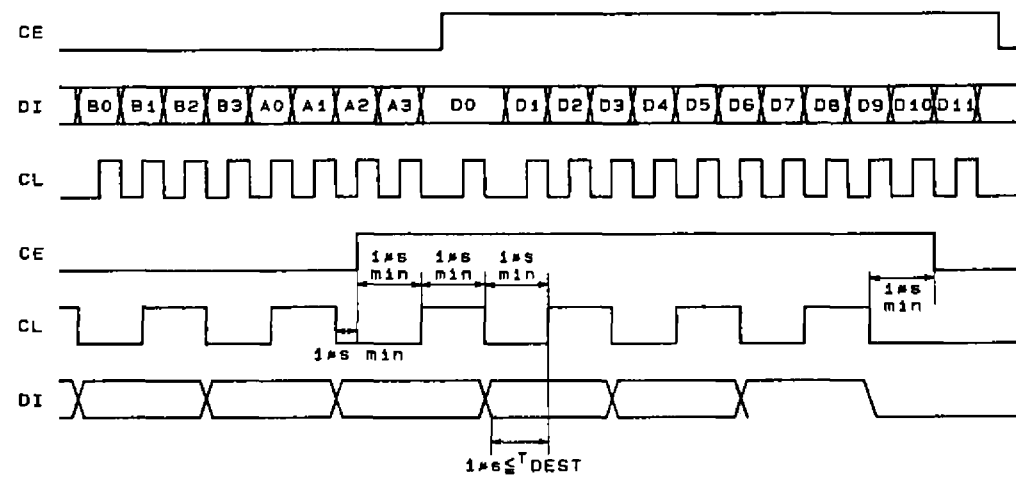
Pin Functions

Pin No.	Symbol	Function	Note
1	L10dBIN	Input pins for the 10 dB step attenuator. Must be driven from a low impedance.	
20	R10dBIN		
2	LCT1	Loudness connections. Connect a high band compensation capacitor between CT1 and 10dBIN and connect a low band compensation capacitor between CT2 and Vref.	
3	LCT2		
19	RCT1		
18	RCT2		
4	L10dBOUT	Output pins for the 10 dB step attenuator. These outputs must be received by a load of about 1 MΩ.	
17	R10dBOUT		
5	L2dBIN	Input pins for the 2 dB step attenuator. Must be driven from a low impedance.	
16	R2dBIN		
6	L2dBOUT	Output pins for the 2 dB step attenuator. These outputs must be received by a load of about 1 MΩ.	
15	R2dBOUT		
7	LVref	Volume circuit common pins. The impedance of the pattern connected to these pins should be kept as low as possible. Since the capacitors between Vref and VSS form the residual resistance components when the volume is cut, adequate care must be taken in determining the value of these capacitors.	
14	RVref		
12	S	Pin that selects the address code in the data format. Data will be accepted for an address code of 88 when this pin is tied to VDD, and for an address code of 89 when tied to VSS.	
9	CL	Serial data and clock inputs for control	
10	DI		
11	CE	Chip enable. The internally latched data is written and the analog switches operate when this pin goes from high to low. Data transfer is enabled when this pin is at the high level.	
8	VDD	These pins must be connected to the power supply.	
13	VSS		

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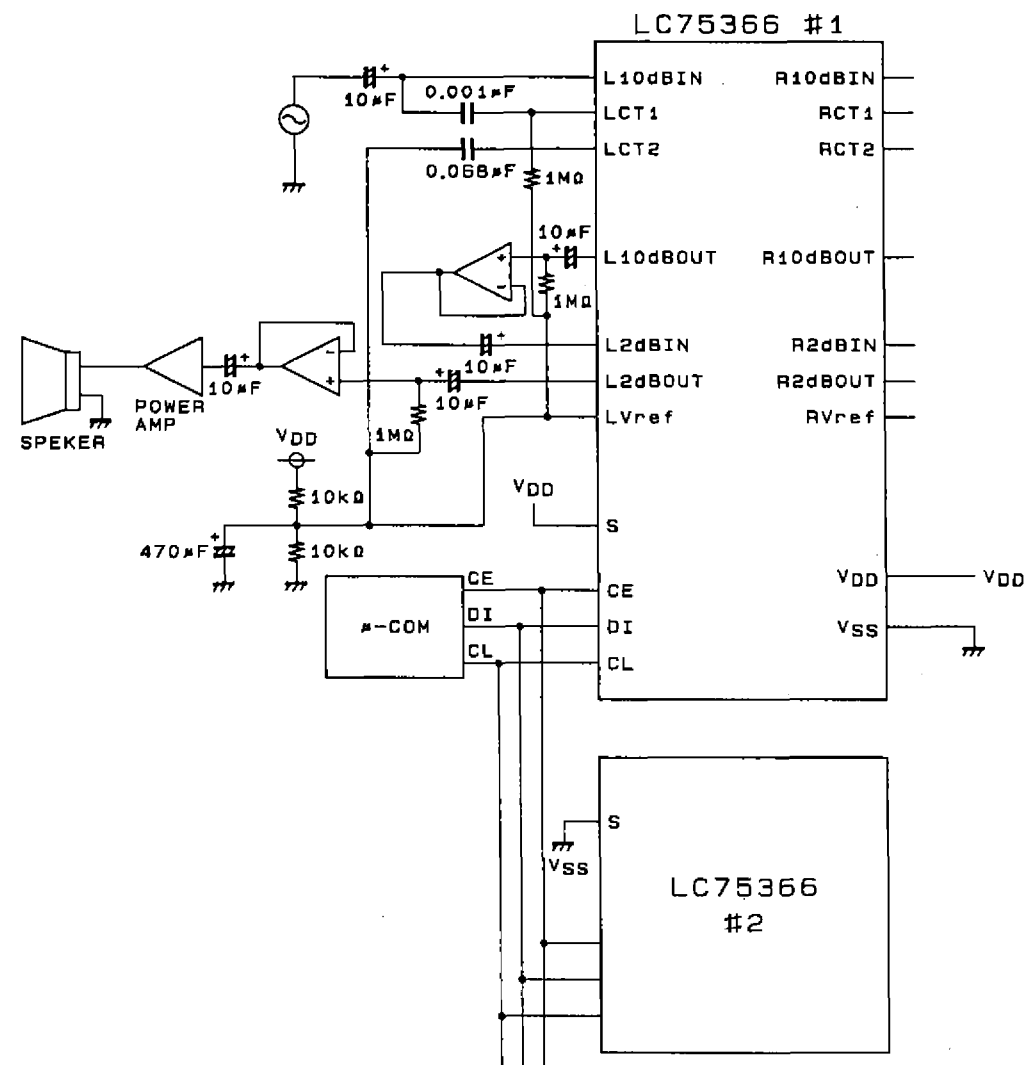
Control System Timing and Data Format

Apply the stipulated serial data to the CE, CL and DI pins to control the LC75366 and LC75366M. The data consists of 20 bits, of which 8 bits are the address and 12 bits are control data.

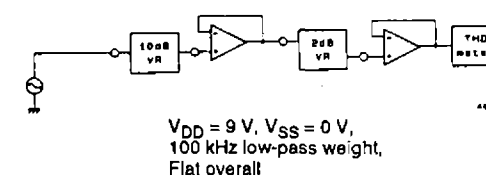
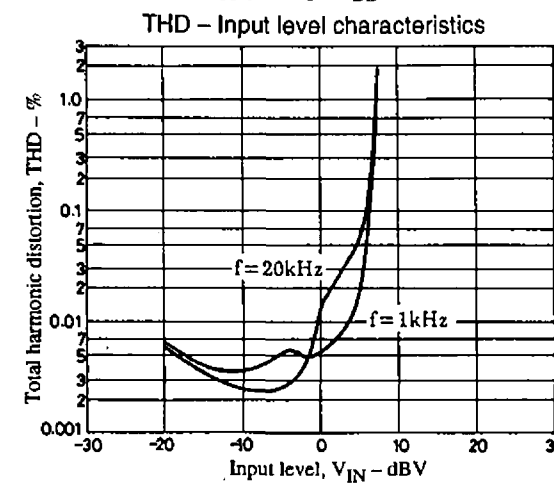
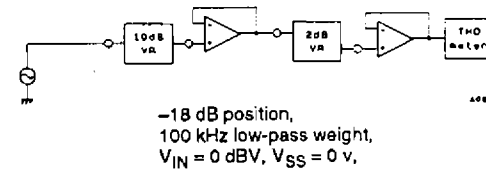
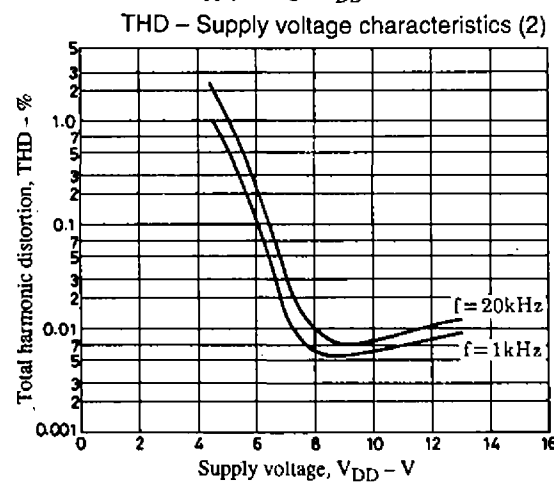
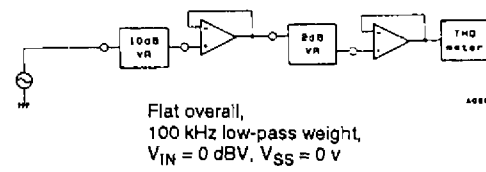
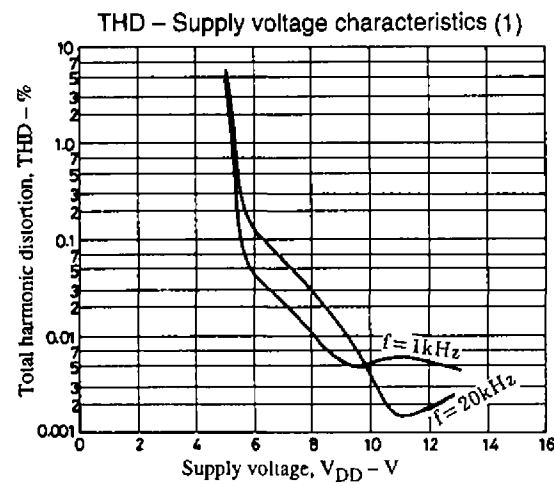
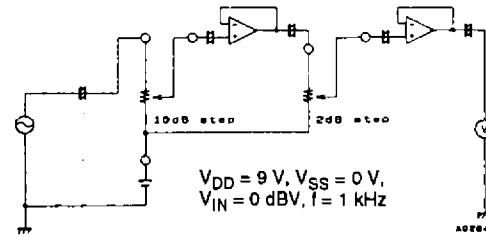
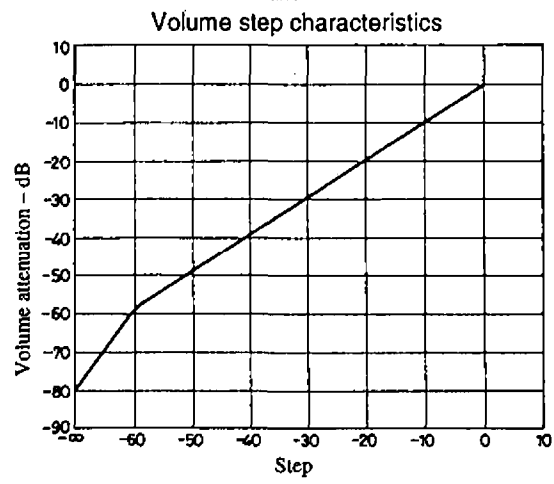


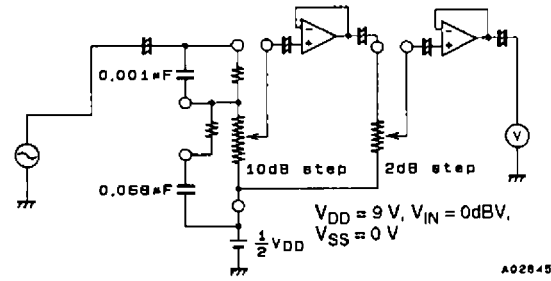
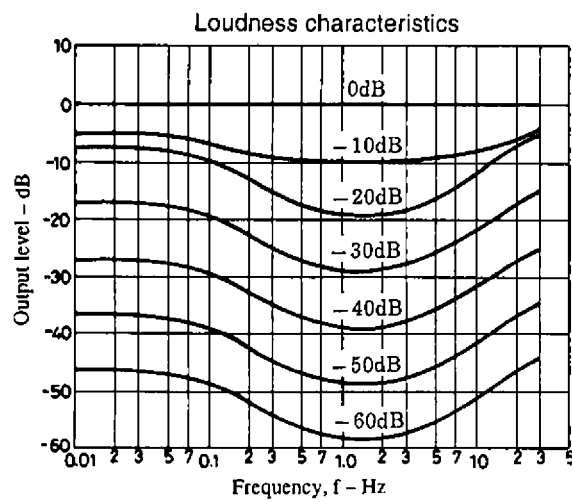
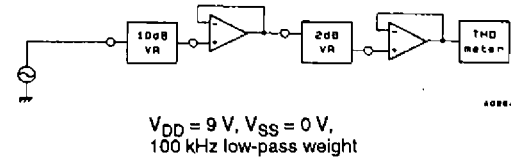
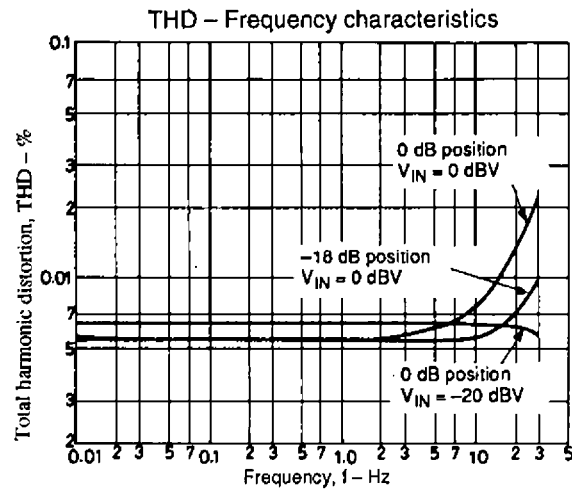
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Sample Application Circuit



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Loudness Function External Circuit Constant Calculation Example

First, refer to the LC75366 and LC75366M 10 dB step internal equivalent circuit shown on page 5. Figure 1 below shows this circuit simplified with the external components used for the loudness function connected for this calculation. The sample calculation below uses this diagram to acquire a 5 dB boost at $f = 100$ Hz.

($f = 100$ Hz, 5 dB boost)
Let R and C in Figure 1 be:
 $R1 = R2 = 10$ k Ω
 $R3 = 1$ k Ω
 $C1 = Z1, C2 = Z2$
Then:

$$V_{OUT} = \frac{\frac{R2(R3 + Z2)}{R2 + R3 + Z2}}{\frac{R1 \cdot Z1}{R1 + Z1} + \frac{R2(R3 + Z2)}{R2 + R3 + Z2}} = -20 \text{ dB}$$

(at = 1 kHz)

$$V_{OUT} = \frac{\frac{R2(R3 + 10 \cdot Z2)}{R2 + R3 + 10 \cdot Z2}}{\frac{R1 \cdot 10 \cdot Z1}{R1 + 10 \cdot Z1} + \frac{R2(R3 + 10 \cdot Z2)}{R2 + R3 + 10 \cdot Z2}} = -15 \text{ dB}$$

(at = 100 Hz)

Solving the above equations gives:

$Z1 \approx 178.3$ k Ω and $Z2 = 176$ Ω

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Therefore, under such conditions where $f = 1 \text{ kHz}$, specifications may be satisfied if C (capacitor) having these impedances is supplied externally.

The result is that $C1 = 893 \text{ pF}$ and $C2 = 0.9 \text{ }\mu\text{F}$.

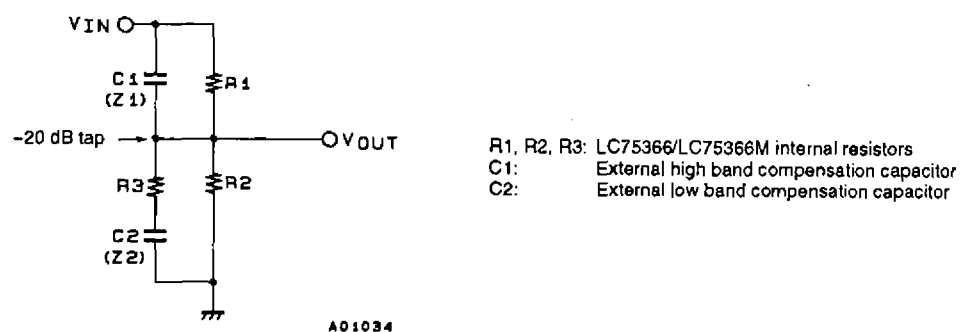


Figure 1

Usage Notes

1. The states of the internal analog switches will be indeterminate when power is first applied. Muting should be applied externally until control data has been transferred and stored.
2. The signal lines for the CL, DI and CE pins should either be covered by the pattern ground or be formed from shielded cable to prevent the high-frequency digital signals transmitted over these lines from entering the analog system.

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