

### **OVERVIEW**

The LC8956 is an error-correcting and ADPCM decoding IC for use in CD-I and CD-ROM XA systems. The LC8956 was developed through the integration of LC8951 and LC8955 ICs into a single chip. The LC8956 incorporates RAM for erasure correction and can use from 64 to 512 Kbits of external SRAM.

The LC8956 operates from a 5.0 V supply and is available in 100-pin SQFPs and QIPs.

### **FEATURES**

- Compatible with CD-ROM, CD-I and CD-ROM XA systems
- · Real-time error detection and correction
- 2.3 Mbyte/s data transfer rate
- Multiple-block buffering for low-speed host applications
- Command-status stack for host interface
- ADPCM decoder block
- 8 Kbit RAM for erasure correction
- CMOS compatible
- Single 5 V power supply
- 100-pin SQFP and 100-pin QIP

#### PINOUT



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# **PACKAGE DIMENSIONS**

Unit: mm 3151-QIP100E



### **BLOCK DIAGRAM**



# **PIN DESCRIPTION**

1     SA0     Host negister citip auto: liqui       2     ZAPCS     Host negister citip auto: liqui       3     BUSY     ADPCM data with BUSY output       4     INTH     Host Interrupt output       5     HDE     Ensure Bis quotup. TAultup resistance       8     MD7     Host data (ICO) signal 7. Pull-up resistance       8     HD5     Host data (ICO) signal 6. Pull-up resistance       9     HD4     Host data (ICO) signal 5. Pull-up resistance       9     HD4     Host data (ICO) signal 5. Pull-up resistance       10     HD3     Host data (ICO) signal 3. Pull-up resistance       11     HD2     Host data (ICO) signal 3. Pull-up resistance       11     HD2     Host data (ICO) signal 3. Pull-up resistance       11     HD1     Host data (ICO) signal 0. Pull-up resistance       12     HD1     Host data (ICO) signal 0. Pull-up resistance       14     VSS     Ground       15     ZEGOP     End of poccess signal output (used in data DMA transfer)       16     MSTEMON     Audio block monitor output       17     MEMPHAS     Audio block monitor output       18     OLRCK     DAC output	Number	Name	Description
3       BUSY       ADPCM data write BUSY output         4       INTH       Hoat Interrupt output         5       HDE       Ensure flag output. Pulkup residence         6       HD7       Hoat data (I/O) signal 7. Pulkup residence         7       HDB       Hoat data (I/O) signal 8. Pulkup residence         8       HD5       Hoat data (I/O) signal 8. Pulkup residence         9       HD4       Hoat data (I/O) signal 4. Pulkup residence         10       HD3       Hoat data (I/O) signal 3. Pulkup residence         11       HD2       Hoat data (I/O) signal 4. Pulkup residence         12       HD1       Hoat data (I/O) signal 7. Pulkup residence         13       HD0       Hoat data (I/O) signal 7. Pulkup residence         14       VSS       Ground         15       ZEDP       End of process signal output (used in data DMA transfer)         14       VSS       Ground         15       ZEDP       End of process signal output         17       MEMPHAS       Audio block monitor output         18       OLRCK       DAC output         20       OBCLK       DAC output         21       SOCI1       LOBBACK-	1	SAO	Host register select input
4   INTH   Host Interrupt output     5   HDE   Erasure flag output Pulk-up resistance     6   HD7   Host data (I/O) signal 7. Pulk-up resistance     7   HD8   Host data (I/O) signal 6. Pulk-up resistance     8   HD5   Host data (I/O) signal 6. Pulk-up resistance     9   HD4   Host data (I/O) signal 6. Pulk-up resistance     10   HD3   Host data (I/O) signal 1. Pulk-up resistance     11   HD2   Host data (I/O) signal 1. Pulk-up resistance     11   HD2   Host data (I/O) signal 0. Pulk-up resistance     11   HD2   Host data (I/O) signal 1. Pulk-up resistance     13   HD0   Host data (I/O) signal 0. Pulk-up resistance     14   VSS   Ground     15   ZEOP   End of process signal output (used in data DMA transfer)     16   MSTEMON   Audio block monitor output     17   MEMPHAS   Audio block monitor output     18   OLRCK   DAC output     20   OBCLK   DAC output     21   SOC1   L2788K-compatible output     22   DACCK   Clock output     23   VSS   Ground     24   RAD   RAM address output 1     25   RA1   RAM address output 1 <td>2</td> <td>ZAPCS</td> <td>Host register chip select input</td>	2	ZAPCS	Host register chip select input
5       HDE       Ensure flag output. Pull-up resistance         6       HD7       Hort data (I/O) signal 7. Pull-up resistance         7       HD6       Hort data (I/O) signal 8. Pull-up resistance         9       HD4       Host data (I/O) signal 8. Pull-up resistance         9       HD4       Host data (I/O) signal 4. Pull-up resistance         10       HD3       Host data (I/O) signal 3. Pull-up resistance         11       HD2       Host data (I/O) signal 3. Pull-up resistance         12       HD1       Host data (I/O) signal 3. Pull-up resistance         13       HD0       Host data (I/O) signal 0. Pull-up resistance         14       VSS       Ground         15       ZEOP       End of process signal output (used in data DMA transfer)         16       MSTEMON       Audio block monitor output         17       MEMPHAS       Audio block monitor output         18       OLROK       DAC output         20       OBCLK       DAC output         21       SOC1       LG7883K-compatible output         22       DACOK       Cock output         23       VSS       Ground         24       RA0       R	З	BUSY	ADPCM data write BUSY output
5   HD7   Host data (IC) signal 7. Pullup resistance     7   HD6   Host data (IC) signal 6. Pullup resistance     8   HD6   Host data (IC) signal 6. Pullup resistance     9   HD4   Host data (IC) signal 3. Pullup resistance     10   HD3   Host data (IC) signal 3. Pullup resistance     11   HD2   Host data (IC) signal 3. Pullup resistance     12   HD1   Host data (IC) signal 2. Pullup resistance     13   HD0   Host data (IC) signal 0. Pullup resistance     14   VSS   Ground     15   ZEOP   End of process signal output (used in data DMA teaster)     16   MSTEMON   Audio book montor output     17   MEMPHAS   Audio book montor output     18   OLRCK   DAC output     20   OBCLK   DAC output     21   SOC1   LC7883K-competible output     22   DACCK   Glock output 1     23   VSS   Ground     24   RAO   RAM address output 0     25   RA1   RAM address output 1     26   RA2   RAM address output 3     28   RA4   RAM address output 4     29   RA5   RAM address output 4     29   RA5   RAM addres	4	INTH	Host interrupt output
7     HD6     Hot data (K0) signal 6. Pull-up resistance       8     HD5     Hot data (K0) signal 5. Pull-up resistance       9     HD4     Hest data (K0) signal 5. Pull-up resistance       10     HD3     Host data (K0) signal 5. Pull-up resistance       11     HD2     Host data (K0) signal 7. Pull-up resistance       11     HD2     Host data (K0) signal 7. Pull-up resistance       12     HD1     Host data (K0) signal 7. Pull-up resistance       13     HD0     Host data (K0) signal 7. Pull-up resistance       14     VSS     Ground       15     ZECP     End of process signal output (used in data DMA transfer)       16     MSTEMON     Audio block monitor output       17     MEMPHAS     Audio block monitor output       18     OLRCK     DAC output       20     OBCLK     DAC output       21     SOC1     LC7se3K-compatible output       22     DACCK     Clock output       23     VSS     Bround       24     FA0     RAM address output 0       25     RA1     RAM address output 1       26     RA2     RAM address output 1	5	HDE	Erasure flag output. Putl-up resistance
8       HD5       HD4 (ata (IC)) signal 5. Pull-up resistance         9       HD4       Host data (IC) signal 5. Pull-up resistance         10       HD3       Host data (IC) signal 5. Pull-up resistance         11       HD2       Host data (IC) signal 5. Pull-up resistance         12       HD1       Host data (IC) signal 1. Pull-up resistance         13       HD0       Host data (IC) signal 0. Pull-up resistance         14       VSS       Ground         15       ZEOP       End of process signal output (used in data DMA transfer)         16       MSTEMON       Audio block monitor output         17       MEMPHAS       Audio block monitor output         18       OLRCK       DAC output         20       OBCLK       DAC output         21       SOC1       LC7s84K-compatible output         22       DACCK       Clock output         23       VSS       Ground         24       FAA       RAM address output 0         25       RA1       RAM address output 1         26       RA2       RAM address output 3         28       RA4       RAM address output 4         29	6	HD7	Host data (I/O) signal 7. Pull-up resistance
9HD4Host data (UC) signal 4. Pul-up resistance10HD3Host data (UC) signal 3. Pul-up resistance11HD2Host data (IKO) signal 2. Pul-up resistance12HD1Host data (IKO) signal 2. Pul-up resistance13HD0Host data (IKO) signal 0. Pul-up resistance14VS5Ground15ZEOPEnd of process signal output (used in data DMA transfer)16MSTEMONAudio block monitor output17MEMPHASAudio block monitor output18OLRCKDAC output20OBCLKDAC output21SOC1LC788X-compatible output22DACCKClock output23VS5Ground24RAORAM address output 025RA1RAM address output 126RA2RAM address output 127RA3RAM address output 428NA4RAM address output 530RA5RAM address output 631RA7RAM address output 633RA9RAM address output 732RA5RAM address output 633RA9RAM address output 732RA5RAM address output 633RA9RAM address output 134RA10RAM address output 135RA11RAM address output 136RA5RAM address output 137RA12RAM address output 1237RA13RAM address output 13	7	HD6	Host data (I/O) signal 6. Pull-up resistance
10HD3Hest data (VO) signal 3. Pul-up resistance11HD2Host data (VO) signal 2. Pul-up resistance12HD1Host data (VO) signal 1. Pul-up resistance13HD0Host data (VO) signal 0. Pul-up resistance14VSSGround16ZEOPEnd of process signal output (used in data DMA transfer)16MSTEMONAudio block monitor output17MEMPHASAudio block monitor output18OLRCKDAC output19ODATADAC output20OBCLKDAC output21SOC1LC7884K-compatible output22DACCKClock output23VSSGround24RA0RAM address output 125RA1RAM address output 227RA2RAM address output 328RA2RAM address output 429RA5RAM address output 321RA4RAM address output 323VSSGround24RA2RAM address output 125RA1RAM address output 126RA2RAM address output 327RA3RAM address output 328RA4RAM address output 429RA5RA4 address output 530RA6RAM address output 531RA7RAM address output 633RA9RAM address output 1035RA11RAM address output 1138RA12RAM address output 12 <t< td=""><td>8</td><td>HD5</td><td>Host data (VO) signal 5. Pull-up resistance</td></t<>	8	HD5	Host data (VO) signal 5. Pull-up resistance
11     HD2     Hot data (I/O) signal 2. Pull-up resistance       12     HD1     Hot data (I/O) signal 1. Pull-up resistance       13     HD0     Hot data (I/O) signal 0. Pull-up resistance       14     VSS     Ground       15     ZEOP     End of process signal output (used in data DMA transfer)       16     MSTEMON     Audio block monitor output       17     MEMPHAS     Audio block monitor output       18     OLRCK     DAC output       20     OBCLK     DAC output       21     SOC1     LC7883K-compatible output       22     DACCK     Clock output       23     VSS     Ground       24     RA0     RAM address output 0       25     RA1     RAM address output 1       26     RA2     RAM address output 2       27     RA3     RAM address output 3       28     RA4     RAM address output 4       29     RA5     RAM address output 4       29     RA5     RAM address output 1       28     RA4     RAM address output 3       29     RA5     RAM address output 4       2	9	HD4	Host data (VO) signal 4. Pull-up resistance
12HD1Host data (VO) signal 1. Pull-up resistance13HD0Host data (VO) signal 0. Pull-up resistance14VSSGround15ZEOPEnd of process signal output (used in data DMA transfer)16MSTEMONAudio block monitor output17MEMPHASAudio block monitor output18OLRCKDAC output19ODATADAC output20OBCLKDAC output21SOC1LC7883K-competible output22DACCKClock output23VSSGround24RA0RAM address output 125RA1RAM address output 227RA3RAM address output 328RA4RAM address output 429RA5RA4 address output 530RA6RAM address output 631RA7RAM address output 633RA9RAM address output 833RA9RAM address output 136RA11RAM address output 136RA12RAM address output 137RA13RAM address output 138RA1RAM address output 137RA13RAM address output 10	10	HD3	Host data (VO) signal 3. Pull-up resistance
13     HDD     Host data (VC) signal 0. Pull-up resistance       14     VSS     Ground       15     ZEOP     End of process signal output (used in data DMA transfer)       16     MSTEMON     Audio block monitor output       17     MEMPHAS     Audio block monitor output       18     OLRCK     DAC output       19     ODATA     DAC output       20     OBCLK     DAC output       21     SOC1     LC78e3K-compable output       22     DACCK     Clock output       23     VSS     Ground       24     RAO     RAM address output 0       25     RA1     RAM address output 1       26     RA2     RAM address output 2       27     RA3     RAM address output 3       28     RA4     RAM address output 4       29     RA5     RAM address output 5       30     RA6     RAM address output 6       31     RA7     RAM address output 6       33     RA9     RAM address output 9       34     RA10     RAM address output 10       35     RA11     RAM address outpu	11	HD2	Host data (VO) signal 2. Pull-up resistance
14VSSGround15ZEOPEnd of process signal output (used in data DMA transfer)16MSTEMONAudio block monitor output17MEMPHASAudio block monitor output18OLRCKDAC output20OBCLKDAC output21SOC1LC7easK-compatible output22DACCKClock output23VSSGround24RAORAM address output 125RA1RAM address output 226RA2RAM address output 128VSSGround29RAARAM address output 126RA2RAM address output 227RA3RAM address output 328RA4RAM address output 429RA5RAM address output 530RA6RAM address output 732RA9RAM address output 833RA9RAM address output 1036RA11RAM address output 1337RA13RAM address output 1237RA13RAM address output 13	12	HD1	Host data (VO) signal 1. Pull-up resistance
15ZEOPEnd of process signal output (used in data DMA transfer)16MSTEMONAudio block monitor output17MEMPHASAudio block monitor output18OLRCKDAC output19ODATADAC output20OBCLKDAC output21SOC1LC7883K-compatible output22DACCKClock output23VSSGround24RAORAM address output 025RA1RAM address output 126RA2RAM address output 227RA3RAM address output 328RA4RAM address output 429RA5RAM address output 530RA5RAM address output 732RA6RAM address output 732RA9RAM address output 734RA10RAM address output 735RA1RAM address output 1036RA1RAM address output 1337RA13RAM address output 1036RA11RAM address output 1337RA13RAM address output 1236RA11RAM address output 1036RA12RAM address output 1237RA13RAM address output 13	13	HD0	Host data (VO) signal 0. Pull-up resistance
16MSTEMONAudio block monitor output17MEMPHASAudio block monitor output18OLRCKDAC output19ODATADAC output20OBCLKDAC output21SOC1LC7883K-compatible output22DACCKClock output23VSSGround24RA0RAM address output 025RA1RAM address output 126RA2RAM address output 227RA3RAM address output 328RA4RAM address output 429RA5RAM address output 530RA6RAM address output 631RA7RAM address output 732RA8RAM address output 833RA9RAM address output 834RA10RAM address output 1035RA1RAM address output 136RA12RAM address output 137RA13RAM address output 1	14	VSS	Ground
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21SOC1LC783K-compatible output22DACCKClock output23VSSGround24RA0RAM address output 025RA1RAM address output 126RA2RAM address output 227RA3RAM address output 328RA4RAM address output 429RA5RAM address output 530RA6RAM address output 631RA7RAM address output 732RA8RAM address output 833RA9RAM address output 934RA10RAM address output 1035RA11RAM address output 1237RA13RAM address output 13	19	ODATA	DAC output
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26RA2RAM address output 227RA3RAM address output 328RA4RAM address output 429RA5RAM address output 530RA6RAM address output 631RA7RAM address output 732RA8RAM address output 833RA9RAM address output 934RA10RAM address output 1035RA11RAM address output 1237RA13RAM address output 13	24	RAO	RAM address output 0
27RA3RAM address output 328RA4RAM address output 429RA5RAM address output 530RA6RAM address output 631RA7RAM address output 732RA8RAM address output 833RA9RAM address output 934RA10RAM address output 1035RA11RAM address output 1237RA13RAM address output 13	25	RA1	RAM address output 1
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29RA5RAM address output 530RA6RAM address output 631RA7RAM address output 732RA8RAM address output 833RA9RAM address output 934RA10RAM address output 1035RA11RAM address output 1136RA12RAM address output 1237RA13RAM address output 13	27	RA3	RAM address output 3
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33RA9RAM address output 934RA10RAM address output 1035RA11RAM address output 1136RA12RAM address output 1237RA13RAM address output 13	31	RA7	RAM address output 7
34   RA10   RAM address output 10     35   RA11   RAM address output 11     36   RA12   RAM address output 12     37   RA13   RAM address output 13	32	RA8	RAM address output 8
35   RA11   RAM address output 11     36   RA12   RAM address output 12     37   RA13   RAM address output 13	33	RA9	RAM address output 9
36   RA12   RAM address output 12     37   RA13   RAM address output 13	34	RA10	RAM address output 10
37 RA13 RAM address output 13	35	RA11	RAM address output 11
	36	RA12	RAM address output 12
38 RA14 RAM address output 14	37	RA13	RAM address output 13
······	38	RA14	RAM address output 14

Number	Name	Description
39	RA15	RAM address output 15
40	VSS	Ground
41	VDD	5 V supply
42	ZRWE	RAM write output
43	ZROE	RAM read output
44	ERA	Erasure flag data 1/0
45	lOo	RAM data buffer I/O 0. Pull-up resistance
46	IO1	RAM data buffer I/O 1. Pull-up resistance
47	102	RAM data buffer I/O 2. Pull-up resistance
48	IO3	RAM data buffer VO 3. Pull-up resistance
49	104	RAM data buffer I/O 4. Pull-up resistance
50	IO5	RAM data buffer I/O 5. Pull-up resistance
51	106	RAM data buffer I/O 6. Pull-up resistance
52	107	RAM data buffer I/O 7. Pull-up resistance
53	VSS	Ground
54	EXTAL	Crystal oscillator input
55	XTAL	Crystal oscillator output
56	TEST	Test input. Normally connected to VSS
57	VSS	Ground
58	МСК	CD-DSP output
59	LRCK	CD-DSP input
60	SDATA	CD-DSP input
61	BCK	CD-DSP input
62	C2PO	CD-DSP input
63	WFCK	SUB-code input
64	EXCK	SUB-code output
65	SBSO	SUB-code input
66	SCOR	SUB-code input
67	CEMPHAS	Connect to CD-DSP EMPHAS
68	ZRESET	Reset input (Reset by a 1 µs LOW-level pulse)
69	SCPUCNT	SUB-CPU I/F selection input
70	Do	SUB-CPU data I/O 0. Pull-up resistance
71	D1	SUB-CPU data VO 1. Pull-up resistance
72	D2	SUB-CPU data 1/O 2. Pull-up resistance
73	D3	SUB-CPU data I/O 3. Puli-up resistance
74	D4	SUB-CPU data 1/0 4. Pull-up resistance
75	D5	SUB-CPU data I/O 5. Pull-up resistance
76	D6	SUB-CPU data I/O 6. Pull-up resistance
77	D7	SUB-CPU data I/O 7. Pull-up resistance

Number	Name	Description
78	VSS	Ground
79	SUAO	SUB-CPU register address select input 0
80	SUA1	SUB-CPU register address select input 1
81	SUA2	SUB-CPU register address select input 2
82	SUA3	SUB-CPU register address select input 3
83	SUA4	SUB-CPU register address select input 4
84	NC	No connection
85	ZINT	SUB-CPU interrupt signal output (open drain). Pull-up resistance
86	RS(ALE)	Internal register set input
87	ZRD	SUB-CPU read input
88	ZWR	SUB-CPU write input
89	VDD	5 V supply
90	VSS	Ground
91	ZCS	SUB-CPU chip select output
92	ZENABLE	HOST chip select input
93	SELDRQ	DRO/WAIT select input
94	ZWAIT/DRQ	DRQ/ZWAIT select output
95	ZDTEN	Data enable output
96	ZSTEN	Status enable output
97	ZHWR	Host data write input
98	ZHRD	Host data read input
99	ZCMD	Host data/command select input
100	SA1	Audio block register select input

### Note

Pin names that begin with Z denote active-LOW pins.

## **SPECIFICATIONS**

# Absolute Maximum Ratings

 $V_{ss} = 0 V$ 

Parameter	Symbol	Rating	Unit	
Suppy voltage range	V <sub>DD</sub>	-0.3 to 7.0	v	
Input voltage range	Vi	-0.3 to V <sub>DD</sub> + 0.3	v	
Output voltage range	Vo	-0.3 to V <sub>DD</sub> + 0.3	v	
Power dissipation	PD	350	mW	
Operating temperature range	Topr	-30 to 70	°C	
Storage temperature range	T <sub>stg</sub>	55 to 125	°C	
Soldering temperature	TsLD	260	°C	
Soldering time	tsu0		s	

# **Recommended Operating Conditions**

#### $V_{SS} = 0$ V, $T_a = 25$ °C

Parameter	Symbol	Rating	Unit
Suppy voltage	V <sub>DD</sub>	5.0	v
Supply voltage range	V <sub>DD</sub>	4.5 to 5.5	V

### **DC Electrical Characteristics**

$V_{DD} = 4.5$ to 5.5	ν,	$V_{SS} =$	0 V,	, T. =	= -30 to	70	°C	unless	otherwise	noted
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Parameter	Symbol	Condition				
		Condition	ការ៉ា	typ	max	Unit
LOW-level input voltage	VIL1	See note 1.	-	-	0,8	٧
HIGH-level input voltage	ViH1	See note 1.	2.2	_	-	v
LOW-level input voltage	V <sub>IL2</sub>	See note 2.	-	-	0.6	v
HIGH-level input voltage	V <sub>IH2</sub>	See nole 2.	2.5	-	_	v
LOW-level cutput voltage	VoL1	l <sub>oL1</sub> = 9 mA	-	_	0.4	v
LOW-level output voltage	V <sub>OL2</sub>	l <sub>012</sub> = 3 mA	-	-	0.4	v
HIGH-level output voltage	Vohi	loн1 = -3 mA	2.4	-	-	v
Input leakage current	ı ار	VI = Vss or VDD	-25	_	25	.μΑ
Pull-up resistance	Rup		10	20	40	kΩ

### Notes

1. All pins except ZHRD, ZHWR, ZENABLE, ZCMD, ZRD, ZCS, ZWR, WFCK, SBSO, SCOR and XTALCK

2. Reset (Schmitt-trigger) and all bus pins

# FUNCTIONAL DESCRIPTION

#### System Configuration



### CD Player Interface/Data Input

Internal registers CSEL and LMSEL select one of three different serial input formats for CD player data communications.

An internal synchronization detection circuit synchronizes and formats input data into block sector units. The synchronization routine employs a sync signal interpolation circuit after pattern detection on external data input. Both synchronization interpolation and pattern detection functions are ON/OFF controllable.

After passing through a descrambling circuit, input data is written to buffer RAM in 8-bit data streams. The C2 error flag (pointer) from the CD player is also stored in RAM. When using 128 Kbits or more of error correction memory, 9 bits of RAM are made available. The C2 error flag can be omitted, in which case 8 bits of RAM are sufficient. In this case, however, erasure correction is no longer supported.

All input data, including sync, header, subheader and parity bits (2352 bytes in total), are written from CD player to RAM sequentially.

In addition, the LC8956 has a master clock output, MCK, to provide oscillator input signals for external CD player ICs.

#### **Error Detection and Correction**

When a sector block of 2352 bytes of data accumulates in RAM, error-correction decoding occurs. Error correction functions are performed in real-time. Accordingly, the software need only wait for the completion of processing. Also, buffering of CD input data and transfer of host computer data can continue simultaneously. This means that data for which error-correction processing has been completed can be transferred to the host without affecting the CD player data transfer rate.

Detection and correction can be combined with erasure correction to ensure high data reliability. Detection and correction can handle one symbol errors, while erasure correction can handle two symbol errors.

The correction algorithm is programmable. The LC8956 can be instructed to use reiterative correction, QP/PQ correction and other means of data reliability enhancement.

After error-correcting code (ECC) decoding, a 32-bit CRC check is performed by the error-detection code (EDC). During CRC checks, the header and subheader are stored in internal registers. After the CRC check, a decoding-complete interrupt is issued to the controlling microcomputer, which then reads the header and subheader of the decoded block and the start address of the block in buffer RAM.

The LC8956 contains 8 Kbits of RAM for erasure correction, so an additional 8 Kbits of external RAM is typically sufficient.

#### Host Interface

The host to LC8956 data transfer rate is 2.3 Mbytes/s. Buffer RAM is a maximum of 60 Kbytes, so that up to 26 sectors can be stored with the CD-ROM drive and used as disk cache memory.

The host interface design incorporates an 8-byte FIFO stack for host command data input. Using control signals on ZHWR, the host can instantaneously write up to 8-bytes of commands. When the host writes to the stack, the LC8956 issues a command interrupt to the controller, and the commands written to the stack are not interpreted. When transferring data to the host, an LC8956 register is set with the number of bytes to be sent and the starting address in buffer RAM of the next block to be sent, and then the transfer trigger register is written to. Then ZDTEN goes LOW, informing the host of the start of data transfer. While ZDTEN is LOW, the host continues to issue ZHRD read pulses and reads data. When the speed with which the host reads data is higher than approximately 2.3 Mbytes/s, a ZWAIT/DRQ signal is output by the LC8956. While ZWAIT/DRQ is LOW, ZHRD must not be switched HIGH. During transfer of a single block, the microcomputer waits for the next transfer-complete interrupt.

A DRQ (data request) can also be sent from SELDRQ of the LC8956. This method of data transfer is similar to that using a DMA controller, with the host sending a pulse on ZHRD in response to a data request signal from the LC8956.

When the last byte of data (of the data block size set by the controller) is read, ZEOP becomes active, read pulses are output, ZDTEN becomes inactive, and a transfer-complete interrupt is then issued, signalling to the control microcomputer the end of data transfer to the host.

The LC8956 control microcomputer passes decoded data requests and CD-ROM drive status information to the 12-byte status register. Handshaking between the microcomputer and host is accomplished by ZSTEN signals. Note that the LC8956 cannot control or alter the contents of this status register, allowing greater freedom in CD-ROM application design.

### **Data/Decode Processing**

Data input and decoding are processed simultaneously using pipeline processing. Writing of input data to buffer RAM, writing and reading of data during decoding, and reading of buffer RAM for transfer to the host all proceed in parallel with synchronization controlled by the LC8956.

#### **ADPCM Decoder**

Error-corrected ADPCM data is sent to the ADPCM decoder block, under microcomputer control. Data transfer is identical to host data transfer. Data is read from the SRAM error correction area and written to the ADPCM data area, read by the ADPCM decoder and then reproduced.

Automatic playback at levels A, B, C and stereo/ monaural playback are possible from subheader data. ADPCM data temporarily stored with the host can also be played back.

CD-DA data can be output from the audio output terminal by setting an internal register. An internal register can also be set to enable digital muting during ADPCM playback only.

The LC8956 supports direct connection with Sanyo's LC7883K 8-times oversampling digital filter and D/A converter.

#### SUB-code Data Interface

SUB-code data values P through W can be read in parallel by the microcomputer when the LC8956 is connected to the SUB-CODE terminal of a CD-DSP. A Q-code CRC check function is also supported.

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