

Overview

The LC89972M is a CCD delay line for PAL television systems. It incorporates a comb filter for chrominance signal and a 1H delay line for luminance signal.

Structure

NMOS + CCD

Functions

- Two CCD shift registers (for chrominance and luminance signals)
- CCD drive circuits
- CCD stage count switching circuit
- CCD signal adder
- Auto-bias circuit
- Sync tip clamping circuit (luminance signal)
- Center-bias circuit (chrominance signal)
- · Sample-and-hold circuit
- PLL 3 × frequency multiplier
- 3 fsc clock output circuit
- · RD voltage generator

Features

- 5 V single-voltage power supply
- Built-in PLL 3 × frequency multiplier circuit allows 3 fsc operation from an fsc (4.43 MHz) input.
- Control pin switchable to handle PAL/GBI and 4.43 MHz NTSC systems.
- Built-in chrominance signal crosstalk exclusion comb filter features high-precision comb characteristics in an adjustment-free circuit.
- Built-in peripheral circuits allow applications to be constructed with a minimum number of external components.
- Positive-phase signal input/positive-phase signal output (luminance signal)

Specifications Absolute MaxImum Ratings at Ta = 25°C

Parameter Symbol Conditions Ratings Unit Maximum supply voltage V_{DD} max -0.3 to +6.0 v Pd max Allowable power dissipation 600 mW Operating temperature Topr -10 to +70 ۰C Tstg Storage temperature -55 to +150 °C

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Package Dimensions

unit: mm 3045B-MFP24



Allowable Operating Ranges at Ta = 25°C

| Parameter | Symbol | Conditions | min | typ | max | Unit |
|----------------------------------|-------------------|------------|------|------------|--------|-------|
| Supply voltage | V _{DD} | | 4.75 | 5.00 | 5.25 | v |
| Clock input amplitude | V _{CLK} | | 300 | 500 | 1000 | mVp-p |
| Clock frequency | FCLK | Sine wave | | 4.43361875 | — — | MHz |
| Clock signal input amplitude | V _{IN-C} | | - | 350 | 500 | mVp-p |
| Luminance signal input amplitude | V _{IN-Y} | | - | 400 | 572 | mVp-p |

Electrical Characteristics at Ta = 25°C, V_{DD} = 5.0 V, F_{CLK} = 4.43361875 MHz, V_{CLK} = 500 mVp-p

| Deveryotes | 0 | Switch states | | | 0 | <u> </u> | 1 | | <u> </u> |
|---------------------------|-----------------------|---------------|-----|------|------------|----------|-----|------|----------|
| Parameter | Symbol | SW1 | SW2 | SW3 | Conditions | min | typ | max | Unit |
| Supply surgest | IDD-1 | a | а | b | 1 | 40 | 50 | 60 | mA |
| Supply current | IDD-2 | b | a | b | | | | | |
| Chrominance System Charac | teristics (with no Y- | IN input) | | | | | | | |
| | VINC-1 | a | a | b | | 2.0 | 2.4 | 2.8 | v |
| Pin voltage (input) | VINC-2 | Ь | a | b | 2 | 2.0 | 2.4 | | |
| Pin voltage (output) | V _{OUTC-1} | a | а | b | 2 | 1.2 | 1.6 | 2.0 | v |
| Fill voltage (output) | V _{OUTC-2} | Ь | a | b | | 1.2 | | | |
| Voltage gain | G _{VC-1} | a | а | b | 3 | -2 | 0 | +2 | đB |
| | G _{VC-2} | þ | a | b | | | | | |
| Comb depth | C _{D-1} | a | a | b | 4 | | -40 | -35 | dB |
| | С _{D-2} | b | a | b | | | | | |
| Linearity | L _{NC-1} | a | a | b | 5 | -0.3 | 0.0 | +0.3 | dB |
| Lateanty | L _{NC-2} | b | a | b | | | | | |
| Clock leakage (3 fsc) | L _{CK3C-1} | a | а | b | | | 10 | 50 | mVrms |
| Cider isanage (5 isc) | L _{CK3C-2} | b | a | b | 6 | | | | |
| Clock leakage (fsc) | L _{CK1C-1} | a | а | b | 0 | - | 0.8 | 1.5 | mVrms |
| CIOCK IBARAYA (ISC) | L _{CK1C-2} | b | а | b | | | | | |
| Noise | N _{C-1} | а | а | b | 7 | | 0.5 | 2.0 | mVrms |
| NOISE | N _{C-2} | b | а | b | / | | | | |
| Output impedance | Z _{OC-1} | a | a | a, b | 8 | 200 | 350 | 500 | Ω |
| Corbor imbendince | Z _{OC-2} | b | a | a, b | ö | | | | |
| 0 H delay time | T _{DC-1} | a | a | b | 9 | | 245 | - | ns |
| on deray time | T _{DC-2} | b | a | b | 8 | | | | |

Continued from preceding page.

| Parameter | | Switch states | | | <u> </u> | | [| | |
|---------------------------|-----------------------|---------------|--------|------|---------------------------------------|------------|-------|-----|-------|
| | Symbol | SW1 | SW2 | SW3 | Conditions | min | typ | max | Unit |
| Luminance System Characte | ristics (with no C-IN | 1 or C-IN2 | input) | | | - - | | | |
| Pin voltage (input) | V _{INY-1} | a | a | Þ | | | 2.1 | 2.5 | v |
| | V _{INY-2} | b | a | b | 10 | 1.7 | | | |
| Pin voltage (output) | V _{OUTY-1} | 8 | a | b | | | | 1.6 | v |
| | V _{OUTY-2} | b | a | b | | 0.8 | 1.2 | | |
| Voltage gain | G _{VY-1} | a | a | b | 11 | -2 | 0 | +2 | dB |
| vonage gam | G _{VY-2} | b | a | b | 14 | | | | |
| Frequency response | G _{FY-1} | a | b | Ъ | 12 | -2 | 0 | +2 | dB |
| | G _{FY-2} | b | b | b | | | | | |
| Differential gain | D _{GY-1} | а | а | b | 13 | 0 | 5 | 7 | % |
| | D _{GY-2} | b | a | b | | | | | |
| Differential phase | D _{PY-1} | a | a | b | | 0 | 5 | 7 | deg |
| Emerential priese | D _{PY-2} | b | a | b | | | | | |
| Linearity | L _{SY-1} | a | a | b | 14 | 37 | 40 | 43 | % |
| Enounty | L _{SY-2} | b | a | b | | | | | |
| Clock leakage (3 fsc) | LCK3Y-1 | a | a | b | · · · · · · · · · · · · · · · · · · · | | 10 | 50 | mVrms |
| Olock loakage (o lac) | L _{CK3Y-2} | b | a | b | 15 | | | | |
| Clock leakage (fsc) | LCK1Y-1 | a | a | b | 15 | - | 0.8 | 1.5 | mVrms |
| Olden Idanago (ISC) | L _{CK1Y-2} | b | a | b | | | | | |
| Noise | N _{Y-1} | а | a | b | 16 | | 0.5 | 2.0 | mVrms |
| | N _{Y-2} | b | a | b | | | | | |
| Output impedance | Z _{OY-1} | a | a | c, b | 17 | 250 | 400 | 550 | |
| oorbot impedance | Z _{OY-2} | b | a | c, b | | | | | Ω |
| Delay time | T _{DY-1} | a | а | b | 18 | _ | 63.92 | | μs |
| Print mint | T _{DY-2} | b | a | b | 10 | _ | 63.47 | | |

Test Conditions

- 1. Supply current with no signal input
- 2. C-OUT voltage (center bias voltage) with no signal input.
- 3. Measure the C-OUT output with 350 mVp-p sine wave signals input to C-IN1 and C-IN2.

$$G_{VC} = 20 \log \frac{C-OUT \text{ output } [mVp-p]}{350 \ [mVp-p]} \ [dB]$$

Test frequencies

G_{VC}-1 4.429662 MHz (PAL/GBI) G_{VC}-2 4.425694 MHz (4.43 NTSC)

4. Measure the comb depth from the C-OUT output with a 350 mVp-p sine wave signal of frequency fa input to C-IN1 and C-IN2 and with a frequency of fb input.

 $C_{D} = 20 \log \frac{C-OUT \text{ output with fb input } [mVp-p]}{C-OUT \text{ output with fa input } [mVp-p]} \text{ [dB]}$

Test frequencies

| | fa | fb |
|-------------------|--------------|--------------------------|
| C _D -1 | 4.429662 MHz | 4.425756 MHz (PAL/GBI) |
| C _D -2 | 4.425694 MHz | 4.417819 MHz (4.43 NTSC) |



5. Measure the C-OUT output with a 200 mVp-p sine wave signal input to C-IN1 and C-IN2 and with 500 mVp-p sine wave signal input and calculate the difference in the gains.

 $L_{NC} = 20 \log \left(\frac{\text{Output for a 500 mVp-p input [mVp-p]}}{500 [mVp-p]} / \frac{\text{Output for a 200 mVp-p input [mVp-p]}}{200 [mVp-p]} \right) \text{ [dB]}$

Test frequencies

- L_{NC}-1 4.429662 MHz (PAL/GBI) L_{NC}-2 4.425694 MHz (4.43 NTSC)
- 6. Measure the 3 fsc (13.3 MHz) and fsc (4.43 MHz) components in the C-OUT output with no input.
- Measure the noise in the C-OUT output with no input. Measure the noise with a noise meter set up with a 200 kHz high-pass filter and a 5 MHz low-pass filter.
- Let V1 be the C-OUT output with a 350 mVp-p sine wave input to C-IN1 and C-IN2 and SW3 set to a, and let V2 be the C-OUT output with SW3 set to b.

$$Z_{OC} = \frac{V2 [mVp-p] - V1 [mVp-p]}{V1 [mVp-p]} \times 500 [\Omega]$$

Test frequencies

Z_{OC}-1 4.429662 MHz (PAL/GBI) Z_{OC}-2 4.425694 MHz (4.43 NTSC)

9. The C-OUT output delay time with respect to inputs to C-IN1. (the CCD 2.5 bit delay)

10. Y-OUT voltage (clamp voltage) with no signal input.

11. Measure the Y-OUT output with a 200 kHz 400 mVp-p sine wave input to Y-IN.

 $G_{VY} = 20 \log \frac{\text{Y-OUT output [mVp-p]}}{400 \text{ [mVp-p]}} \text{ [dB]}$

12. Measure the Y-OUT output with a 200 kHz 200 mVp-p sine wave input to Y-IN and with a 3.3 MHz 200 mVp-p sine wave input.

 $G_{FY} = 20 \log \frac{Y \text{-}OUT \text{ output with a 3.3 MHz input } [mVp-p]}{Y \text{-}OUT \text{ output with a 200 kHz input } [mVp-p]} \text{ [dB]}$

Note that V_{bias} should be adjusted so that the circuit is biased to the clamp level plus 250 mV.

13. Input a five-level step waveform (see the figure below) to Y-IN and measure the differential gain and differential phase in the Y-OUT output with a vector scope.



14. Input a five-level step waveform (see the figure below) to Y-IN and measure the luminance level (Y) and the sync level (S) in the Y-OUT output.



- 15. Measure the 3 fsc (13.3 MHz) and fsc (4.43 MHz) components in the Y-OUT output with no input.
- 16. Measure the noise in the Y-OUT output with no input. Measure the noise with a noise meter set up with a 200 kHz high-pass filter, a 5 MHz low-pass filter and a 4.43 MHz trap filter.
- 17. Let V1 be the Y-OUT output with a 200 kHz 400 mVp-p sine wave input and SW3 set to c, and let V2 be the C-OUT output with SW3 set to b.

$$Z_{OY} = \frac{V2 [mVp-p] - V1 [mVp-p]}{V1 [mVp-p]} \times 500 [Ω]$$

18. The Y-OUT delay time with respect to Y-IN

Block Dlagram



Control Pln Function

| CONT | Mode (representative example) | Chrominance signal delay (CCD bits) | Luminance signal delay (CCD bits) | | |
|------|-------------------------------|--|--------------------------------------|--|--|
| Low | PAL/GBI | 2 H (1705) + 0 H (2.5) | 1 H (849.5) | | |
| High | 4.43 NTSC | 1 H (847) + 0 H (2.5) | 1 H (843.5) | | |

Switching Voltage Levels

| Low/high | Symbol | min | typ | max | Unit |
|----------|----------------|------|-----|------|------|
| Low | V _L | -0.3 | 0.0 | +0.5 | V |
| High | V _H | 2.0 | 5.0 | 6.0 | V |

Note: Since the control pin has a built-in pull-down resistor, the pin will be set to the low state if left open.

VCO OUT PIn Function

This pin outputs the 3 fsc clock generated by the PLL 3 × frequency multiplier circuit.



Test Circuit



Pin Assignment



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