National Semiconductor

Quad SPST JFET Analog Switches

LF11331, LF13331 4 Normally Open Switches with Disable
LF11332, LF13332 4 Normally Closed Switches with Disable
LF11333, LF13333 2 Normally Closed Switches and 2 Normally Open Switches with Disable
LF11201, LF13201 4 Normally Closed Switches
LF11202, LF13202 4 Normally Open Switches

General Description

These devices are a monolithic combination of bipolar and JFET technology producing the industry's first one chip quad JFET switch. A unique circuit technique is employed to maintain a constant resistance over the analog voltage range of ±10V. The input is designed to operate from minimum TTL levels, and switch operation also ensures a break-before-make action.

These devices operate from ±15V supplies and swing a ±10V analog signal. The JFET switches are designed for applications where a dc to medium frequency analog signal needs to be controlled.

Features

- Analog signals are not loaded
- Constant "ON" resistance for signals up to ±10V and 100 kHz
- Pin compatible with CMOS switches with the advantage of blow out free handling
- Small signal analog signals to 50 MHz
- Break-before-make action $t_{OFF} < t_{ON}$
- High open switch isolation at 1.0 MHz −50 dB
- Low leakage in "OFF" state <1.0 nA
- TTL, DTL, RTL compatibility
- Single disable pin opens all switches in package on LF11331, LF11332, LF11333
- LF11201 is pin compatible with DG201

Test Circuit and Schematic Diagram

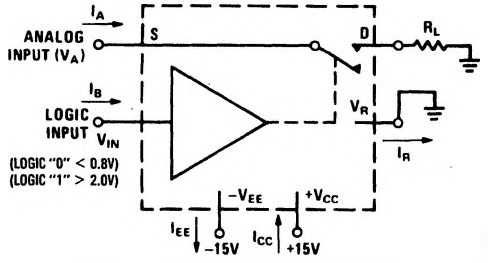

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FIGURE 1. Typical Circuit for One Switch

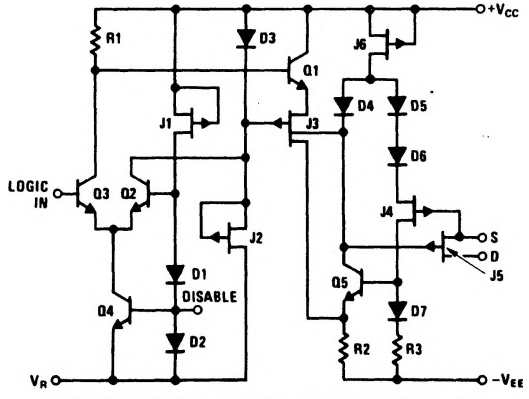

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FIGURE 2. Schematic Diagram (Normally Open)

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications. (Note 1)

Supply Voltage ($V_{CC}-V_{EE}$)	36V
Reference Voltage	$V_{EE} \le V_R \le V_{CC}$
Logic Input Voltage	$V_R-4.0V \le V_{IN} \le V_R+6.0V$
Analog Voltage	$V_{EE} \le V_A \le V_{CC}+6V$; $V_A \le V_{EE}+36V$
Analog Current	$\|I_A\| < 20$ mA

Power Dissipation (Note 2)	
Molded DIP (N Suffix)	500 mW
Cavity DIP (D Suffix)	900 mW
Operating Temperature Range	
LF11201, 2 and LF11331, 2, 3	−55°C to +125°C
LF13201, 2 and LF13331, 2, 3	0°C to +70°C
Storage Temperature	−65°C to +150°C
Soldering Information	
N and D Package (10 sec.)	300°C
SO Package	
Vapor Phase (60 sec.)	215°C
Infrared (15 sec.)	220°C

Electrical Characteristics (Note 3)

Symbol	Parameter	Conditions		LF11331/2/3 LF11201/2			LF13331/2/3 LF13201/2			Units
				Min	Typ	Max	Min	Typ	Max	
R_{ON}	"ON" Resistance	$V_A=0$, $I_D=1$ mA	$T_A=25°C$		150	200		150	250	Ω
					200	300		200	350	Ω
R_{ON} Match	"ON" Resistance Matching		$T_A=25°C$		5	20		10	50	Ω
V_A	Analog Range			±10	±11		±10	±11		V
$I_{S(ON)}$ + $I_{D(ON)}$	Leakage Current in "ON" Condition	Switch "ON," $V_S=V_D=\pm10V$	$T_A=25°C$		0.3	5		0.3	10	nA
					3	100		3	30	nA
$I_{S(OFF)}$	Source Current in "OFF" Condition	Switch "OFF," $V_S=+10V$, $V_D=-10V$	$T_A=25°C$		0.4	5		0.4	10	nA
					3	100		3	30	nA
$I_{D(OFF)}$	Drain Current in "OFF" Condition	Switch "OFF," $V_S=+10V$, $V_D=-10V$	$T_A=25°C$		0.1	5		0.1	10	nA
					3	100		3	30	nA
V_{INH}	Logical "1" Input Voltage			2.0			2.0			V
V_{INL}	Logical "0" Input Voltage					0.8			0.8	V
I_{INH}	Logical "1" Input Current	$V_{IN}=5V$	$T_A=25°C$		3.6	10		3.6	40	μA
						25			100	μA
I_{INL}	Logical "0" Input Current	$V_{IN}=0.8$	$T_A=25°C$			0.1			0.1	μA
						1			1	μA
t_{ON}	Delay Time "ON"	$V_S=\pm10V$, *(Figure 3)*	$T_A=25°C$		500			500		ns
t_{OFF}	Delay Time "OFF"	$V_S=\pm10V$, *(Figure 3)*	$T_A=25°C$		90			90		ns
$t_{ON}-t_{OFF}$	Break-Before-Make	$V_S=\pm10V$, *(Figure 3)*	$T_A=25°C$		80			80		ns
$C_{S(OFF)}$	Source Capacitance	Switch "OFF," $V_S=\pm10V$	$T_A=25°C$		4.0			4.0		pF
$C_{D(OFF)}$	Drain Capacitance	Switch "OFF," $V_D=\pm10V$	$T_A=25°C$		3.0			3.0		pF
$C_{S(ON)}$ + $C_{D(ON)}$	Active Source and Drain Capacitance	Switch "ON," $V_S=V_D=0V$	$T_A=25°C$		5.0			5.0		pF
$I_{SO(OFF)}$	"OFF" Isolation	*(Figure 4)*, (Note 4)	$T_A=25°C$		−50			−50		dB
CT	Crosstalk	*(Figure 4)*, (Note 4)	$T_A=25°C$		−65			−65		dB
SR	Analog Slew Rate	(Note 5)	$T_A=25°C$		50			50		V/μs
I_{DIS}	Disable Current	*(Figure 5)*, (Note 6)	$T_A=25°C$		0.4	1.0		0.6	1.5	mA
					0.6	1.5		0.9	2.3	mA
I_{EE}	Negative Supply Current	All Switches "OFF," $V_S=\pm10V$	$T_A=25°C$		3.0	5.0		4.3	7.0	mA
					4.2	7.5		6.0	10.5	mA
I_R	Reference Supply Current	All Switches "OFF," $V_S=\pm10V$	$T_A=25°C$		2.0	4.0		2.7	5.0	mA
					2.8	6.0		3.8	7.5	mA
I_{CC}	Positive Supply Current	All Switches "OFF," $V_S=\pm10V$	$T_A=25°C$		4.5	6.0		7.0	9.0	mA
					6.3	9.0		9.8	13.5	mA

Note 1: Refer to RETSF11201X, RETSF11331X, RETSF11332X and RETSF11333X for military specifications.

Note 2: For operating at high temperature the molded DIP products must be derated based on a +100°C maximum junction temperature and a thermal resistance of +150°C/W, devices in the cavity DIP are based on a +150°C maximum junction temperature and are derated at ±100°C/W.

Note 3: Unless otherwise specified, $V_{CC}=+15V$, $V_{EE}=-15V$, $V_R=0V$, and limits apply for $-55°C \le T_A \le +125°C$ for the LF11331/2/3 and the LF11201/2, $-25°C \le T_A \le +85°C$ for the LF13331/2/3 and the LF13201/2.

Note 4: These parameters are limited by the pin to pin capacitance of the package.

Note 5: This is the analog signal slew rate above which the signal is distorted as a result of finite internal slew rates.

Note 6: All switches in the device are turned "OFF" by saturating a transistor at the disable node as shown in *Figure 5*. The delay time will be approximately equal to the t_{ON} or t_{OFF} plus the delay introduced by the external transistor.

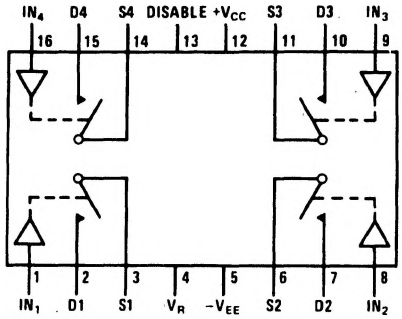
Note 7: This graph indicates the analog current at which 1% of the analog current is lost when the drain is positive with respect to the source.

Note 8: θ_{JA} (Typical) Thermal Resistance

Molded DIP (N)	85°C/W
Cavity DIP (D)	100°C/W
Small Outline (M)	105°C/W

Connection Diagrams (Top View for SO and Dual-In-Line Packages) (All Switches Shown are For Logical "0")

LF11331/LF13331



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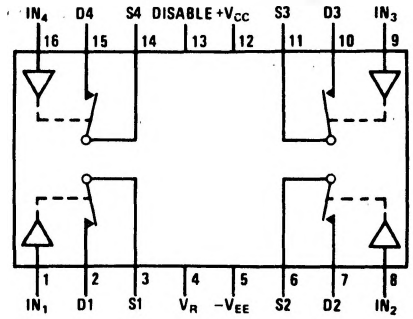
LF11332/LF13332



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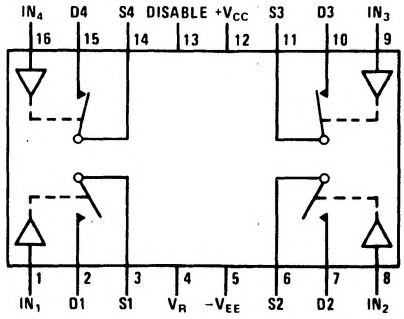
LF11333/LF13333



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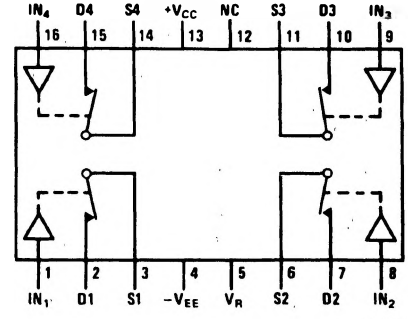
LF11201/LF13201



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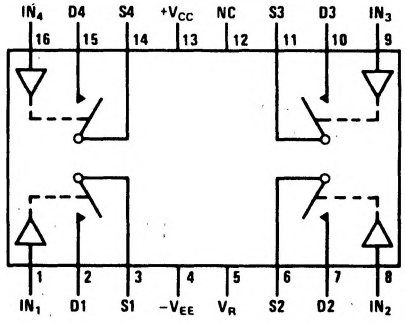
LF11202/LF13202



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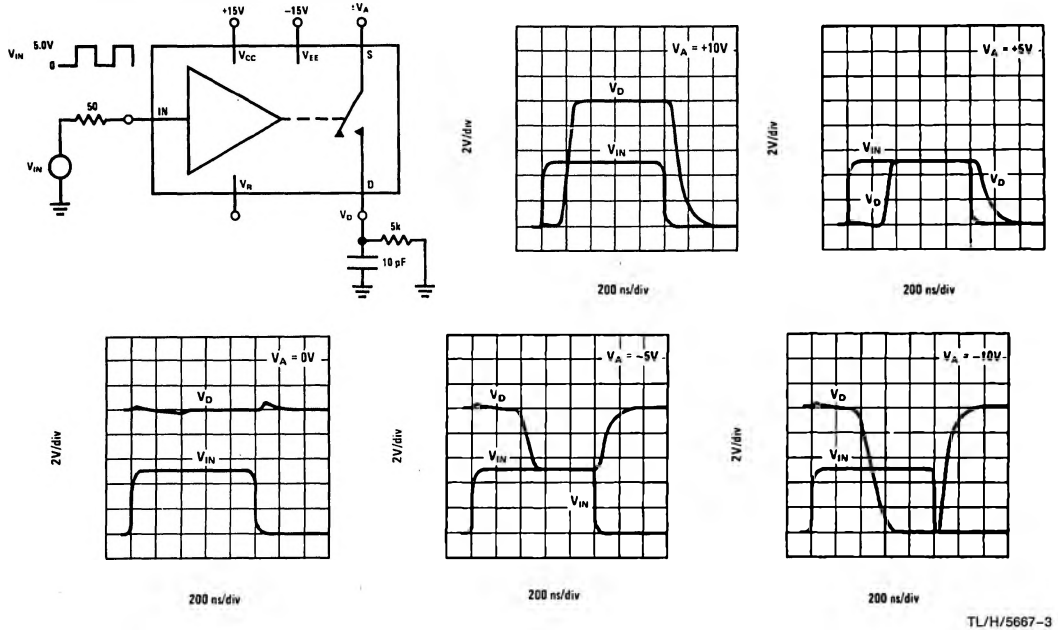
Order Number LF13201D, LF11201D, LF11201D/883, LF13202D, LF11202D, LF11202D/883, LF13331D, LF11331D, LF11331D/883, LF13332D, LF11332D, LF11332D/883, LF13333D, LF11333D or LH11333D/883
See NS Package Number D16C

Order Number LF13201M, LF13202M, LF13331M, LF13332M or LF13333M
See NS Package Number M16A

Order Number LF13201N, LF13202N, LF13331N, LF13332N or LF13333N
See NS Package Number N16A

Test Circuit and Typical Performance Curves

Delay Time, Rise Time, Settling Time, and Switching Transients



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Additional Test Circuits

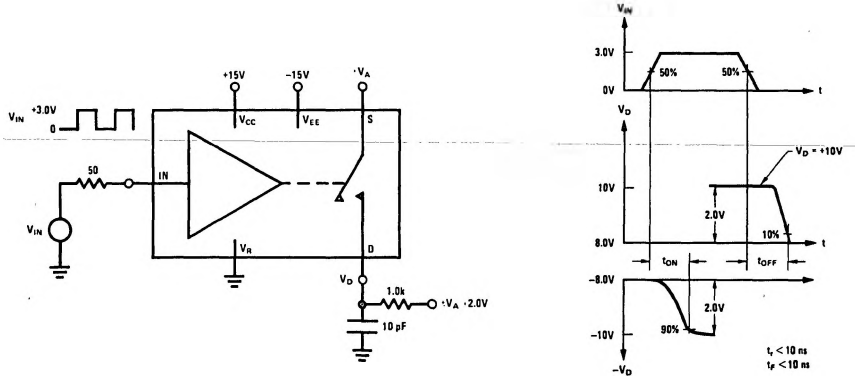

FIGURE 3. t_{ON}, t_{OFF} Test Circuit and Waveforms for a Normally Open Switch

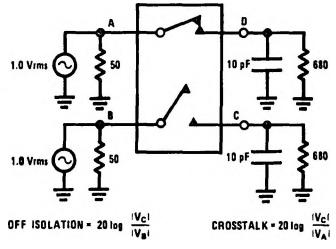

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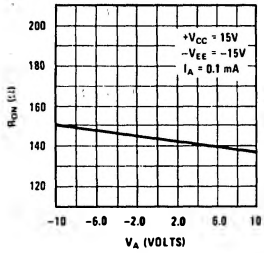
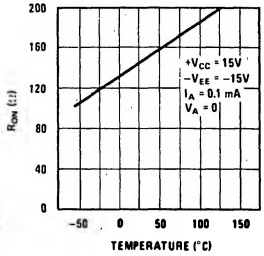
FIGURE 4. "OFF" Isolation, Crosstalk, Small Signal Response

Typical Performance Characteristics

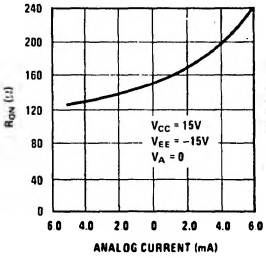
"ON" Resistance



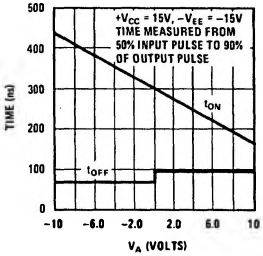
"ON" Resistance



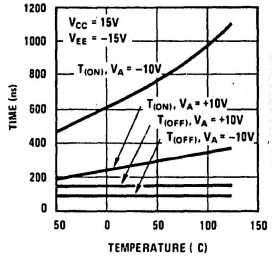
"ON" Resistance



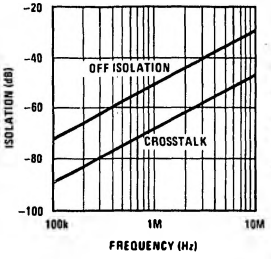
Break-Before-Make Action



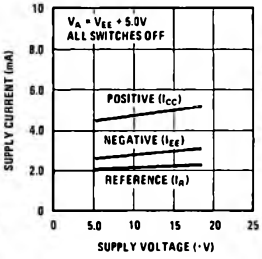
Switching Times



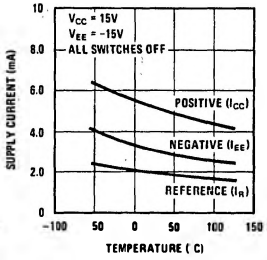
Crosstalk and "OFF" Isolation vs Frequency Using Test Circuit of *Figure 5*



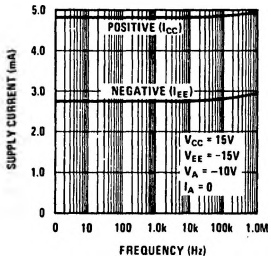
Supply Current



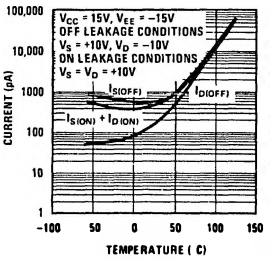
Supply Current



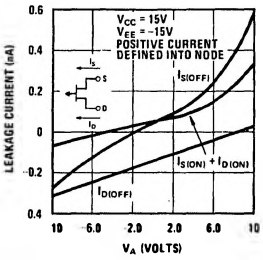
Supply Current



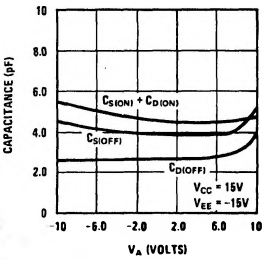
Switch Leakage Currents



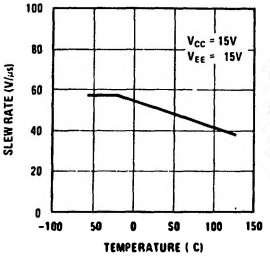
Switch Leakage Current



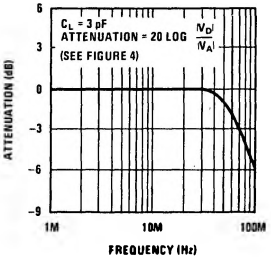
Switch Capacitances



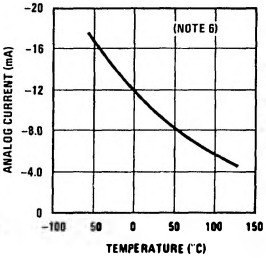
Slew Rate of Analog Voltage Above Which Signal Loading Occurs



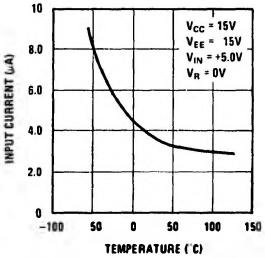
Small Signal Response



Maximum Accurate Analog Current vs Temperature



Logical "1" Input Bias Current



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Application Hints

GENERAL INFORMATION

These devices are monolithic quad JFET analog switches with "ON" resistances which are essentially independent of analog voltage or analog current. The leakage currents are typically less than 1 nA at 25°C in both the "OFF"and "ON" switch states and introduce negligible errors in most applications. Each switch is controlled by minimum TTL logic levels at its input and is designed to turn "OFF" faster than it will turn "ON." This prevents two analog sources from being transiently connected together during switching. The switches were designed for applications which require break-before-make action, no analog current loss, medium speed switching times and moderate analog currents.

Because these analog switches are JFET rather than CMOS, they do not require special handling.

LOGIC INPUTS

The logic input (IN), of each switch, is referenced to two forward diode drops (1.4V at 25°C) from the reference supply (V_R) which makes it compatible with DTL, RTL, and TTL logic families. For normal operation, the logic "0" voltage can range from 0.8V to −4.0V with respect to V_R and the logic "1" voltage can range from 2.0V to 6.0V with respect to V_R, provided V_{IN} is not greater than (V_{CC}−2.5V). If the input voltage is greater than (V_{CC} −2.5V), the input current will increase. If the input voltage exceeds 6.0V or −4.0V with respect to V_R, a resistor in series with the input should be used to limit the input current to less than 100μA.

ANALOG VOLTAGE AND CURRENT

Analog Voltage

Each switch has a constant "ON" resistance (R_{ON}) for analog voltages from (V_{EE}+5V) to (V_{CC}−5V). For analog voltages greater than (V_{CC}−5V), the switch will remain ON independent of the logic input voltage. For analog voltages less than (V_{EE}+5V), the ON resistance of the switch will increase. Although the switch will not operate normally when the analog voltage is out of the previously mentioned range, the source voltage can go to either (V_{EE}+36V) or (V_{CC}+6V), whichever is more positive, and can go as negative as V_{EE} without destruction. The drain (D) voltage can also go to either (V_{EE}+36V) or (V_{CC}+6V), whichever is more positive, and can go as negative as (V_{CC}−36V) without destruction.

Analog Current

With the source (S) positive with respect to the drain (D), the R_{ON} is constant for low analog currents, but will increase at higher currents (>5 mA) when the FET enters the saturation region. However, if the drain is positive with respect to the source and a small analog current loss at high analog currents (Note 6) is tolerable, a low R_{ON} can be maintained for analog currents greater than 5 mA at 25°C.

LEAKAGE CURRENTS

The drain and source leakage currents, in both the ON and the OFF states of each switch, are typically less than 1 nA at 25°C and less than 100 nA at 125°C. As shown in the typical curves, these leakage currents are Dependent on power supply voltages, analog voltage, analog current and the source to drain voltage.

DELAY TIMES

The delay time OFF (t_{OFF}) is essentially independent of both the analog voltage and temperature. The delay time ON (t_{ON}) will decrease as either ($V_{CC}-V_A$) decreases or the temperature decreases.

POWER SUPPLIES

The voltage between the positive supply (V_{CC}) and either the negative supply (V_{EE}) or the reference supply (V_R) can be as much as 36V. To accommodate variations in input logic reference voltages, V_R can range from V_{EE} to (V_{CC}−4.5V). Care should be taken to ensure that the power supply leads for the device never become reversed in polarity or that the device is never inadvertantly installed backwards in a test socket. If one of these conditions occurs, the supplies would zener an internal diode to an unlimited current; and result in a destroyed device.

SWITCHING TRANSIENTS

When a switch is turned OFF or ON, transients will appear at the load due to the internal transient voltage at the gate of the switch JFET being coupled to the drain and source by the junction capacitances of the JFET. The magnitude of these transients is dependent on the load. A lower value R_L produces a lower transient voltage. A negative transient occurs during the delay time ON, while a positive transient occurs during the delay time OFF. These transients are relatively small when compared to faster switch families.

DISABLE NODE

This node can be used, as shown in *Figure 5*, to turn all the switches in the unit off independent of logic inputs. Normally, the node floats freely at an internal diode drop (≈0.7V) above V_R. When the external transistor in *Figure 5* is saturated, the node is pulled very close to V_R and the unit is disabled. Typically, the current from the node will be less than 1 mA. This feature is not available on the LF11201 or LF11202 series.

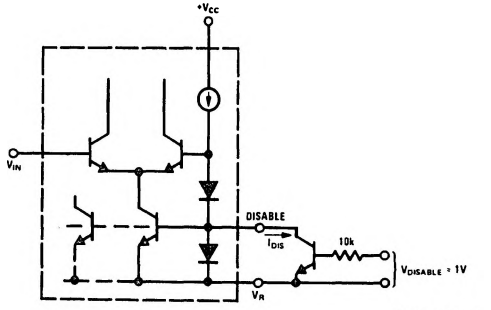

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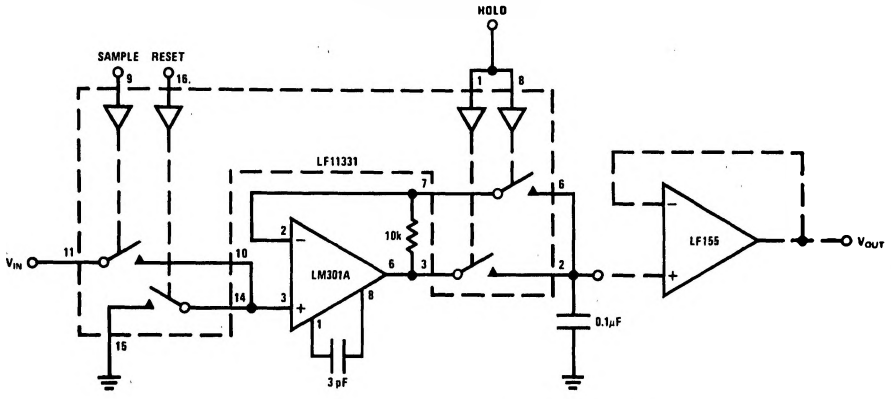
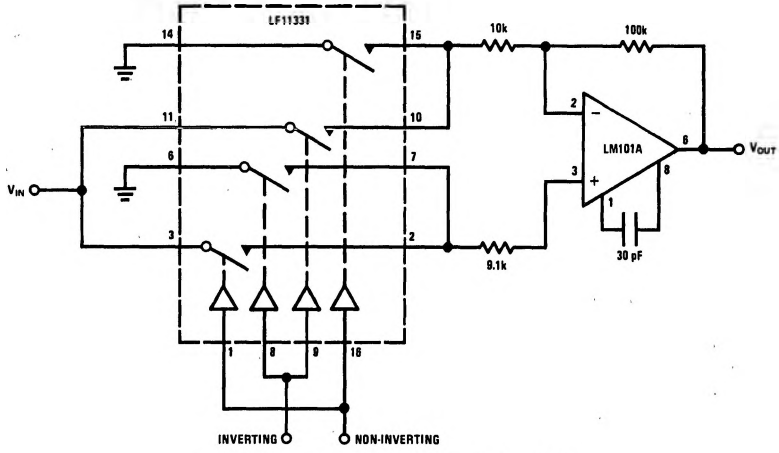
FIGURE 5. Disable Function

Typical Applications

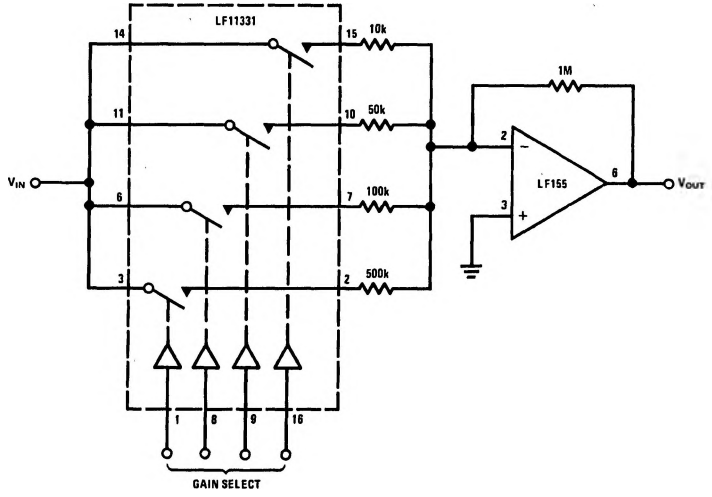
Sample and Hold with Reset



Programmable Inverting Non-Inverting Operational Amplifier



Programmable Gain Operational Amplifier



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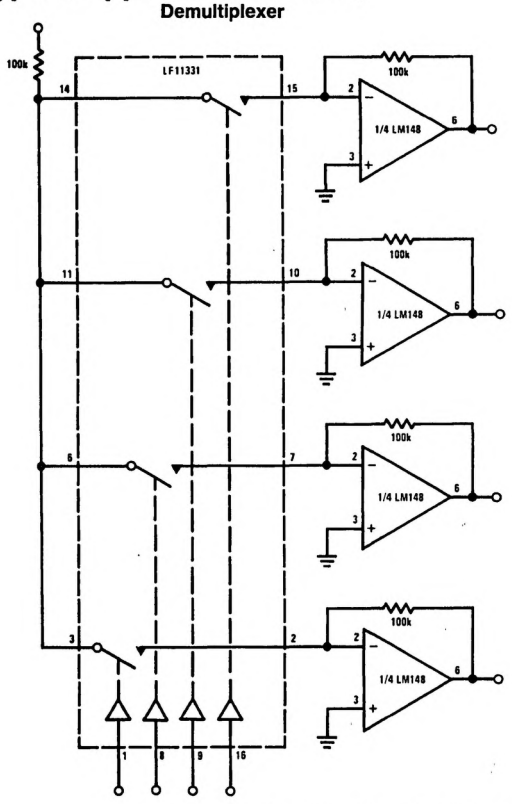
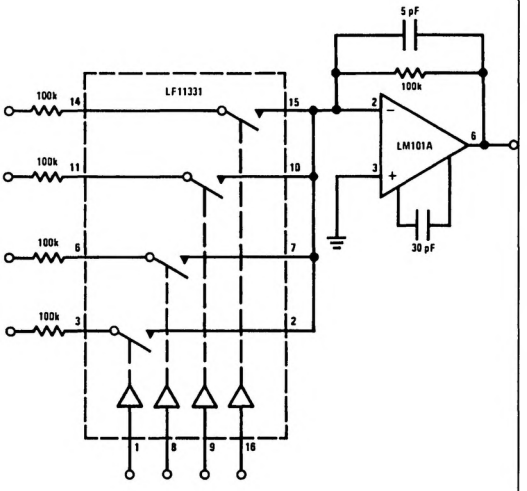
Typical Applications (Continued)

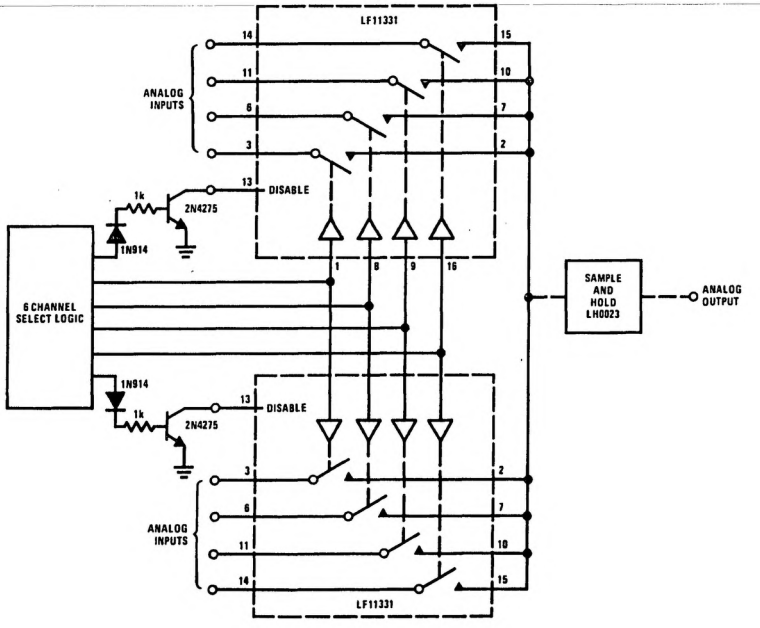
Demultiplexer



Multiplexer/Mixer



8-Channel Analog Commutator with 6-Channel Select Logic



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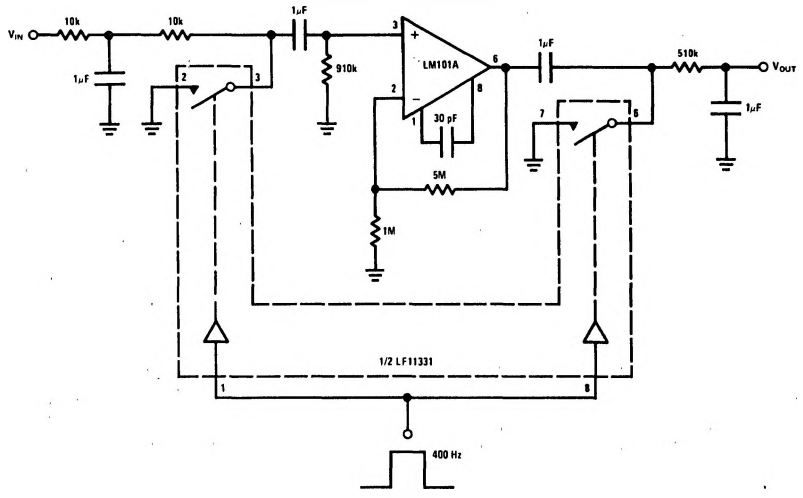
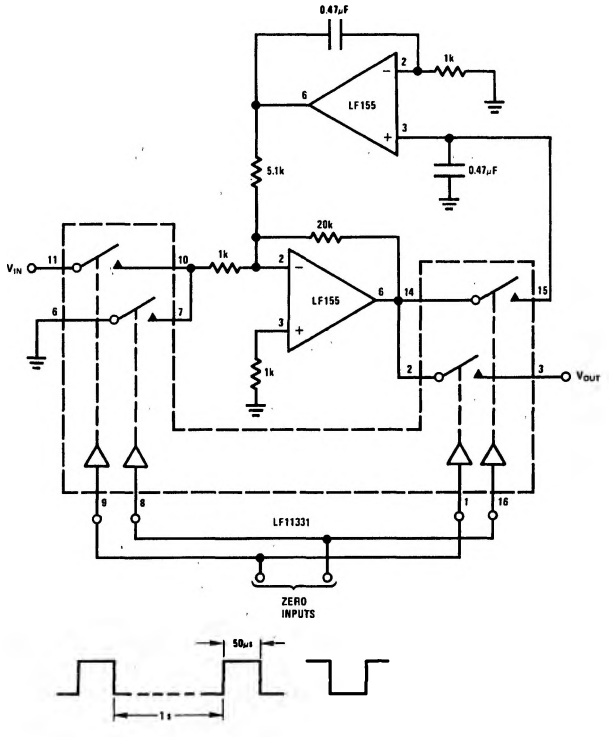
Typical Applications (Continued)

Chopper Channel Amplifier



Self-Zeroing Operational Amplifier



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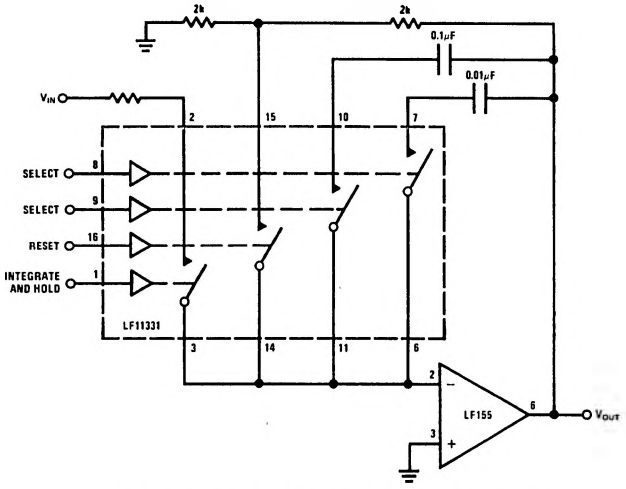
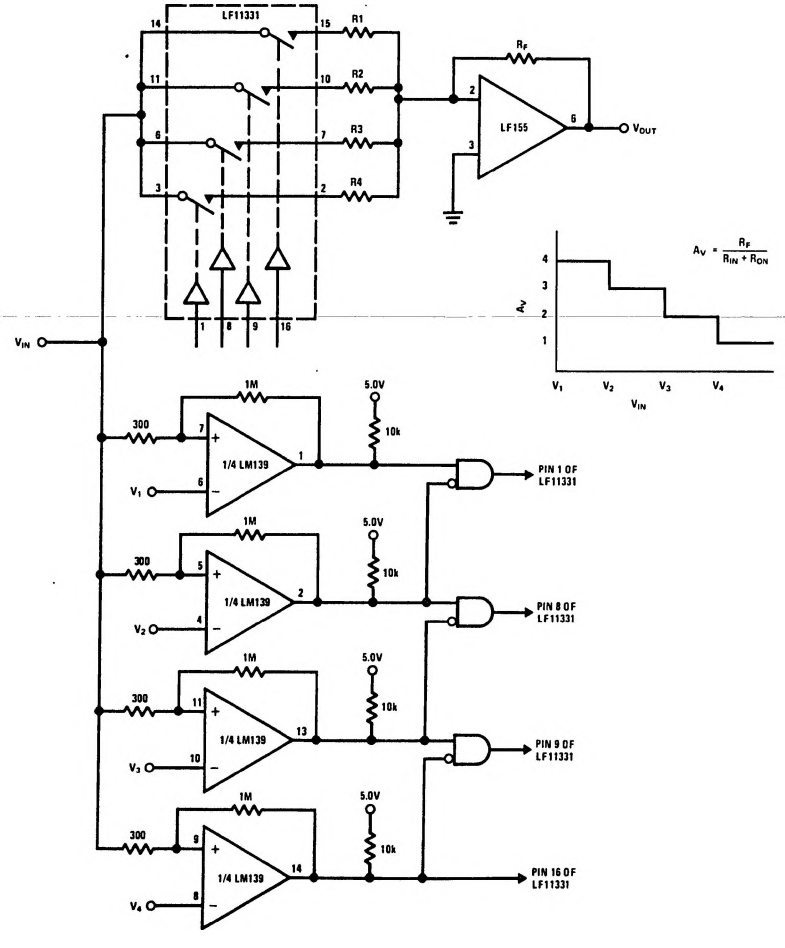
Typical Applications (Continued)

Programmable Integrator with Reset and Hold



Staircase Transfer Function Operational Amplifier



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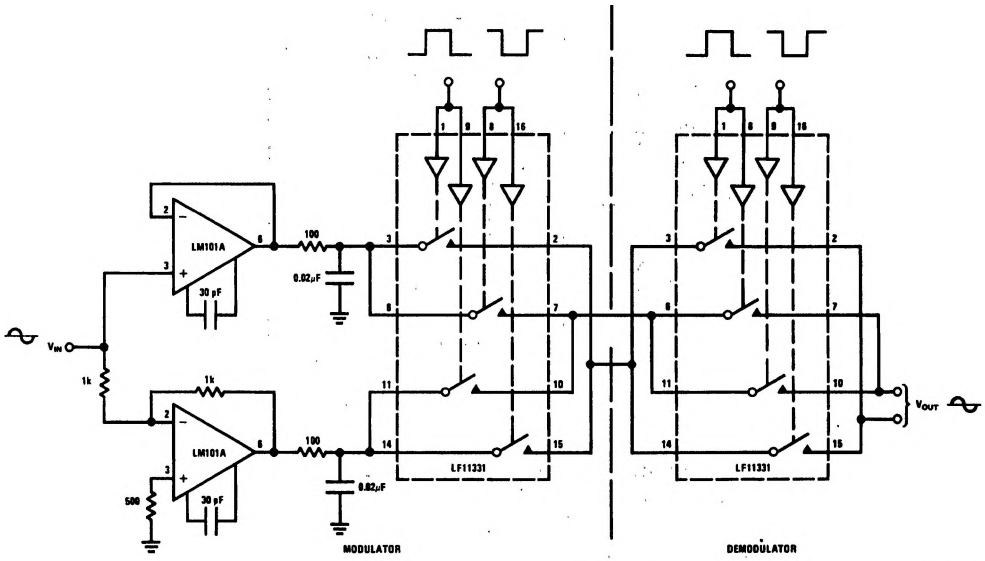
Typical Applications (Continued)

DSB Modulator-Demodulator



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