◩ National Semiconductor

LF198/LF298/LF398, LF198A/LF398A
Monolithic Sample and Hold Circuits

General Description

The LF198/LF298/LF398 are monolithic sample and hold circuits which utilize BI-FET technology to obtain ultra-high dc accuracy with fast acquisition of signal and low droop rate. Operating as a unity gain follower, dc gain accuracy is 0.002% typical and acquisition time is as low as 6 μs to 0.01%. A bipolar input stage is used to achieve low offset voltage and wide bandwidth. Input offset adjust is accomplished with a single pin, and does not degrade input offset drift. The wide bandwidth allows the LF198 to be included inside the feedback loop of 1 MHz op amps without having stability problems. Input impedance of $10^{10}\Omega$ allows high source impedances to be used without degrading accuracy.

P-channel junction FET's are combined with bipolar devices in the output amplifier to give droop rates as low as 5 mV/min with a 1 μF hold capacitor. The JFET's have much lower noise than MOS devices used in previous designs and do not exhibit high temperature instabilities. The overall design guarantees no feed-through from input to output in the hold mode, even for input signals equal to the supply voltages.

Features

■ Operates from ±5V to ±18V supplies
■ Less than 10 μs acquisition time
■ TTL, PMOS, CMOS compatible logic input
■ 0.5 mV typical hold step at $C_h = 0.01$ μF
■ Low input offset
■ 0.002% gain accuracy
■ Low output noise in hold mode
■ Input characteristics do not change during hold mode
■ High supply rejection ratio in sample or hold
■ Wide bandwidth

Logic inputs on the LF198 are fully differential with low input current, allowing direct connection to TTL, PMOS, and CMOS. Differential threshold is 1.4V. The LF198 will operate from ±5V to ±18V supplies. It is available in an 8-lead TO-5 package.

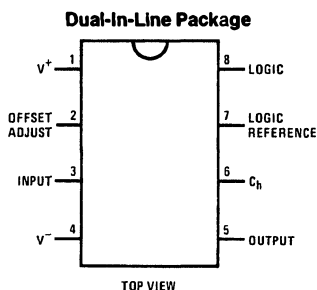An "A" version is available with tightened electrical specifications.
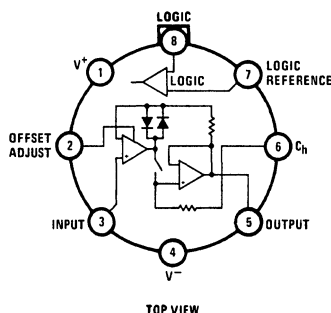
Typical Connection and Performance Curve

Acquisition Time
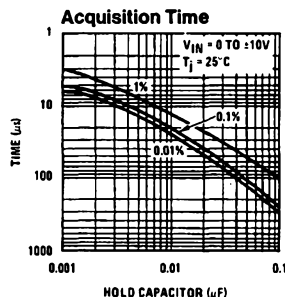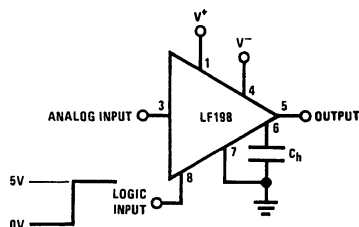
TL/H/5692–2

Connection Diagrams

Dual-In-Line Package

TOP VIEW

Order Number LF398N or LF398AN
See NS Package Number N08E

Metal Can Package

TOP VIEW

TL/H/5692–11

Order Number LF198H, LF298H,
LF398H, LF198AH or LF398AH
See NS Package Number H08C

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	±18V
Power Dissipation (Package Limitation) (Note 1)	500 mW

Operating Ambient Temperature Range

LF198/LF198A	−55°C to +125°C
LF298	−25°C to +85°C
LF398/LF398A	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Input Voltage	Equal to Supply Voltage
Logic To Logic Reference Differential Voltage (Note 2)	+7V, −30V
Output Short Circuit Duration	Indefinite
Hold Capacitor Short Circuit Duration	10 sec
Lead Temperature (Soldering, 10 seconds)	260°C

Thermal Resistance (θ_{JA}) (typicals)

H package	215°C/W (Board mount in still air)
	85°C/W (Board mount in 400LF/min air flow)
N package	115°C/W

θ_{JC} (typical) 20°C/W

Electrical Characteristics (Note 3)

Parameter	Conditions	LF198/LF298			LF398			Units
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage, (Note 6)	$T_j = 25°C$		1	3		2	7	mV
	Full Temperature Range			5			10	mV
Input Bias Current, (Note 6)	$T_j = 25°C$		5	25		10	50	nA
	Full Temperature Range			75			100	nA
Input Impedance	$T_j = 25°C$		10^{10}			10^{10}		Ω
Gain Error	$T_j = 25°C$, $R_L = 10k$		0.002	0.005		0.004	0.01	%
	Full Temperature Range			0.02			0.02	%
Feedthrough Attenuation Ratio at 1 kHz	$T_j = 25°C$, $C_h = 0.01\ \mu F$	86	96		80	90		dB
Output Impedance	$T_j = 25°C$, "HOLD" mode		0.5	2		0.5	4	Ω
	Full Temperature Range			4			6	Ω
"HOLD" Step, (Note 4)	$T_j = 25°C$, $C_h = 0.01\ \mu F$, $V_{OUT} = 0$		0.5	2.0		1.0	2.5	mV
Supply Current, (Note 6)	$T_j \geq 25°C$		4.5	5.5		4.5	6.5	mA
Logic and Logic Reference Input Current	$T_j = 25°C$		2	10		2	10	μA
Leakage Current into Hold Capacitor (Note 6)	$T_j = 25°C$, (Note 5) Hold Mode		30	100		30	200	pA
Acquisition Time to 0.1%	$\Delta V_{OUT} = 10V$, $C_h = 1000$ pF		4			4		μs
	$C_h = 0.01\ \mu F$		20			20		μs
Hold Capacitor Charging Current	$V_{IN} - V_{OUT} = 2V$		5			5		mA
Supply Voltage Rejection Ratio	$V_{OUT} = 0$	80	110		80	110		dB
Differential Logic Threshold	$T_j = 25°C$	0.8	1.4	2.4	0.8	1.4	2.4	V

Electrical Characteristics (Continued) (Note 3)

Parameter	Conditions	LF198A			LF398A			Units
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage, (Note 6)	$T_j = 25°C$		1	1		2	2	mV
	Full Temperature Range			2			3	mV
Input Bias Current, (Note 6)	$T_j = 25°C$		5	25		10	25	nA
	Full Temperature Range			75			50	nA
Input Impedance	$T_j = 25°C$		10^{10}			10^{10}		Ω
Gain Error	$T_j = 25°C, R_L = 10k$		0.002	0.005		0.004	0.005	%
	Full Temperature Range			0.01			0.01	%
Feedthrough Attenuation Ratio at 1 kHz	$T_j = 25°C, C_h = 0.01 \mu F$	86	96		86	90		dB
Output Impedance	$T_j = 25°C$, "HOLD" mode		0.5	1		0.5	1	Ω
	Full Temperature Range			4			6	Ω
"HOLD" Step, (Note 4)	$T_j = 25°C, C_h = 0.01\mu F, V_{OUT} = 0$		0.5	1		1.0	1	mV
Supply Current, (Note 6)	$T_j \geq 25°C$		4.5	5.5		4.5	6.5	mA
Logic and Logic Reference Input Current	$T_j = 25°C$		2	10		2	10	μA
Leakage Current into Hold Capacitor (Note 6)	$T_j = 25°C$, (Note 5) Hold Mode		30	100		30	100	pA
Acquisition Time to 0.1%	$\Delta V_{OUT} = 10V, C_h = 1000$ pF		4	6		4	6	μs
	$C_h = 0.01 \mu F$		20	25		20	25	μs
Hold Capacitor Charging Current	$V_{IN} - V_{OUT} = 2V$		5			5		mA
Supply Voltage Rejection Ratio	$V_{OUT} = 0$	90	110		90	110		dB
Differential Logic Threshold	$T_j = 25°C$	0.8	1.4	2.4	0.8	1.4	2.4	V

Note 1: The maximum junction temperature of the LF198/LF198A is 150°C, for the LF298, 115°C, and for the LF398/LF398A, 100°C. When operating at elevated ambient temperature, the power dissipation must be derated based on a thermal resistance (Θ_{jA}) of 150°C/W.

Note 2: Although the differential voltage may not exceed the limits given, the common-mode voltage on the logic pins may be equal to the supply voltages without causing damage to the circuit. For proper logic operation, however, one of the logic pins must always be at least 2V below the positive supply and 3V above the negative supply.
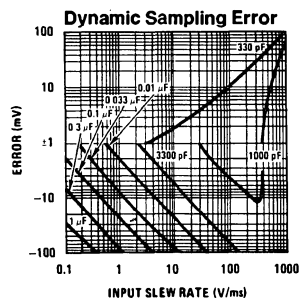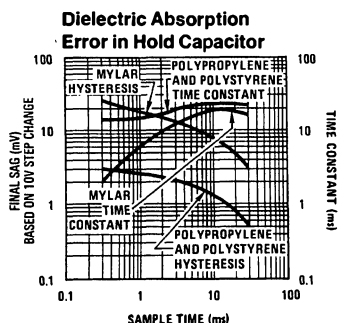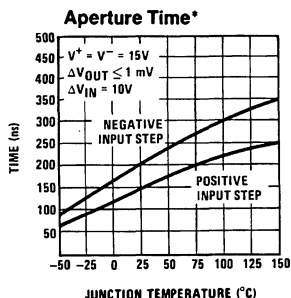
Note 3: Unless otherwise specified, the following conditions apply. Unit is in "sample" mode, $V_S = \pm 15V$, $T_j = 25°C$, $-11.5V \leq V_{IN} \leq +11.5V, C_h = 0.01 \mu F$, and $R_L = 10 k\Omega$. Logic reference voltage = 0V and logic voltage = 2.5V.

Note 4: Hold step is sensitive to stray capacitive coupling between input logic signals and the hold capacitor. 1 pF, for instance, will create an additional 0.5 mV step with a 5V logic swing and a $0.01\mu F$ hold capacitor. Magnitude of the hold step is inversely proportional to hold capacitor value.

Note 5: Leakage current is measured at a *junction* temperature of 25°C. The effects of junction temperature rise due to power dissipation or elevated ambient can be calculated by doubling the 25°C value for each 11°C increase in chip temperature. Leakage is guaranteed over full input signal range.
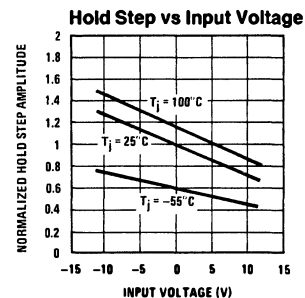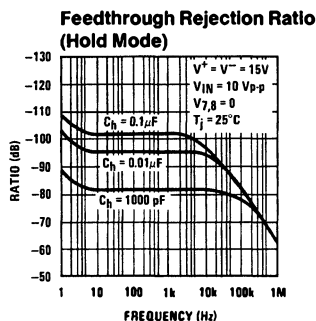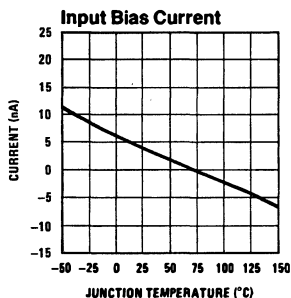
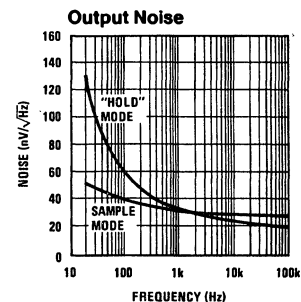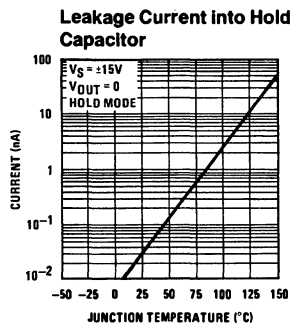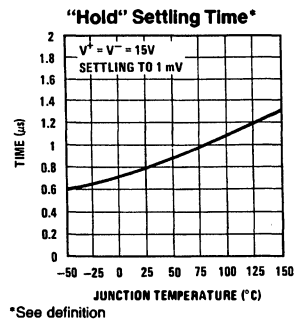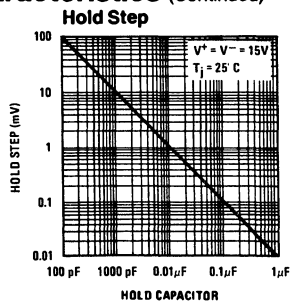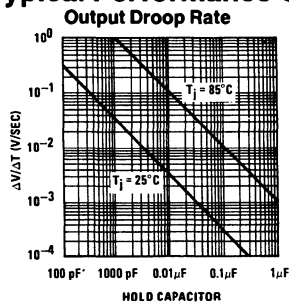**Note 6:** These parameters guaranteed over a supply voltage range of ± 5 to $\pm 18V$, and an input range of $-V_S + 3.5V \leq V_{IN} \leq +V_S - 3.5V$.
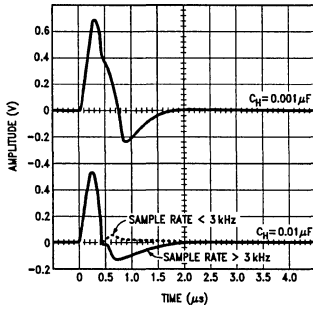
Typical Performance Characteristics

Aperture Time*

JUNCTION TEMPERATURE (°C)

*See Definition of Terms

Dielectric Absorption Error in Hold Capacitor

SAMPLE TIME (ms)

Dynamic Sampling Error

INPUT SLEW RATE (V/ms)

TL/H/5692-3

Typical Performance Characteristics (Continued)

Output Droop Rate

Hold Step

"Hold" Settling Time*

*See definition

Leakage Current into Hold Capacitor

Phase and Gain (Input to Output, Small Signal)

Gain Error

Power Supply Rejection

Output Short Circuit Current

Output Noise

Input Bias Current

Feedthrough Rejection Ratio (Hold Mode)
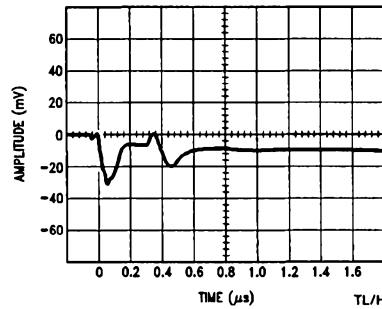

Hold Step vs Input Voltage
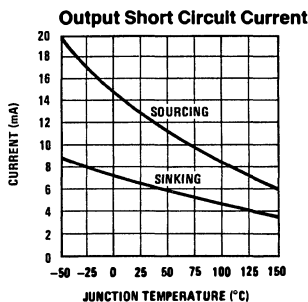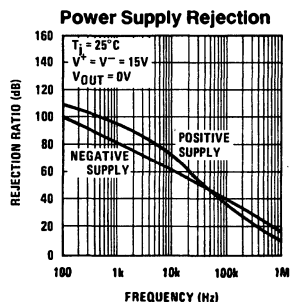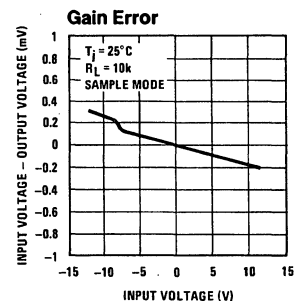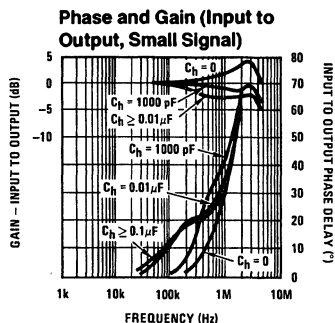
TL/H/5692–4

Typical Performance Characteristics (Continued)

Output Transient at Start of Sample Mode
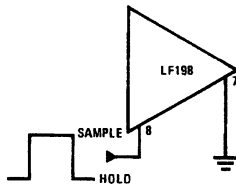

TL/H/5692–12

Output Transient at Start of Hold Mode

TL/H/5692–13

Logic Input Configurations

TTL & CMOS
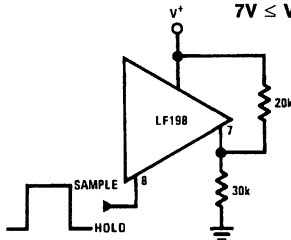### $3V \leq V_L$ (Hi State) $\leq 7V$
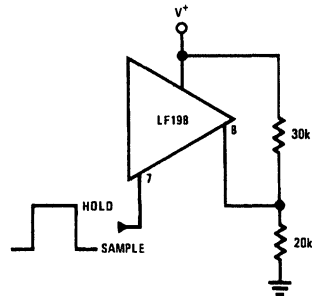

Threshold = 1.4V
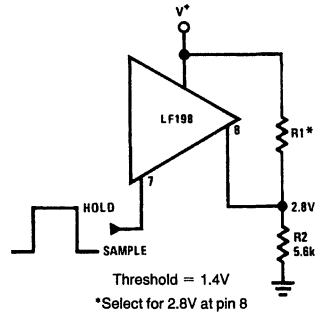
Threshold = 1.4V

*Select for 2.8V at pin 8
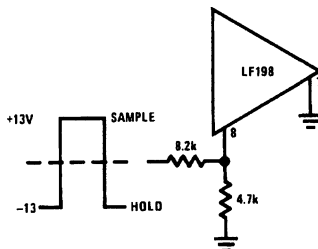
CMOS
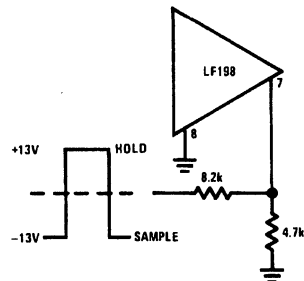### $7V \leq V_L$ (Hi State) $\leq 15V$

Threshold = 0.6 (V⁺) + 1.4V

Threshold = 0.6 (V⁺) − 1.4V

Op Amp Drive

Threshold ≈ +4V

Threshold = −4V

TL/H/5692–6

Application Hints

Hold Capacitor

Hold step, acquisition time, and droop rate are the major trade-offs in the selection of a hold capacitor value. Size and cost may also become important for larger values. Use of the curves included with this data sheet should be helpful in selecting a reasonable value of capacitance. Keep in mind that for fast repetition rates or tracking fast signals, the capacitor drive currents may cause a significant temperature rise in the LF198.

A significant source of error in an accurate sample and hold circuit is dielectric absorption in the hold capacitor. A mylar cap, for instance, may "sag back" up to 0.2% after a quick change in voltage. A long sample time is required before the circuit can be put back into the hold mode with this type of capacitor. Dielectrics with very low hysteresis are polystyrene, polypropylene, and Teflon. Other types such as mica and polycarbonate are not nearly as good. Ceramic is unusable with > 1% hysteresis. The advantage of polypropylene over polystyrene is that it extends the maximum ambient temperature from 85°C to 100°C. "NPO" or "COG" capacitors are now available for 125°C operation and also have low dielectric absorption. For more exact data, see the curve *Dielectric Absorption Error.* The hysteresis numbers on the curve are final values, taken after full relaxation. The hysteresis error can be significantly reduced if the output of the LF198 is digitized quickly after the hold mode is initiated. The hysteresis relaxation time constant in polypropylene, for instance, is 10—50 ms. If A-to-D conversion can be made within 1 ms, hysteresis error will be reduced by a factor of ten.

DC and AC Zeroing

DC zeroing is accomplished by connecting the offset adjust pin to the wiper of a 1 kΩ potentiometer which has one end tied to V^+ and the other end tied through a resistor to ground. The resistor should be selected to give ≈0.6 mA through the 1k potentiometer.

AC zeroing (hold step zeroing) can be obtained by adding an inverter with the adjustment pot tied input to output. A 10 pF capacitor from the wiper to the hold capacitor will give ±4 mV hold step adjustment with a 0.01 μF hold capacitor and 5V logic supply. For larger logic swings, a smaller capacitor (< 10 pF) may be used.

Logic Rise Time

For proper operation, logic signals into the LF198 must have a minimum dV/dt of 1.0 V/μs. Slower signals will cause excessive hold step. If a R/C network is used in front of the logic input for signal delay, calculate the slope of the waveform at the threshold point to ensure that it is at least 1.0 V/μs.

Sampling Dynamic Signals

Sample error to moving input signals probably causes more confusion among sample-and-hold users than any other parameter. The primary reason for this is that many users make the assumption that the sample and hold amplifier is truly locked on to the input signal while in the sample mode. In actuality, there are finite phase delays through the circuit creating an input-output differential for fast moving signals. In addition, although the output may have settled, the hold capacitor has an additional lag due to the 300Ω series resistor on the chip. This means that at the moment the "hold" command arrives, the hold capacitor voltage may be somewhat different than the actual analog input. The effect of these delays is opposite to the effect created by delays in the logic which switches the circuit from sample to hold. For example, consider an analog input of 20 Vp-p at 10 kHz. Maximum dV/dt is 0.6 V/μs. With no analog phase delay and 100 ns logic delay, one could expect up to (0.1 μs) (0.6V/μs) = 60 mV error if the "hold" signal arrived near maximum dV/dt of the input. A positive-going input would give a +60 mV error. Now assume a 1 MHz (3 dB) bandwidth for the overall analog loop. This generates a phase delay of 160 ns. If the hold capacitor sees this exact delay, then error due to analog delay will be (0.16 μs) (0.6 V/μs) = −96 mV. Total output error is +60 mV (digital) −96 mV (analog) for a total of −36 mV. To add to the confusion, analog delay is proportioned to hold capacitor value while digital delay remains constant. A family of curves (dynamic sampling error) is included to help estimate errors.

A curve labeled *Aperture Time* has been included for sampling conditions where the input is steady during the sampling period, but may experience a sudden change nearly coincident with the "hold" command. This curve is based on a 1 mV error fed into the output.

A second curve, *Hold Settling Time* indicates the time required for the output to settle to 1 mV after the "hold" command.

Digital Feedthrough

Fast rise time logic signals can cause hold errors by feeding externally into the analog input at the same time the amplifier is put into the hold mode. To minimize this problem, board layout should keep logic lines as far as possible from the analog input. Grounded guarding traces may also be used around the input line, especially if it is driven from a high impedance source. Reducing high amplitude logic signals to 2.5V will also help.
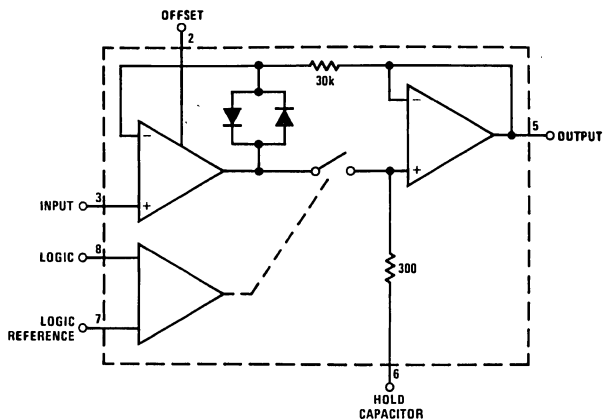
Guarding Technique
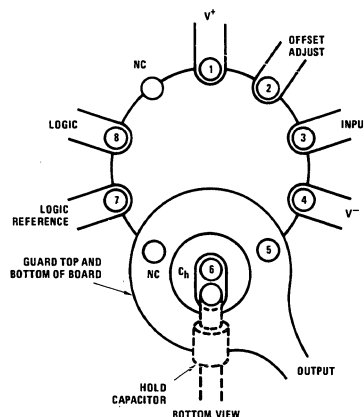
TL/H/5692–5

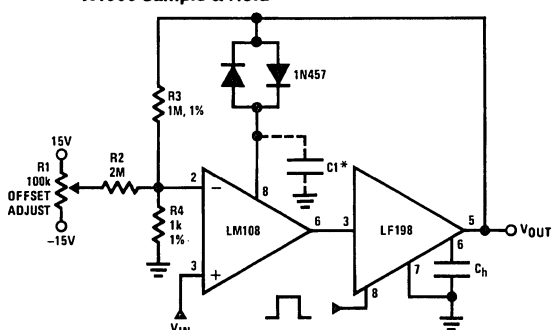**Use 10-pin layout. Guard around C_h is tied to output.**

Functional Diagram

TL/H/5692–1

Typical Applications (Continued)

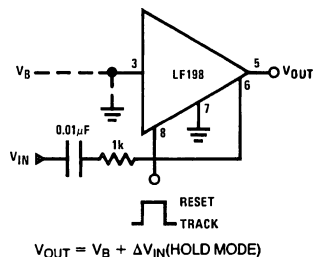### X1000 Sample & Hold

*For lower gains, the LM108 must be frequency compensated

Use $\approx \dfrac{100}{A_V}$ pF from comp 2 to ground

Sample and Difference Circuit
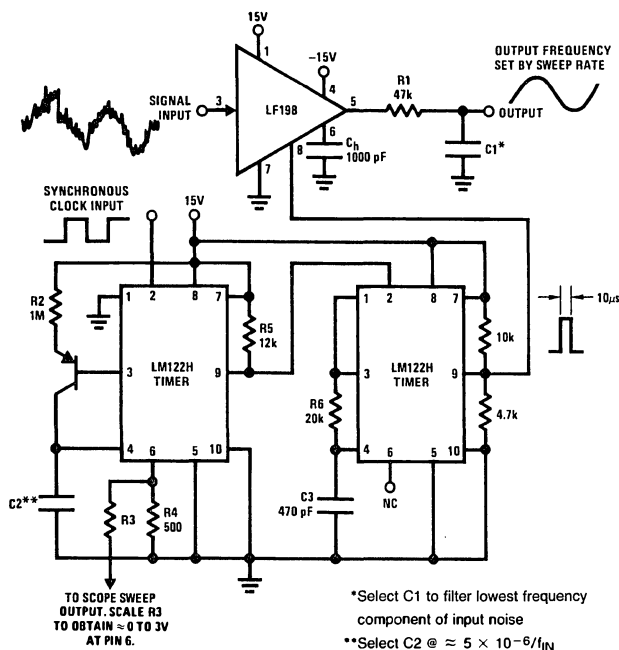### (Output Follows Input in *Hold* Mode)
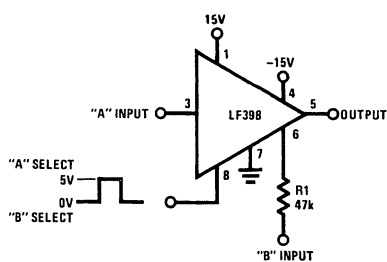

$V_{OUT} = V_B + \Delta V_{IN}$(HOLD MODE)

TL/H/5692–7

Typical Applications (Continued)

Ramp Generator with Variable Reset Level

*Select for ramp rate
R2 ≥ 10k

$$\frac{\Delta V}{\Delta T} = \frac{1.2V}{(R2)(C_h)}$$

Integrator with Programmable Reset Level

$$V_{OUT} \text{ (Hold Mode)} = \left[\frac{1}{(R1)(C_h)}\int_0^t V_{IN}\,dt\right] + \left[V_R\right]$$

Output Holds at Average of Sampled Input

$$\text{Select } (R_h)(C_h) \geqslant \frac{1}{2\pi f_{IN} \text{ (Min)}}$$

Increased Slew Current

Reset Stabilized Amplifier (Gain of 1000)

$V_{OS} \leq 20\mu V$ (No trim)

$Z_{IN} \approx 1\,M\Omega$

$$\frac{\Delta V_{OS}}{\Delta t} \approx 30\mu V/sec$$

$$\frac{\Delta V_{OS}}{\Delta T} \approx 0.1\mu V/°C$$

Fast Acquisition, Low Droop Sample & Hold

TL/H/5692–8

Typical Applications (Continued)

Synchronous Correlator for Recovering Signals Below Noise Level

TO SCOPE SWEEP OUTPUT. SCALE R3 TO OBTAIN ≈ 0 TO 3V AT PIN 6.

*Select C1 to filter lowest frequency component of input noise

**Select C2 @ ≈ $5 \times 10^{-6}/f_{IN}$

2-Channel Switch

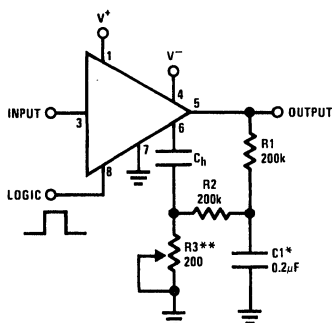|	A	B
Gain	1 ± 0.02%	1 ± 0.2%
Z_{IN}	$10^{10}\Omega$	47 kΩ
BW	≅ 1 MHz	≅ 400 kHz
Crosstalk @ 1 kHz	−90 dB	−90 dB
Offset	≤ 6 mV	≤ 75 mV

DC & AC Zeroing
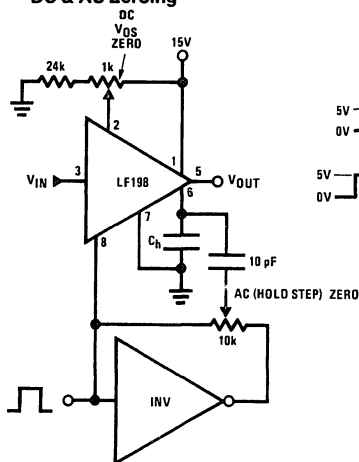
Staircase Generator
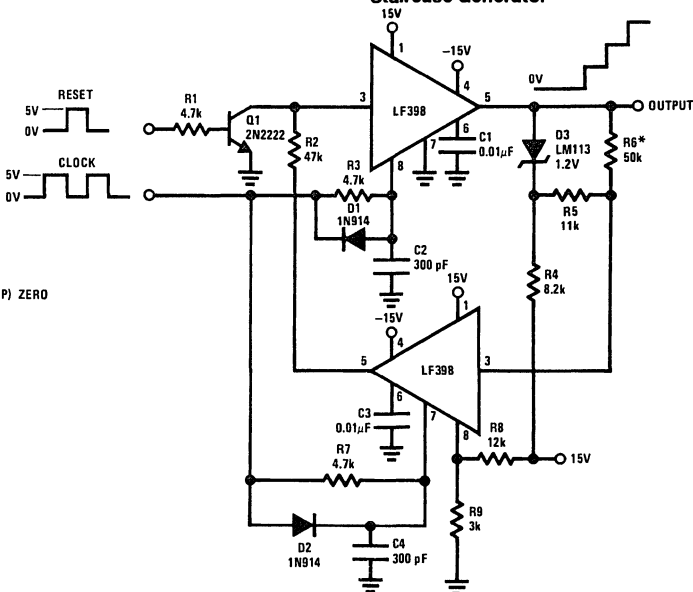
*Select for step height
50k ⟶ ≅ 1V Step
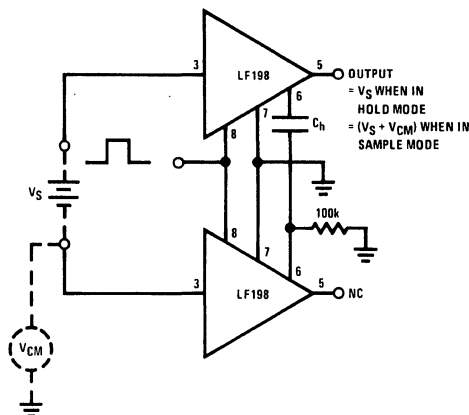
TL/H/5692–9

5-13

Typical Applications (Continued)

Capacitor Hysteresis Compensation

*Select for time constant $C1 = \dfrac{\tau}{100k}$

**Adjust for amplitude

Differential Hold

OUTPUT
= V_S WHEN IN HOLD MODE
= ($V_S + V_{CM}$) WHEN IN SAMPLE MODE

TL/H/5692–10

Definition of Terms

Hold Step: The voltage step at the output of the sample and hold when switching from sample mode to hold mode with a steady (dc) analog input voltage. Logic swing is 5V.

Acquisition Time: The time required to acquire a new analog input voltage with an output step of 10V. Note that acquisition time is not just the time required for the output to settle, but also includes the time required for all internal nodes to settle so that the output assumes the proper value when switched to the hold mode.

Gain Error: The ratio of output voltage swing to input voltage swing in the sample mode expressed as a per cent difference.

Hold Settling Time: The time required for the output to settle within 1 mV of final value after the "hold" logic command.

Dynamic Sampling Error: The error introduced into the held output due to a changing analog input at the time the hold command is given. Error is expressed in mV with a given hold capacitor value and input slew rate. Note that this error term occurs even for long sample times.

Aperture Time: The delay required between "Hold" command and an input analog transition, so that the transition does not affect the held output.