National Semiconductor Corporation

LH4003/LH4003C Precision RF Closed Loop Buffer

General Description

The LH4003 is a precision RF buffer optimized for unity gain applications. The LH4003 features a small signal bandwidth of 250 MHz. The buffer is internally compensated to be unity gain stable and has internal short circuit protection. The LH4003 is useful in applications such as video buffering, cable driving, and flash converter input conditioning.
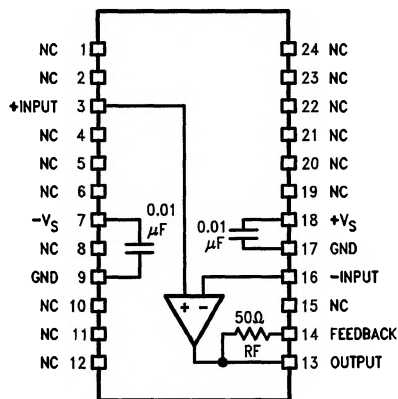
Features

- Operation from ±6V supplies
- Drive 50Ω directly
- Internal power supply bypassing
- Short circuit protection
- 1000 V/μs slew rate
- 0.97 gain accuracy into 50Ω

Applications

- Line drivers
- Video buffers

Block and Connection Diagram

NC	1		24	NC
NC	2		23	NC
+INPUT	3		22	NC
NC	4		21	NC
NC	5		20	NC
NC	6		19	NC
$-V_S$	7		18	$+V_S$
NC	8		17	GND
GND	9		16	$-$INPUT
NC	10		15	NC
NC	11		14	FEEDBACK
NC	12		13	OUTPUT

0.01 μF   0.01 μF   50Ω RF

Note 1: NC = No Connection
Note 2: Pins 9 & 17 Internally Connected

TL/K/9243–1

Top View

Order Number LH4003D, LH4003CD
See NS Package Number D24D

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage, V_S	$\pm 8V$
Power Dissipation, P_D	
$T_A = 25°C$, derate linearly at 62.5°C/W	2W
$T_C = 25°C$, derate linearly at 33.3°C/W	3.75W
Input Common Mode Voltage Range, V_{CM}	$\pm V_S$
Output Current, I_O	± 100 mA

Output Short Circuit Duration	Continuous
Operating Temperature Range, T_A	
LH4003CD	$-25°C$ to $+85°C$
LH4003D	$-55°C$ to $+125°C$
Storage Temperature Range, T_{STG}	$-65°C$ to $+150°C$
Maximum Junction Temperature, T_J	150°C
Lead Temperature (Soldering, 10 sec.)	300°C

DC Electrical Characteristics $V_S = \pm 6V$, $R_S = R_L = 50\Omega$, $T_A = 25°C$ unless otherwise noted. (Notes 1, 6)

Symbol	Parameter	Conditions		LH4003C			Units (Max Unless Otherwise Stated)
				Typ	Tested Limit (Note 2)	Design Limit (Note 3)	
V_{OS}	Output Offset Voltage	$T_A = T_J = 25°C$ (Note 4)		5	15		mV
$V_{OS/\Delta T}$	Offset Voltage Drift			100			$\mu V/°C$
I_B	Input Bias Current	$R_S = 300\Omega$, $T_A = T_J = 25°C$ (Note 4)		100	200		μA
A_V	Voltage Gain	$V_{IN} = 2\ V_{PP}$ $f = 1$ kHz	$R_L = 50\Omega$	0.98	0.95		$V/V_{(Min)}$
			$R_L = 1$ kΩ	0.98	0.95		
V_O	Output Voltage Swing				± 3		$V_{(Min)}$
PSRR	Power Supply Rejection Ratio	$V_S = \pm 4V$ to $\pm 8V$		55	45		$dB_{(Min)}$
I_S	Supply Current	$R_L = 1$ kΩ (Note 7)		55	65		mA
P_D	Power Dissipation					780	mW

AC Electrical Characteristics $V_S = \pm 6V$, $R_S = R_L = 50\Omega$, $T_A = 25°C$ unless otherwise noted. (Note 1)

Symbol	Parameter	Conditions		LH4003C			Units (Max Unless Otherwise Stated)
				Typ	Tested Limit (Note 2)	Design Limit (Note 3)	
t_r	Small Signal Rise Time	$\Delta V_{IN} = 0.5V$		2			ns
t_s	Settling Time to 0.1%	$V_{IN} = \pm 3V$		80			
SR	Slew Rate	$V_{IN} = -3V$ to $+3V$	10%–90%	1000		800	$V/\mu s$ (Min)
		$V_{IN} = +3V$ to $-3V$	10%–90%	1200		1000	
$f_{-3\ dB}$	Small Signal Bandwidth	$V_{OUT} = 100$ mVp-p		250	200		MHz (Min)
	Full Power Bandwidth	$V_{IN} = \pm 2V$, (Note 5)		65			MHz
	Harmonic Distortion	Second Order, $V_{OUT} = 4V$ p-p, $f_{IN} = 10$ MHz		-60			dB

DC Electrical Characteristics $V_S = \pm 6V, R_S = R_L = 50\Omega, T_A = 25°C$ unless otherwise noted. (Notes 1, 6)

Symbol	Parameter	Conditions		Typ	LH4003 Tested Limit (Note 2)	Design Limit (Note 3)	Units (Max Unless Otherwise Stated)
V_{OS}	Output Offset Voltage	$T_A = T_J = 25°C$ (Note 4)		2	15		mV
					20		
$V_{OS/\Delta T}$	Offset Voltage Drift			100			$\mu V/°C$
I_B	Input Bias Current	$R_S = 300\Omega$	$T_A = T_J = 25°C$, (Note 4)	100	200		μA
					200		
A_V	Voltage Gain	$V_{IN} = 2 V_{PP}$ $f = 1 kHz$	$R_L = 50\Omega$	0.98	0.95	**0.93**	V/V(Min)
			$R_L = 1 k\Omega$	0.98	0.95		
					0.93		
V_O	Output Voltage Swing	$A_V = +1$			± 3	± 3	V (Min)
PSRR	Power Supply Rejection Ratio	$V_S = \pm 4V$ to $\pm 8V$		55	45		dB (Min)
					40		
I_S	Supply Current	$R_L = 1 k\Omega$ (Note 7)		55	65	**80**	mA
P_D	Power Dissipation					780	mW

AC Electrical Characteristics $V_S = \pm 6V, R_S = R_L = 50\Omega, T_A = 25°C$ unless otherwise noted. (Note 1)

Symbol	Parameter	Conditions		Typ	LH4003 Tested Limit (Note 2)	Design Limit (Note 3)	Units (Max Unless Otherwise Stated)
t_r	Small Signal Rise Time	$\Delta V_{IN} = 0.5V$		2			ns
t_s	Settling Time to 0.1%	$V_{IN} = \pm 3V$		80			ns
SR	Slew Rate	$V_{IN} = -3V$ to $+3V$	10%–90%	1000		800	$V_{\mu S}$ (Min)
		$V_{IN} = +3V$ to $-3V$	10%–90%	1200		1000	
$f_{-3 dB}$	Small Signal Bandwidth	$V_{OUT} = 100 mVp\text{-}p$		250	200		MHz (Min)
	Full Power Bandwidth	$V_{IN} = \pm 2V$, (Note 5)		65			MHz
	Harmonic Distortion	Second Order, $V_{OUT} = 4V$ p-p, $f_{IN} = 10$ MHz		-60			dB

Note 1: These measurements are taken with the LH4003 strapped for a gain of +1.

Note 2: Tested limits are guaranteed and 100% tested in production.

Note 3: Design limits are guaranteed (but not 100% production tested) over indicated temperature and supply voltage ranges. These limits are not used to calculate outgoing quality levels.
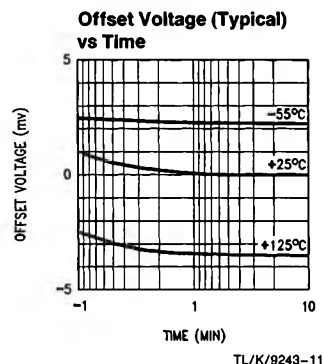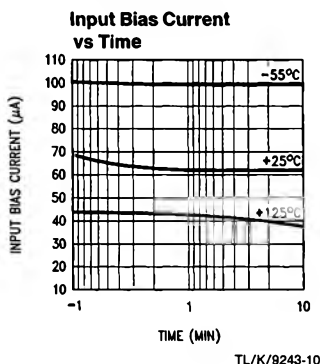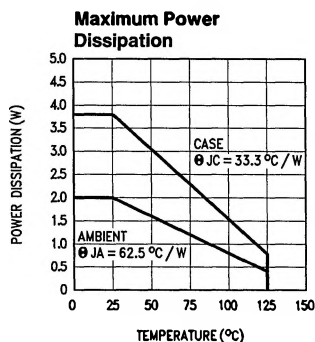
Note 4: Specification is at 25°C junction temperature due to requirements of high speed automatic testing. Actual values at operating temperature will exceed value at $T_J = 25°C$. See Typical Performance Characteristics for more information.

Note 5: Full power bandwidth is calculated based on slew rate measurement using FPBW = slew rate / (2 πV peak).

Note 6: Boldface limits are guaranteed over full temperature. Operating ambient temperature range of LH4003C is −25°C to +85°C, and LH4003 is −55°C to +125°C.

Note 7: When the LH4003 is operated at elevated temperature (such as 125°C), some form of heat sinking or forced air cooling is required. The quiescent power with V_S of $\pm 6V$ is 780 mW, whereas the package is rated to 750 mW without a heatsink at 125°C.

Typical Performance Characteristics

Maximum Power Dissipation

TL/K/9243–2

Input Bias Current vs Time

TL/K/9243-10

Offset Voltage (Typical) vs Time

TL/K/9243–11

Application Information

The unity gain follower configuration shown in *Figure 1,* offers a 250 MHz small signal bandwidth to the −3dB point and the minimum slew rate of 800 V/μs insures a full power bandwidth of 65 MHz for a 4V peak-to-peak signal, according to the formula:

$$B = SR/2 \pi Vp$$

Where SR is the slew rate in μs, B is the bandwidth of the device in MHz for a peak sine wave voltage Vp.

The unity gain follower/buffer is therefore an excellent choice for wideband sinewave buffering or pulse amplification. *Figure 2* shows the typical pulse response for such a configuration.

DRIVING CAPACITIVE LOADS

Flash A/D, unterminated cables, etc, can exhibit up to 300 pF of capacitance, thus creating stability or settling problems. *Figure 3* shows the compensation scheme for driving such capacitive loads while still insuring optimum settling. The output current limit of the LH4003 is a considerable help for driving capacitive loads, the charging current is kept in control and the damping resistor can be small without overloading the output stage. A 20Ω resistor in series with the capacitance is required for insuring an optimum settling time of 0.5% in less than 20 ns which is suitable for driving a 7 bit flash A to D converter in video applications at a sampling rate of 20 MSPS (see *Figure 4*).

LAYOUT CONSIDERATIONS

The layout of a RF/Video PC board where the signal frequency is beyond 100 MHz required special attention. All the traces or connections must be as short and as wide as possible in order to keep their parasitic inductance to a minimum. This is especially critical for the supply lines where the current can reach over 100 mA in a few nanoseconds.

Although the LH4003 contains internal decoupling, it still requires some external bypassing capacitors, which have to be located as close to the supply pins as possible. A 4.7 μF in parallel with a 100 nF low inductance capacitor will insure good filtering. In some cases of noisy environment, or when the power supply is located far from the circuit, it may be necessary to use a dual stage decoupling as shown in *Figure 5*.

Ground can also become a considerable problem. It is assumed to be uniformly zero volts and considered as a reference. In practice, if the ground is poorly laid out, every single point may be at a different potential and at a different phase, which is a source of instability or signal distortion.

The most reliable solution to this problem is to have a ground plane that will minimize the parasitic inductance and therefore, potential and phase differences.
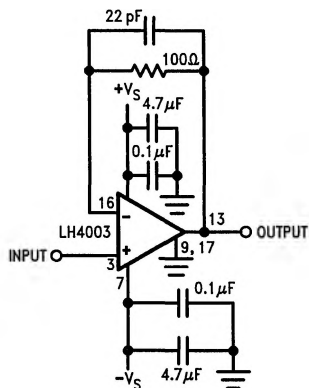
INPUT CAPACITANCE

The input capacitance of the LH4003 is typically 8 pF and will slightly increase with frequency. A large source resistance value in front of this will form a pole, which may substantially reduce the bandwidth of the circuit and affect stability.

This is the reason why resistor values higher than 500 ohms should not be utilized in the feedback network and high source impedance should be avoided.

BIAS CURRENT

The input bias current is typically 100 μA and may create an undesirable output offset voltage when the source impedance is high. An internal 50Ω resistor is provided for matching with a 50Ω source impedance in order to minimize the output offset voltage. *Figure 6* shows a circuit that uses a FET transistor pair for the input stage in order to reduce the input bias current to the sub-nanoampere region.
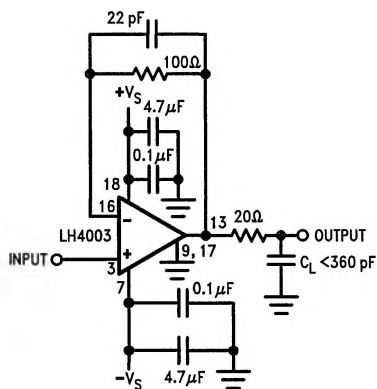
Typical Applications

TL/K/9243-3

FIGURE 1. Unity Gain Follow,
Typical BW 3dB = 250 MHz
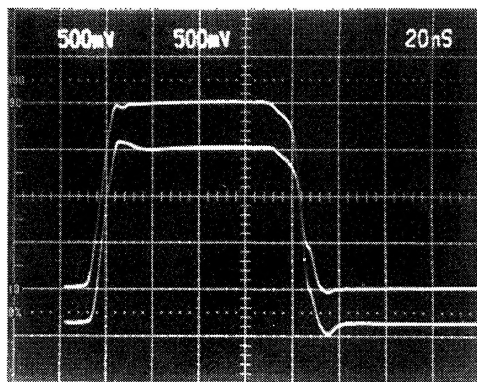
TL/K/9243-4

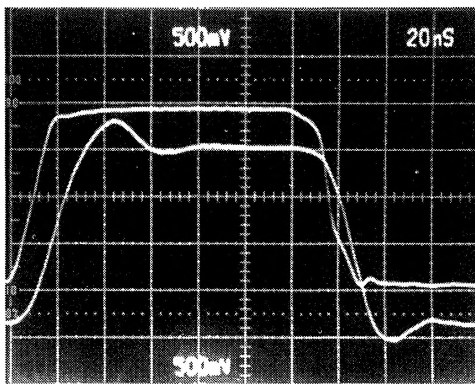**Note:** Top trace is input and bottom trace is output. $V_{CC} = \pm 6V$, $R_S = R_L = 50\Omega$.

FIGURE 2. Pulse Response of Follower

TL/K/9243-6

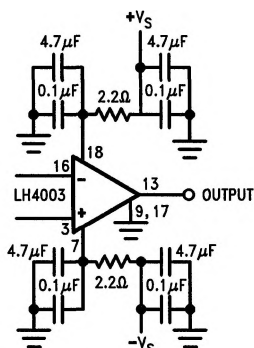**FIGURE 3. Driving Capacitance**
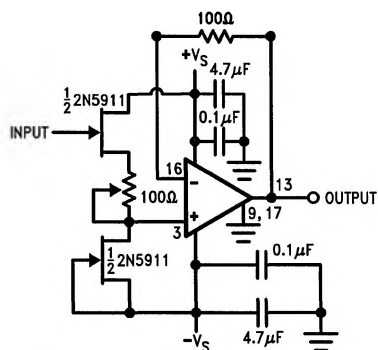
3-31

Typical Applications (Continued)

TL/K/9243–7

Note: Top trace is input and bottom trace is output. $V_{CC} = \pm 6V$, $R_S = 50\Omega$, $R_{ISO} = 20\Omega$ and $C_L = 300$ pF.

FIGURE 4. Pulse Response when Driving Capacitance.

TL/K/9243–8

FIGURE 5. Dual Stage Decoupling

TL/K/9243–9

FIGURE 6. FET Buffer Reduces Bias Current