National Semiconductor Corporation

PRELIMINARY

LH4006/LH4006C Precision RF Closed Loop Buffer

General Description

The LH4006 is a precision RF buffer optimized for unity gain applications. It features a small signal bandwidth of 350 MHz. The buffer is internally compensated to be unity gain stable and has internal short circuit protection. The LH4006 is useful in applications such as video buffering, cable driving, and flash converter input conditioning. The high bandwidth also allows the LH4006 to be used in RF/IF signal conditioning such as amplification or down conversion.

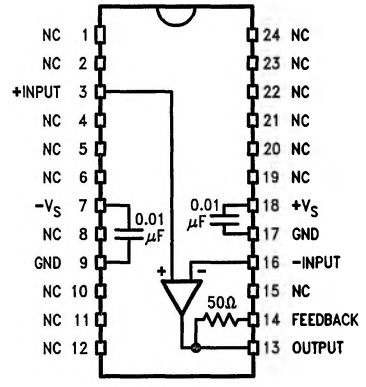
Features

- Operation from ±6V supplies
- Drives 50Ω directly
- Internal power supply bypassing
- Short circuit protection
- 1000 V/μs slew rate
- 0.95 gain accuracy into 50Ω

Applications

- Line drivers
- Video buffers
- Pulse amplifiers

Connection Diagram



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Top View

Note 1: NC = not connected.

Note 2: Pins 9 & 17 are internally connected.

Order Number LH4006D & LH4006CD
See NS Package Number D24D

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage, V_S ±8V

Power Dissipation, P_D
- T_C = 25°C, Derate Linearly at 33.3°C/W 3.75W
- T_A = 25°C, Derate Linearly at 62.5°C/W 2W

Input Common Mode Voltage Range, V_{CM} $\pm V_S$

Output Current, I_O ±100 mA

Output Short Circuit Duration Continuous

Operating Temperature Range, T_A
- LH4006CD −25°C to +85°C
- LH4006D −55°C to +125°C

Storage Temperature Range, T_{STG} −65°C to +150°C

Maximum Junction Temperature, T_J 150°C

Lead Temperature (Soldering < 10 sec.) 300°C

ESD Rating to be determined.

DC Electrical Characteristics (Notes 1 & 6)

V_S = ±6V, R_S = R_L = 50Ω, T_A = 25°C unless otherwise noted.

Symbol	Parameter	Conditions		LH4006C Typ	LH4006C Tested Limit (Note 2)	LH4006C Design Limit (Note 3)	Units (Max unless otherwise stated)
V_{OS}	Output Offset Voltage	T_A = T_J = 25°C, Note 4		5	15		mV
$V_{OS/\Delta T}$	Offset Voltage Drift			100			µV/°C
I_B	Input Bias Current	R_S = 300Ω, Note 4		100	300		µA
A_V	Voltage Gain	V_{IN} = 2 Vp-p, f = 1 kHz	R_L = 50Ω	0.98	0.95		V/V (min)
			R_L = 1 kΩ	0.98	0.95		
V_O	Output Voltage Swing	A_V = +1			±3		V (min)
PSRR	Power Supply Rejection Ratio	V_S = ±4V to ±8V, R_L = 1 kΩ		55	45		dB (min)
I_S	Supply Current	V_{IN} = 0V, R_L = 1 kΩ, Note 7		55	65		mA
P_D	Power Dissipation					780	mW

AC Electrical Characteristics (Note 1)

V_S = ±6V, R_S = R_L = 50Ω, T_A = 25°C unless otherwise noted.

Symbol	Parameter	Conditions		LH4006C Typ	LH4006C Tested Limit (Note 2)	LH4006C Design Limit (Note 3)	Units (Max unless otherwise stated)
tr	Small Signal Rise Time	ΔV_{IN} = 0.5V		2			ns
ts	Settling Time to 0.1%	V_{IN} = ±3V		80			
SR	Slew Rate	V_{IN} = −3V to +3V	10%–90%	1000			V/µs (min)
		V_{IN} = +3V to −3V	10%–90%	1200			
$f_{-3\,dB}$	Small Signal Bandwidth	V_{OUT} = 100 mVp-p	A_V = +1	350	300		MHz (min)
	Full Power Bandwidth	V_{IN} = ±2V, Note 5		80			
	Second Order Harmonic Distortion	V_{OUT} = 4 Vp-p, f_{IN} = 10 MHz		−60			dB

DC Electrical Characteristics (Notes 1 & 6)

V_S = ±6V, R_S = R_L = 50Ω, T_A = 25°C unless otherwise noted.

Symbol	Parameter	Conditions		LH4006 Typ	LH4006 Tested Limit (Note 2)	LH4006 Design Limit (Note 3)	Units (Max unless otherwise stated)
V_{OS}	Output Offset Voltage	$T_A = T_J = 25°C$		2	15		mV
					25		
$V_{OS/\Delta T}$	Offset Voltage Drift	V_{IN} = 0V		100			µV/°C
I_B	Input Bias Current	R_S = 300Ω $T_A = T_J = 25°C$, Note 4		100	300		µA
					400		
A_V	Voltage Gain	V_{IN} = 2 Vp-p, f = 1 kHz	R_L = 50Ω	0.98	0.95 **0.93**		V/V (min)
			R_L = 1 kΩ	0.98	0.95 **0.93**		
V_O	Output Voltage Swing	A_V = +1			±3	**±3**	V (min)
PSRR	Power Supply Rejection Ratio	V_S = ±4V to +8V		55	45		dB (min)
					40		
I_S	Supply Current	V_{IN} = 0V, R_L = 1 kΩ (Note 7)		55	65	**80**	mA
P_D	Power Dissipation					780	mW

AC Electrical Characteristics (Note 1)

V_S = ±6V, R_S = R_L = 50Ω, T_A = 25°C unless otherwise noted.

Symbol	Parameter	Conditions		LH4006 Typ	LH4006 Tested Limit (Note 2)	LH4006 Design Limit (Note 3)	Units (Max unless otherwise stated)
tr	Small Signal Rise Time	ΔV_{IN} = 0.5V		2			ns
ts	Settling Time to 0.1%	V_{IN} = ±3V		80			
SR	Slew Rate	V_{IN} = −3V to +3V	10%–90%	1000			V/µs (min)
		V_{IN} = +3V to −3V	10%–90%	1200			
$f_{-3\,dB}$	Small Signal Bandwidth	V_{OUT} = 100 mVp-p	A_V = +1	350	300		MHz (min)
	Full Power Bandwidth	V_{IN} = ±2V, Note 5		80			
	Second Order Harmonic Distortion	V_{OUT} = 4 Vp-p, f_{IN} = 10 MHz		−60			dB

Note 1: These measurements are taken with the LH4006 strapped for a gain of +1.

Note 2: Tested limits are guaranteed and 100% tested in production.

Note 3: Design limits are guaranteed (but not 100% production tested) over indicated temperature and supply voltage ranges. These limits are not used to calculate outgoing quality levels.

Note 4: Specification is at 25°C junction temperature due to requirements of high speed automatic testing. Actual value may be higher at operating junction temperature.

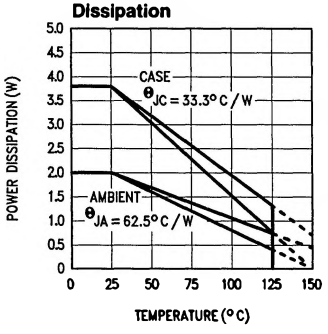
Note 5: Full power bandwidth is calculated based on slew rate measurement using FPBW = slew rate/(2 πV peak).

Note 6: Boldface limits are guaranteed over full temperature. Operating ambient temperature range of LH4006C is −25°C to +85°C, and LH4006 is −55°C to +125°C.

Note 7: When the LH4006 is operated at elevated temperature (such as 125°C), some form of heat sinking or forced air cooling is required. The quiescent power with V_S of ±6V is 780 mW, whereas the package is rated to 750 mW without a heatsink at 125°C.

Typical Performance Characteristics

Maximum Power Dissipation



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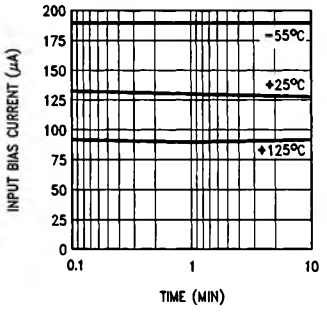
Input Bias Current vs Time



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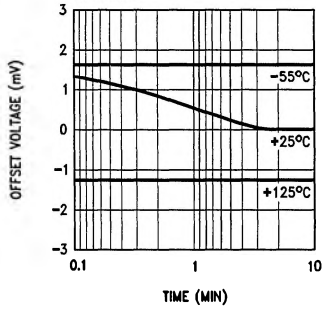
Offset Voltage (Typical) vs Time



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Application Information

The unity gain follower configuration shown in *Figure 1*, offers a 350 MHz small signal bandwidth to the −3 dB point and the minimum slew rate of 1000 V/μs insures a full power bandwidth of 80 MHz for a 4V peak to peak signal, according to the formula:

$$B = \frac{SR}{2\pi Vp}$$

Where SR is the slew rate in V/μs, B is the bandwidth of the device in MHz for a peak sine wave voltage Vp.

The unity gain follower/buffer is therefore an excellent choice for wideband sinewave buffering or pulse amplification. *Figure 2* shows the typical pulse response for such a configuration.

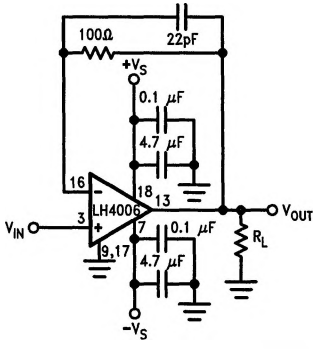

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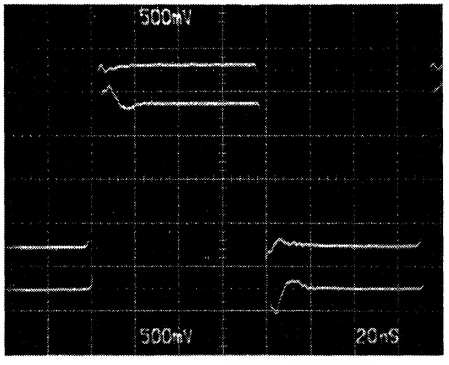
FIGURE 1. Unity Gain Follower



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V_{CC} = ±6V, R_S = R_L = 50Ω.

FIGURE 2. Follower/Buffer Pulse Response

Driving Capacitive Loads

Flash A/D, unterminated cables, etc, can exhibit up to 300 pF of capacitance, thus creating stability or settling problems. *Figure 3* shows the compensation scheme for driving such capacitive loads while still insuring optimum settling. The output current limit of the LH4006 is a considerable help for driving capacitive loads, the charging current is kept in control and the damping resistor can be small without overloading the output stage. A 20Ω resistor in series with the capacitance is required for insuring an optimum settling time to 0.5% in less than 20 ns which is suitable for driving a 7 bit flash A to D converter in video applications at a sampling rate of 20 MSPS (see *Figure 4*).

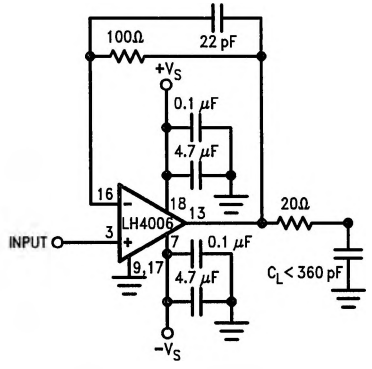

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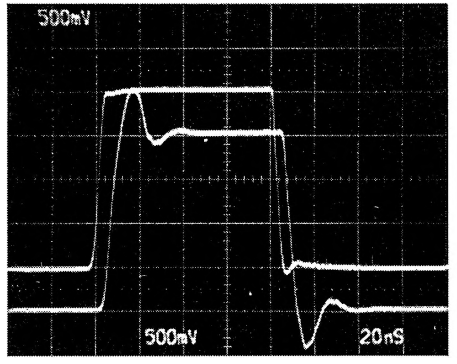
FIGURE 3. Driving Capacitance



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V_{CC} = ±6 Volts

C_L = 360 pF

FIGURE 4. Pulse Response When Driving Capacitance

Layout Considerations

The layout of a RF/Video PC board where the signal frequency is beyond 100 MHz requires special attention. All the traces or connections must be as short and as wide as possible in order to keep their parasitic inductance to a minimum. This is especially critical for the supply lines where the current can reach over 100 mA in a few nanoseconds.

Although the LH4006 contains internal decoupling, it still requires some external bypassing capacitors, which have to be located as close to the supply pins as possible. A 4.7 μF in parallel with a 100 nF low inductance capacitor will insure good filtering. In some cases of noisy environment, or when the power supply is located far from the circuit, it may be necessary to use a dual stage decoupling as shown in *Figure 5.*

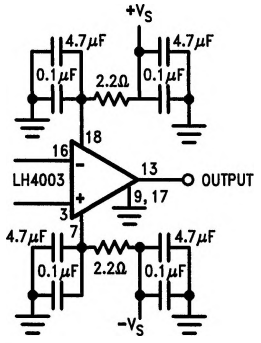

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FIGURE 5. Dual Stage Decoupling

Ground can also become a considerable problem. It is assumed to be uniformly zero volts and considered as a reference. In practice, if the ground is poorly laid out, every single point may be at a different potential and at a different phase, which is a source of instability or signal distortion.

The most reliable solution to this problem is to have a ground plane that will minimize the parasitic inductance and therefore, potential and phase differences.

Input Capacitance

The input capacitance of the LH4006 is typically 8 pF and will slightly increase with frequency. A large source resistance value in front of this will form a pole, which may substantially reduce the bandwidth of the circuit and affect stability.

This is the reason why resistor values higher than 500Ω should not be used in the feedback network and high source impedance should be avoided.

Bias Current

The input bias current is typically 100 μA and may create an undesirable output offset voltage when the source impedance is high. An internal 50Ω resistor is provided for matching with a 50Ω source impedance in order to minimize the output offset voltage. *Figure 6* shows a circuit that uses a FET transistor pair for the input stage in order to reduce the input bias current to the sub-nanoampere region.

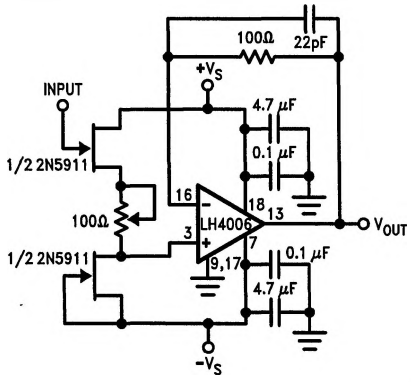

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FIGURE 6. FET Input Follower Buffer