LM119QML High Speed Dual Comparator

Check for Samples: LM119QML

FEATURES

- **Available with radiation guaranteed**
  - **High Dose Rate 100 krad(Si)**
  - **ELDRS Free 100 krad(Si)**
- **Two independent comparators**
- **Operates from a single 5V supply**
- **Typically 80 ns response time at ±15V**
- **Minimum fan-out of 2 each side**
- **Maximum input current of 1 µA over temperature**
- **Inputs and outputs can be isolated from system ground**
- **High common mode slew rate**

DESCRIPTION

The LM119 is a precision high speed dual comparator fabricated on a single monolithic chip. It is designed to operate over a wide range of supply voltages down to a single 5V logic supply and ground. Further, it has higher gain and lower input currents than devices like the LM710. The uncommitted collector of the output stage makes the LM119 compatible with RTL, DTL and TTL as well as capable of driving lamps and relays at currents up to 25 mA.

Although designed primarily for applications requiring operation from digital logic supplies, the LM119 is fully specified for power supplies up to ±15V. It features faster response than the LM111 at the expense of higher power dissipation. However, the high speed, wide operating voltage range and low package count make the LM119 much more versatile than older devices like the LM711.

Connection Diagrams

CDIP Package

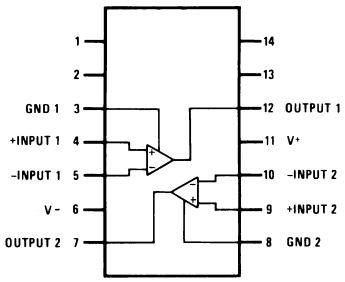


Figure 1. Top View
Package Number J0014A

LCCC Package

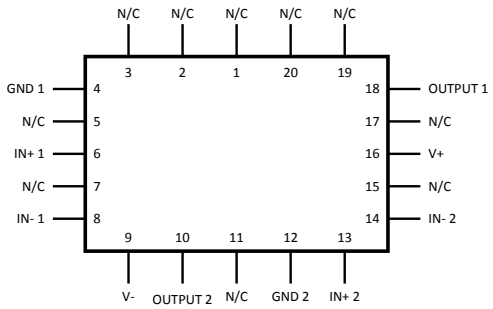
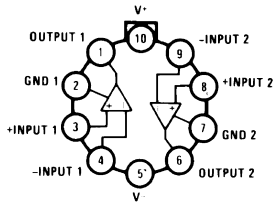


Figure 2. Top View
Package Number NAJ0020A

TO-100 Package



Case is connected to pin 5 (V^-).

Figure 3. Top View
Package Number LME0010C

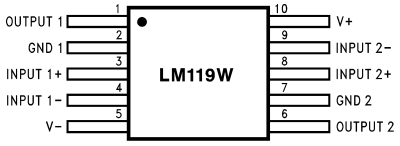
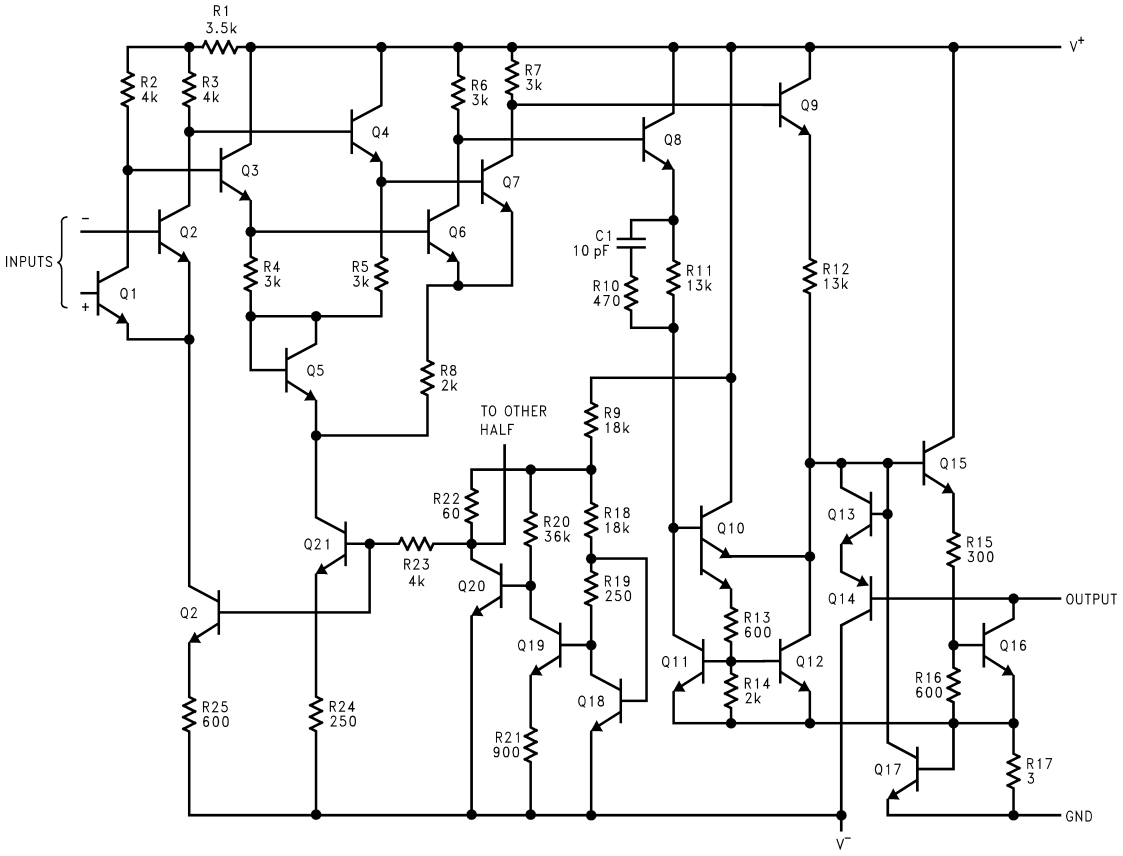


Figure 4. Top View
Package Number NAD0010A, NAC0010A

Schematic Diagram



*Do not operate the LM119 with more than 16V between GND and V^+

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings (1)

Total Supply Voltage	36V
Output to Negative Supply Voltage	36V
Ground to Negative Supply Voltage	25V
Ground to Positive Supply Voltage	18V
Differential Input Voltage	±5V
Input Voltage (2)	±15V
Power Dissipation (3)	500 mW
Output Short Circuit Duration	10 sec
Storage Temperature Range	−65°C ≤ T_A ≤ 150°C
Operating Ambient Temperature Range	−55°C ≤ T_A ≤ 125°C
Maximum Junction Temperature (T_J)	150°C
Lead Temperature (Soldering, 10 sec.)	260°C
Thermal Resistance	
θ_{JA}	
LCCC Package (Still Air)	89°C/W
LCCC Package (500LF/Min Air flow)	63°C/W
TO-100 Package (Still Air)	162°C/W
TO-100 Package (500LF/Min Air flow)	88°C/W
CDIP Package (Still Air)	94°C/W
CDIP Package (500LF/Min Air flow)	52°C/W
CLGA Package (Still Air)	215°C/W
CLGA Package (500LF/Min Air flow)	132°C/W
CLGA Package (Still Air)	215°C/W
CLGA Package (500LF/Min Air flow)	132°C/W
θ_{JC}	
LCCC Package	5°C/W
TO-100 Package	31°C/W
CDIP Package	11°C/W
CLGA Package	13°C/W
CLGA Package	13°C/W
Package Weight	
LCCC Package	TBD
TO-100 Package	TBD
CDIP Package	TBD
CLGA Package	TBD
CLGA Package	225mg
ESD rating (4)	800V

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

(2) For supply voltages less than ±15V the absolute maximum input voltage is equal to the supply voltage.

(3) The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{Jmax} (maximum junction temperature), θ_{JA} (package junction to ambient thermal resistance), and T_A (ambient temperature). The maximum allowable power dissipation at any temperature is $P_{Dmax} = (T_{Jmax} - T_A)/\theta_{JA}$ or the number given in the Absolute Maximum Ratings, whichever is lower.

(4) Human Body model, 1.5KΩ in series with 100pF.

Table 1. Quality Conformance Inspection(1)

Subgroup	Description	Temp °C
1	Static tests at	25
2	Static tests at	125
3	Static tests at	-55
4	Dynamic tests at	25
5	Dynamic tests at	125
6	Dynamic tests at	-55
7	Functional tests at	25
8A	Functional tests at	125
8B	Functional tests at	-55
9	Switching tests at	25
10	Switching tests at	125
11	Switching tests at	-55
12	Settling time at	25
13	Settling time at	125
14	Settling time at	-55

(1) Mil-Std-883, Method 5005 - Group 5

LM119/883 Electrical Characteristics DC Parameters

The following conditions apply, unless otherwise specified. V_{CM} = 0V

Symbol	Parameter	Conditions	Notes	Min	Max	Units	Sub-groups
$+I_{CC}$	Positive Supply Current	$\pm V_{CC}$ = ±15V, V_O = Low V^+ = 5.6V thru 1.4KΩ			11	mA	1
					11.5	mA	2
$-I_{CC}$	Negative Supply Current	$\pm V_{CC}$ = ±15V, V_O = Low V^+ = 5.6V thru 1.4KΩ		-4.2		mA	1
				-4.5		mA	2
I_{Leak}	Output Leakage Current	$^+V_{CC}$ = 15V, $^-V_{CC}$ = -1V, V_{Gnd} = 0V, V_O = 35V, V_I = 5mV			1.8	µA	1
					9.5	µA	2
					10.0	µA	3
I_{IB}	Input Bias Current	$\pm V_{CC}$ = ±15V			0.475	µA	1
					0.95	µA	2, 3
		$^+V_{CC}$ = 5V, $^-V_{CC}$ = 0V, V_{CM} = 1.5V			0.475	µA	1
					.95	µA	2, 3
V_{IO}	Input Offset Voltage	$^+V_{CC}$ = 5V, $^-V_{CC}$ = 0V, V_{CM} = 1V, R_S ≤ 5KΩ		-3.8	3.8	mV	1
				-6.8	6.8	mV	2, 3
		$^+V_{CC}$ = 5V, $^-V_{CC}$ = 0V, V_{CM} = 3V, R_S ≤ 5KΩ		-3.8	3.8	mV	1
				-6.8	6.8	mV	2, 3
		$\pm V_{CC}$ = ±15V, V_{CM} = 12V, R_S ≤ 5KΩ		-3.8	3.8	mV	1
				-6.8	6.8	mV	2, 3
		$\pm V_{CC}$ = ±15V, V_{CM} = -12V, R_S ≤ 5KΩ		-3.8	3.8	mV	1
				-6.8	6.8	mV	2, 3
I_{IO}	Input Offset Current	$^+V_{CC}$ = 5V, $^-V_{CC}$ = 0V, V_{CM} = 1V		-75	75	nA	1
				-100	100	nA	2, 3
		$^+V_{CC}$ = 5V, $^-V_{CC}$ = 0V, V_{CM} = 3V		-75	75	nA	1
				-100	100	nA	2, 3
		$\pm V_{CC}$ = ±15V, V_{CM} = 12V		-75	75	nA	1
				-100	100	nA	2, 3
		$\pm V_{CC}$ = ±15V, V_{CM} = -12V		-75	75	nA	1
				-100	100	nA	2, 3
V_{Sat}	Output Saturation Voltage	$\pm V_{CC}$ = ±15V, I_O = 25mA, V_I = -5mV			1.5	V	1
		$^+V_{CC}$ = 5V, $^-V_{CC}$ = 0V, I_O= 4.0mA	(1)		0.4	V	1, 2
			(1)		0.6	V	3
A_V	Voltage Gain	$\pm V_{CC}$ = ±15V, Delta V_O = 12V, R_L = 1.4KΩ	(2), (3)	10.5		K	4
			(2), (3)	10		K	5, 6
		$^+V_{CC}$ = 5V, $^-V_{CC}$ = 0V, Delta V_O = 4.5V, R_L = 1.4KΩ	(2), (4)	8.0		K	4
			(2), (4)	5.0		K	5
			(2), (4)	5.8		K	6

(1) Output is monitored by measuring V_I with limits from 0 to 6mV at all temperatures
(2) K = V/mV.
(3) Gain is computed with an output swing from +13.5V to +1.5V.
(4) Gain is computed with an output swing from +5.0V to +0.5V.

LM119-SMD Electrical Characteristics SMD 8601401 DC Parameters

The following conditions apply, unless otherwise specified. V_{CM} = 0V

Symbol	Parameter	Conditions	Notes	Min	Max	Units	Sub-groups
$+I_{CC}$	Positive Supply Current	$\pm V_{CC}$ = ±15V, V_O = Low V^+ = 5.6V thru 1.4KΩ			11	mA	1
					11.5	mA	2, 3
$-I_{CC}$	Negative Supply Current	$\pm V_{CC}$ = ±15V, V_O = Low V^+ = 5.6V thru 1.4KΩ		-4.2		mA	1
				-4.5		mA	2
				-6.0		mA	3
I_{Leak}	Output Leakage Current	$^+V_{CC}$ = 15V, $^-V_{CC}$ = -1V, V_{Gnd} = 0V, V_O = 35V	(1)		1.8	µA	1
			(1)		10	µA	2, 3
I_{IB}	Input Bias Current	$\pm V_{CC}$ = ±15V			0.475	µA	1
					0.95	µA	2, 3
		$^+V_{CC}$ = 5V	(2)		0.475	µA	1
			(2)		.95	µA	2, 3
V_{IO}	Input Offset Voltage	$^+V_{CC}$ = 5V, V_{CM} = 1V, R_S ≤ 5KΩ	(2)	-3.8	3.8	mV	1
			(2)	-6.8	6.8	mV	2, 3
		$^+V_{CC}$ = 5V, V_{CM} = 3V, R_S ≤ 5KΩ	(2)	-3.8	3.8	mV	1
			(2)	-6.8	6.8	mV	2, 3
		$\pm V_{CC}$ = ±15V, V_{CM} = 12V, R_S ≤ 5KΩ		-3.8	3.8	mV	1
				-6.8	6.8	mV	2, 3
		$\pm V_{CC}$ = ±15V, V_{CM} = -12V, R_S ≤ 5KΩ		-3.8	3.8	mV	1
				-6.8	6.8	mV	2, 3
I_{IO}	Input Offset Current	$^+V_{CC}$ = 5V, V_{CM} = 1V	(2)	-75	75	nA	1
			(2)	-100	100	nA	2, 3
		$^+V_{CC}$ = 5V, V_{CM} = 3V	(2)	-75	75	nA	1
			(2)	-100	100	nA	2, 3
		$\pm V_{CC}$ = ±15V, V_{CM} = 12V		-75	75	nA	1
				-100	100	nA	2, 3
		$\pm V_{CC}$ = ±15V, V_{CM} = -12V		-75	75	nA	1
				-100	100	nA	2, 3
V_I	Input Voltage Range	$^+V_{CC}$ = 5V	(2), (3)	1.0	3.0	V	1, 2, 3
		$\pm V_{CC}$ = ±15V	(3)	-12	12	V	1, 2, 3
V_{Sat}	Output Saturation Voltage	$\pm V_{CC}$ = ±15V, I_O = 25mA, V_I ≤ -5mV	(1)		1.5	V	1, 2, 3
		$^+V_{CC}$ = 3.5V, $^-V_{CC}$ = -1V, V_I ≤ -6mV, I_O ≤ 3.2mA			0.4	V	1, 2
					0.6	V	3
A_V	Voltage Gain	$\pm V_{CC}$ = ±15V, Delta V_O = 12V, R_L = 1.4KΩ	(4)	10.5		K	4
			(4)	10		K	5, 6
		$^+V_{CC}$ = 5V, $^-V_{CC}$ = 0V, Delta V_O = 4.5V, R_L = 1.4KΩ	(2), (4)	8.0		K	4
			(2), (4)	5.0		K	5
			(2), (4)	5.8		K	6
CMRR	Common Mode Rejection Ratio	$\pm V_{CC}$ = ±15V, V_{CM} = ±12V		80		dB	4

(1) V_I ≥ 8mV at extremes for I_{Leak} and V_I ≤ −8mV at extremes for V_{Sat} (V_I to exceed V_{OS}.
(2) 5V differential across $+V_{CC}$ and $-V_{CC}$.
(3) Parameter guaranteed by V_{IO} and I_{IO} tests.
(4) K = V/mV.

LM119 Electrical Characteristics SMD 5962-9679801, HIGH DOSE RATE DC Parameters

The following conditions apply, unless otherwise specified. V_{CM} = 0V

Symbol	Parameter	Conditions	Notes	Min	Max	Units	Sub-groups
$+I_{CC}$	Positive Supply Current	$\pm V_{CC}$ = ±15V, V_O = Low V^+ = 5.6V thru 1.4KΩ			11	mA	1
					11.5	mA	2, 3
$-I_{CC}$	Negative Supply Current	$\pm V_{CC}$ = ±15V, V_O = Low V^+ = 5.6V thru 1.4KΩ		-4.2		mA	1
				-4.5		mA	2
				-6.0		mA	3
I_{Leak}	Output Leakage Current	$^+V_{CC}$ = 15V, $^-V_{CC}$ = -1V, V_{Gnd} = 0V, V_O = 35V	(1)		1.8	µA	1
			(1)		10	µA	2, 3
I_{IB}	Input Bias Current	$\pm V_{CC}$ = ±15V			0.475	µA	1
					0.95	µA	2, 3
		$^+V_{CC}$ = 5V	(2)		0.475	µA	1
			(2)		.95	µA	2, 3
V_{IO}	Input Offset Voltage	$^+V_{CC}$ = 5V, V_{CM} = 1V, $R_S \le 5K\Omega$	(2)	-3.8	3.8	mV	1
			(2)	-6.8	6.8	mV	2, 3
		$^+V_{CC}$ = 5V, V_{CM} = 3V, $R_S \le 5K\Omega$	(2)	-3.8	3.8	mV	1
			(2)	-6.8	6.8	mV	2, 3
		$\pm V_{CC}$ = ±15V, V_{CM} = 12V, $R_S \le 5K\Omega$		-3.8	3.8	mV	1
				-6.8	6.8	mV	2, 3
		$\pm V_{CC}$ = ±15V, V_{CM} = -12V, $R_S \le 5K\Omega$		-3.8	3.8	mV	1
				-6.8	6.8	mV	2, 3
I_{IO}	Input Offset Current	$^+V_{CC}$ = 5V, V_{CM} = 1V	(2)	-75	75	nA	1
			(2)	-100	100	nA	2, 3
		$^+V_{CC}$ = 5V, V_{CM} = 3V	(2)	-75	75	nA	1
			(2)	-100	100	nA	2, 3
		$\pm V_{CC}$ = ±15V, V_{CM} = 12V		-75	75	nA	1
				-100	100	nA	2, 3
		$\pm V_{CC}$ = ±15V, V_{CM} = -12V		-75	75	nA	1
				-100	100	nA	2, 3
V_I	Input Voltage Range	$^+V_{CC}$ = 5V	(2), (3)	1.0	3.0	V	1, 2, 3
		$\pm V_{CC}$ = ±15V	(3)	-12	12	V	1, 2, 3
V_{Sat}	Output Saturation Voltage	$\pm V_{CC}$ = ±15V, I_O = 25mA, $V_I \le$ -5mV	(1)		1.5	V	1, 2, 3
		$^+V_{CC}$ = 3.5V, $^-V_{CC}$ = -1V, $V_I \le$ -6mV, $I_O \le$ 3.2mA			0.4	V	1, 2
					0.6	V	3
A_V	Voltage Gain	$\pm V_{CC}$ = ±15V, Delta V_O = 12V, R_L = 1.4KΩ	(4)	10.5		K	4
			(4)	10		K	5, 6
		$^+V_{CC}$ = 5V, $^-V_{CC}$ = 0V, Delta V_O = 4.5V, R_L = 1.4KΩ	(2), (4)	8.0		K	4
			(2), (4)	5.0		K	5
			(2), (4)	5.8		K	6
CMRR	Common Mode Rejection Ratio	$\pm V_{CC}$ = ±15V, V_{CM} = ±12V		80		dB	4

(1) $V_I \ge$ 8mV at extremes for I_{Leak} and $V_I \le$ −8mV at extremes for V_{Sat} (V_I to exceed V_{OS}.
(2) 5V differential across $+V_{CC}$ and $-V_{CC}$.
(3) Parameter guaranteed by V_{IO} and I_{IO} tests.
(4) K = V/mV.

SMD 5962-9679801, HIGH DOSE RATE DC DELTA Parameters

The following conditions apply, unless otherwise specified.

V_{CM} = 0V, Delta calculations performed on QMLV devices at group B, subgroup 5 only.

Symbol	Parameter	Conditions	Notes	Min	Max	Units	Sub-groups
$+I_{CC}$	Positive Supply Current	$\pm V_{CC}$ = ±15V, V_O = Low V^+ = 5.6V thru 1.4KΩ		-1.0	1.0	mA	1
$-I_{CC}$	Negative Supply Current	$\pm V_{CC}$ = ±15V, V_O = Low V^+ = 5.6V thru 1.4KΩ		-0.5	0.5	mA	1
V_{IO}	Input Offset Voltage	$^+V_{CC}$ = 5V, V_{CM} = 1V, $R_S \le 5K\Omega$		-0.4	0.4	mV	1

SMD 5962-9679801, High Dose Rate 100K Post Radiation Parameters @ 25°C (1)

The following conditions apply, unless otherwise specified. V_{CM} = 0V

Symbol	Parameter	Conditions	Notes	Min	Max	Units	Sub-groups
I_{IB}	Input Bias Current	$\pm V_{CC}$ = ±15V			1.0	µA	1
		V_{CC} = 5V			1.0	µA	1
V_{IO}	Input Offset Voltage	$^+V_{CC}$ = 5V, V_{CM} = 1V, $R_S \le 5K\Omega$		-4.0	4.0	mV	1
		$^+V_{CC}$ = 5V, V_{CM} = 3V, $R_S \le 5K\Omega$		-4.0	4.0	mV	1
		$\pm V_{CC}$ = ±15V, V_{CM} = 12V, $R_S \le$ 5KΩ		-4.0	4.0	mV	1
		$\pm V_{CC}$ = ±15V, V_{CM} = −12V, $R_S \le$ 5KΩ		-4.0	4.0	mV	1

(1) Pre and post irradiation limits are identical to those listed under AC and DC electrical characteristics except as listed in the Post Radiation Limits Table. These parts may be dose rate sensitive in a space environment and demonstrate enhanced low dose rate sensitivity. Radiation end point limits for the noted parameters are guaranteed only for the conditions as specified in MIL-STD-883, per Test Method 1019, Condition A.

LM119 Electrical Characteristics SMD 5962-9679802, ELDRS FREE DC Parameters

The following conditions apply, unless otherwise specified. V_{CM} = 0V

Symbol	Parameter	Conditions	Notes	Min	Max	Units	Sub-groups
$+I_{CC}$	Positive Supply Current	$\pm V_{CC}$ = ±15V, V_O = Low V^+ = 5.6V thru 1.4KΩ			11	mA	1
					11.5	mA	2, 3
$-I_{CC}$	Negative Supply Current	$\pm V_{CC}$ = ±15V, V_O = Low V^+ = 5.6V thru 1.4KΩ		-4.2		mA	1
				-4.5		mA	2
				-6.0		mA	3
I_{Leak}	Output Leakage Current	$^+V_{CC}$ = 15V, $^-V_{CC}$ = -1V, V_{Gnd} = 0V, V_O = 35V	(1)		1.8	µA	1
			(1)		10	µA	2, 3
I_{IB}	Input Bias Current	$\pm V_{CC}$ = ±15V			0.475	µA	1
					0.95	µA	2, 3
		$^+V_{CC}$ = 5V	(2)		0.475	µA	1
			(2)		.95	µA	2, 3

(1) $V_I \ge$ 8mV at extremes for I_{Leak} and $V_I \le$ −8mV at extremes for V_{Sat} (V_I to exceed V_{OS}.

(2) 5V differential across $+V_{CC}$ and $-V_{CC}$.

LM119 Electrical Characteristics SMD 5962-9679802, ELDRS FREE DC Parameters (continued)

The following conditions apply, unless otherwise specified. V_{CM} = 0V

Symbol	Parameter	Conditions	Notes	Min	Max	Units	Sub-groups
V_{IO}	Input Offset Voltage	$^{+}V_{CC}$ = 5V, V_{CM} = 1V, $R_S \le 5K\Omega$	(2)	-3.8	3.8	mV	1
			(2)	-6.8	6.8	mV	2, 3
		$^{+}V_{CC}$ = 5V, V_{CM} = 3V, $R_S \le 5K\Omega$	(2)	-3.8	3.8	mV	1
			(2)	-6.8	6.8	mV	2, 3
		$\pm V_{CC}$ = ±15V, V_{CM} = 12V, $R_S \le 5K\Omega$		-3.8	3.8	mV	1
				-6.8	6.8	mV	2, 3
		$\pm V_{CC}$ = ±15V, V_{CM} = -12V, $R_S \le 5K\Omega$		-3.8	3.8	mV	1
				-6.8	6.8	mV	2, 3
I_{IO}	Input Offset Current	$^{+}V_{CC}$ = 5V, V_{CM} = 1V	(2)	-75	75	nA	1
			(2)	-100	100	nA	2, 3
		$^{+}V_{CC}$ = 5V, V_{CM} = 3V	(2)	-75	75	nA	1
			(2)	-100	100	nA	2, 3
		$\pm V_{CC}$ = ±15V, V_{CM} = 12V		-75	75	nA	1
				-100	100	nA	2, 3
		$\pm V_{CC}$ = ±15V, V_{CM} = -12V		-75	75	nA	1
				-100	100	nA	2, 3
V_I	Input Voltage Range	$^{+}V_{CC}$ = 5V	(3), (3)	1.0	3.0	V	1, 2, 3
		$\pm V_{CC}$ = ±15V	(3)	-12	12	V	1, 2, 3
V_{Sat}	Output Saturation Voltage	$\pm V_{CC}$ = ±15V, I_O = 25mA, $V_I \le$ -5mV	(1)		1.5	V	1, 2, 3
		$^{+}V_{CC}$ = 3.5V, $^{-}V_{CC}$ = -1V, $V_I \le$ -6mV, $I_O \le$ 3.2mA			0.4	V	1, 2
					0.6	V	3
A_V	Voltage Gain	$\pm V_{CC}$ = ±15V, Delta V_O = 12V, R_L = 1.4KΩ	(4)	10.5		K	4
			(4)	10		K	5, 6
		$^{+}V_{CC}$ = 5V, $^{-}V_{CC}$ = 0V, Delta V_O = 4.5V, R_L = 1.4KΩ	(5), (4)	8.0		K	4
			(5), (4)	5.0		K	5
			(5), (4)	5.8		K	6
CMRR	Common Mode Rejection Ratio	$\pm V_{CC}$ = ±15V, V_{CM} = ±12V		80		dB	4

(3) Parameter guaranteed by V_{IO} and I_{IO} tests.
(4) K = V/mV.
(5) 5V differential across $+V_{CC}$ and $-V_{CC}$.

SMD 5962-9679802, ELDRS FREE DC DELTA Parameters

The following conditions apply, unless otherwise specified.
V_{CM} = 0V, Delta calculations performed on QMLV devices at group B, subgroup 5 only.

Symbol	Parameter	Conditions	Notes	Min	Max	Units	Sub-groups
$+I_{CC}$	Positive Supply Current	$\pm V_{CC}$ = ±15V, V_O = Low V^+ = 5.6V thru 1.4KΩ		-1.0	1.0	mA	1
$-I_{CC}$	Negative Supply Current	$\pm V_{CC}$ = ±15V, V_O = Low V^+ = 5.6V thru 1.4KΩ		-0.5	0.5	mA	1
V_{IO}	Input Offset Voltage	$^{+}V_{CC}$ = 5V, V_{CM} = 1V, $R_S \le 5K\Omega$		-0.4	0.4	mV	1

SMD 5962-9679802, ELDRS FREE 100K Post Radiation Parameters @ 25°C (1)

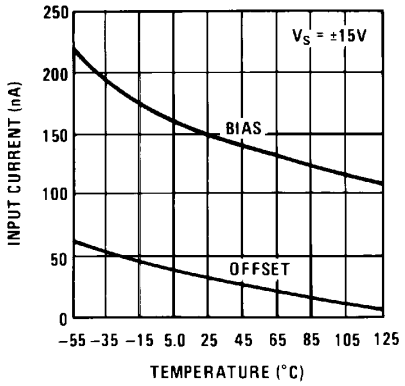
The following conditions apply, unless otherwise specified. V_{CM} = 0V

Symbol	Parameter	Conditions	Notes	Min	Max	Units	Sub-groups
I_{IB}	Input Bias Current	$\pm V_{CC}$ = ±15V			1.0	µA	1
		V_{CC} = 5V			1.0	µA	1
V_{IO}	Input Offset Voltage	$^{+}V_{CC}$ = 5V, V_{CM} = 1V, $R_S \leq 5K\Omega$		-4.0	4.0	mV	1
		$^{+}V_{CC}$ = 5V, V_{CM} = 3V, $R_S \leq 5K\Omega$		-4.0	4.0	mV	1
		$\pm V_{CC}$ = ±15V, V_{CM} = 12V, $R_S \leq 5K\Omega$		-4.0	4.0	mV	1
		$\pm V_{CC}$ = ±15V, V_{CM} = −12V, $R_S \leq 5K\Omega$		-4.0	4.0	mV	1

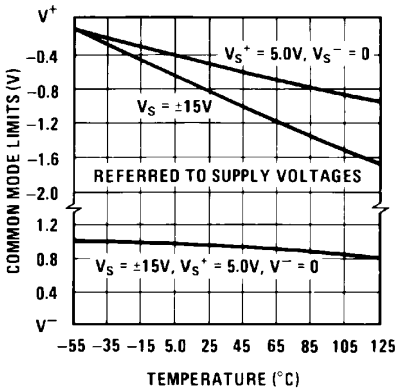
(1) Pre and post irradiation limits are identical to those listed under AC and DC electrical characteristics except as listed in the Post Radiation Limits Table. Low dose rate testing has been performed on a wafer-by-wafer basis, per Test Method 1019, Condition D of MIL-STD-883, with no enhanced low dose rate sensitivity (ELDRS).

Typical Performance Characteristics

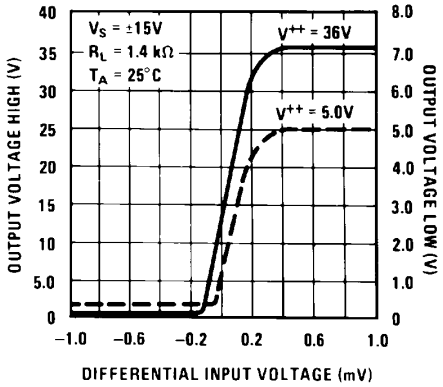
Input Currents



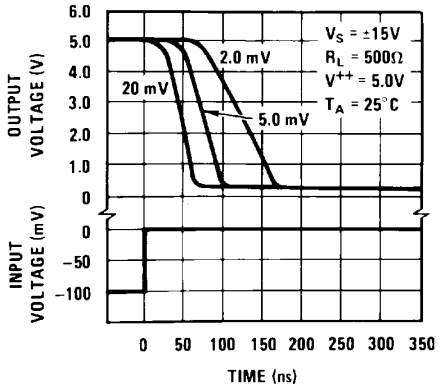
Common Mode Limits



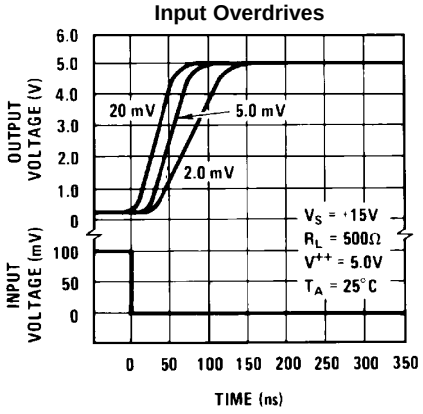
Transfer Function



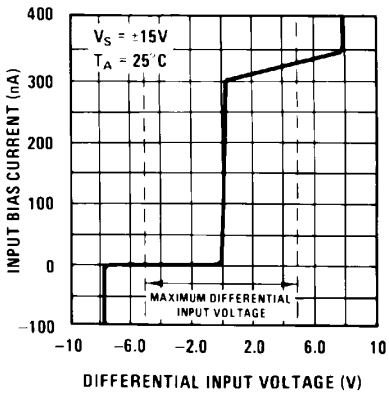
Response Time for Various Input Overdrives



Response Time for Various Input Overdrives

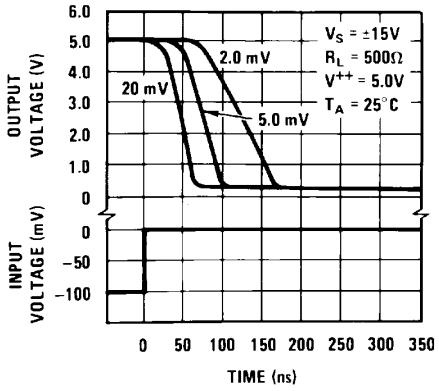


Input Characteristics

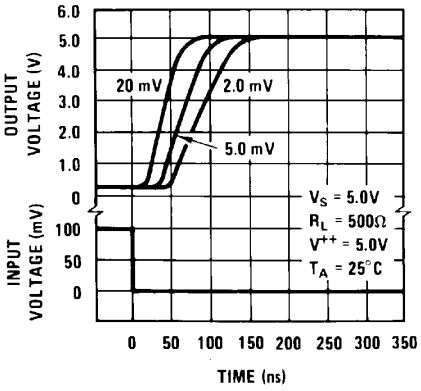


Typical Performance Characteristics (continued)

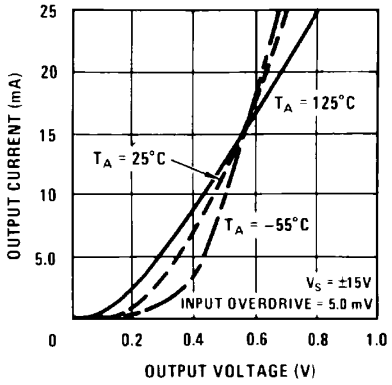
Response Time for Various Input Overdrives



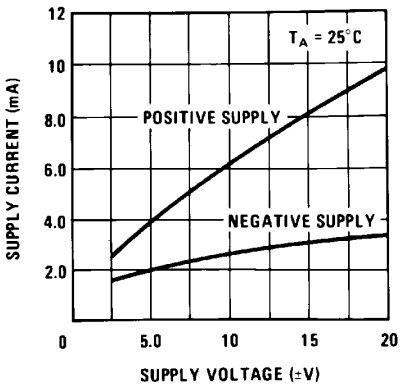
Response Time for Various Input Overdrives



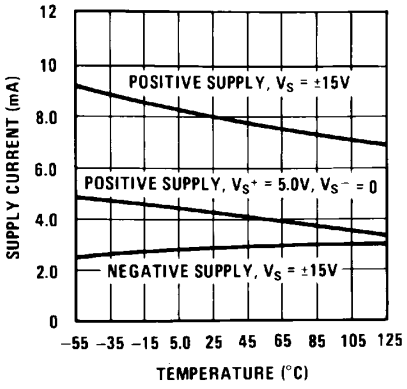
Output Saturation Voltage



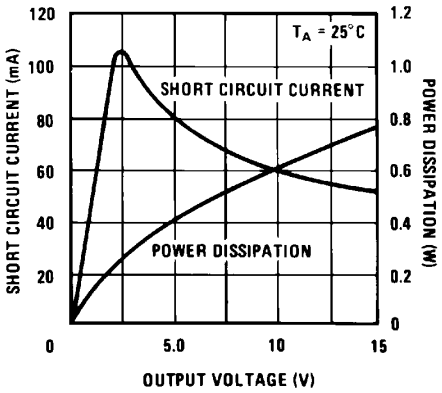
Supply Current



Supply Current

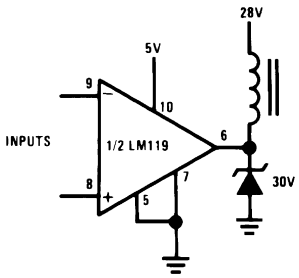


Output Limiting Characteristics



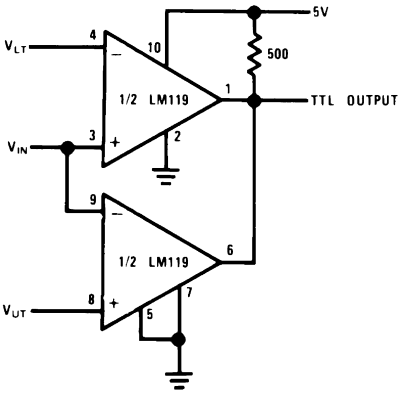
TYPICAL APPLICATIONS

Relay Driver



Pin numbers are for LME0010C package.

Window Detector



V_{OUT} = 5V for $V_{LT} \le V_{IN} \le V_{UT}$
V_{OUT} = 0 for $V_{IN} \le V_{LT}$or $V_{IN} \ge V_{UT}$

REVISION HISTORY

Date Released	Revision	Section	Originator	Changes
07/24/08	A	New release to corporate format	L. Lytle	2 MDS datasheets converted into one corporate data sheet format. Added Radiation information. MDS data sheets MNLM119-X Rev. 0F1 & MDLM119-X Rev 2A2 will be archived.
01/13/09	B	Features, Ordering Info., Electrical Section, Notes 13 and 14	Larry McGee	Added reference to ELDRS and Die NSID's to data sheet. Correction from: 100k rd(Si) to 100 krad(Si) in ordering info. Changed wording in Notes 13 and 14 Revision A will be Archived.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
5962-9679801VCA	ACTIVE	CDIP	J	14	25	TBD	A42 SNPB	Level-1-NA-UNLIM	-55 to 125	LM119J-QMLV 5962-9679801VCA Q	Samples
5962-9679801VIA	ACTIVE	TO-100	LME	10	20	TBD	POST-PLATE	Level-1-NA-UNLIM	-55 to 125	LM119H-QMLV 5962-9679801VIA Q ACO 5962-9679801VIA Q >T	Samples
5962R9679801VCA	ACTIVE	CDIP	J	14	25	TBD	A42 SNPB	Level-1-NA-UNLIM	-55 to 125	LM119JRQMLV 5962R9679801VCA Q	Samples
5962R9679801VHA	ACTIVE	CLGA	NAD	10	19	TBD	A42 SNPB	Level-1-NA-UNLIM	-55 to 125	LM119W RQMLV Q 5962R96798 01VHA ACO 01VHA >T	Samples
5962R9679801VIA	ACTIVE	TO-100	LME	10	20	TBD	POST-PLATE	Level-1-NA-UNLIM	-55 to 125	LM119HRQMLV 5962R9679801VIA Q ACO 5962R9679801VIA Q >T	Samples
5962R9679801VXA	ACTIVE	CLGA	NAC	10	54	TBD	Call TI	Level-1-NA-UNLIM	-55 to 125	LM119WG RQMLV Q 5962R96798 01VXA ACO 01VXA >T	Samples
5962R9679802VCA	ACTIVE	CDIP	J	14	25	TBD	A42 SNPB	Level-1-NA-UNLIM	-55 to 125	LM119JRLQMLV 5962R9679802VCA Q	Samples
5962R9679802VHA	ACTIVE	CLGA	NAD	10	19	TBD	A42 SNPB	Level-1-NA-UNLIM	-55 to 125	LM119W RLQMLV Q 5962R96798 02VHA ACO 02VHA >T	Samples
5962R9679802VIA	ACTIVE	TO-100	LME	10	20	TBD	Call TI	Call TI	-55 to 125	LM119HRLQMLV 5962R9679802VIA Q ACO 5962R9679802VIA Q >T	Samples
5962R9679802VXA	ACTIVE	CLGA	NAC	10	54	TBD	A42 SNPB	Level-1-NA-UNLIM	-55 to 125	LM119WG RLQMLV Q 5962R96798 02VXA ACO 02VXA >T	Samples
86014012A	ACTIVE	LCCC	NAJ	20	50	TBD	POST-PLATE	Level-1-NA-UNLIM	-55 to 125	LM119E -SMD Q	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
										5962-86014 012A ACO 012A >T	
8601401CA	ACTIVE	CDIP	J	14	25	TBD	A42 SNPB	Level-1-NA-UNLIM	-55 to 125	LM119J-SMD 5962-8601401CA Q	Samples
8601401HA	ACTIVE	CLGA	NAD	10	19	TBD	A42 SNPB	Level-1-NA-UNLIM	-55 to 125	LM119W -SMD Q 5962-86014 01HA ACO 01HA >T	Samples
8601401IA	ACTIVE	TO-100	LME	10	20	TBD	POST-PLATE	Level-1-NA-UNLIM	-55 to 125	LM119H-SMD 5962-8601401IA Q ACO 5962-8601401IA Q >T	Samples
LM119E-SMD	ACTIVE	LCCC	NAJ	20	50	TBD	POST-PLATE	Level-1-NA-UNLIM	-55 to 125	LM119E -SMD Q 5962-86014 012A ACO 012A >T	Samples
LM119E/883	ACTIVE	LCCC	NAJ	20	50	TBD	POST-PLATE	Level-1-NA-UNLIM	-55 to 125	LM119E /883 Q ACO /883 Q >T	Samples
LM119H-QMLV	ACTIVE	TO-100	LME	10	20	TBD	POST-PLATE	Level-1-NA-UNLIM	-55 to 125	LM119H-QMLV 5962-9679801VIA Q ACO 5962-9679801VIA Q >T	Samples
LM119H-SMD	ACTIVE	TO-100	LME	10	20	TBD	POST-PLATE	Level-1-NA-UNLIM	-55 to 125	LM119H-SMD 5962-8601401IA Q ACO 5962-8601401IA Q >T	Samples
LM119H/883	ACTIVE	TO-100	LME	10	20	TBD	POST-PLATE	Level-1-NA-UNLIM	-55 to 125	LM119H/883 Q ACO LM119H/883 Q >T	Samples
LM119HRLQMLV	ACTIVE	TO-100	LME	10	20	TBD	Call TI	Call TI	-55 to 125	LM119HRLQMLV 5962R9679802VIA Q ACO 5962R9679802VIA Q >T	Samples
LM119HRQMLV	ACTIVE	TO-100	LME	10	20	TBD	POST-PLATE	Level-1-NA-UNLIM	-55 to 125	LM119HRQMLV 5962R9679801VIA Q ACO 5962R9679801VIA Q >T	Samples
LM119J-QMLV	ACTIVE	CDIP	J	14	25	TBD	A42 SNPB	Level-1-NA-UNLIM	-55 to 125	LM119J-QMLV 5962-9679801VCA Q	Samples
LM119J-SMD	ACTIVE	CDIP	J	14	25	TBD	A42 SNPB	Level-1-NA-UNLIM	-55 to 125	LM119J-SMD	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
										5962-8601401CA Q	
LM119J/883	ACTIVE	CDIP	J	14	25	TBD	A42 SNPB	Level-1-NA-UNLIM	-25 to 85	LM119J/883 Q	Samples
LM119JRLQMLV	ACTIVE	CDIP	J	14	25	TBD	A42 SNPB	Level-1-NA-UNLIM	-55 to 125	LM119JRLQMLV 5962R9679802VCA Q	Samples
LM119JRQMLV	ACTIVE	CDIP	J	14	25	TBD	A42 SNPB	Level-1-NA-UNLIM	-55 to 125	LM119JRQMLV 5962R9679801VCA Q	Samples
LM119W-SMD	ACTIVE	CLGA	NAD	10	19	TBD	A42 SNPB	Level-1-NA-UNLIM	-55 to 125	LM119W -SMD Q 5962-86014 01HA ACO 01HA >T	Samples
LM119W/883	ACTIVE	CLGA	NAD	10	19	TBD	A42 SNPB	Level-1-NA-UNLIM	-55 to 125	LM119W /883 Q ACO /883 Q >T	Samples
LM119WGRLQMLV	ACTIVE	CLGA	NAC	10	54	TBD	A42 SNPB	Level-1-NA-UNLIM	-55 to 125	LM119WG RLQMLV Q 5962R96798 02VXA ACO 02VXA >T	Samples
LM119WGRQMLV	ACTIVE	CLGA	NAC	10	54	TBD	Call TI	Level-1-NA-UNLIM	-55 to 125	LM119WG RQMLV Q 5962R96798 01VXA ACO 01VXA >T	Samples
LM119WRLQMLV	ACTIVE	CLGA	NAD	10	19	TBD	A42 SNPB	Level-1-NA-UNLIM	-55 to 125	LM119W RLQMLV Q 5962R96798 02VHA ACO 02VHA >T	Samples
LM119WRQMLV	ACTIVE	CLGA	NAD	10	19	TBD	A42 SNPB	Level-1-NA-UNLIM	-55 to 125	LM119W RQMLV Q 5962R96798 01VHA ACO 01VHA >T	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Only one of markings shown within the brackets will appear on the physical device.

OTHER QUALIFIED VERSIONS OF LM119QML, LM119QML-SP :

- Military: LM119QML
- Space: LM119QML-SP

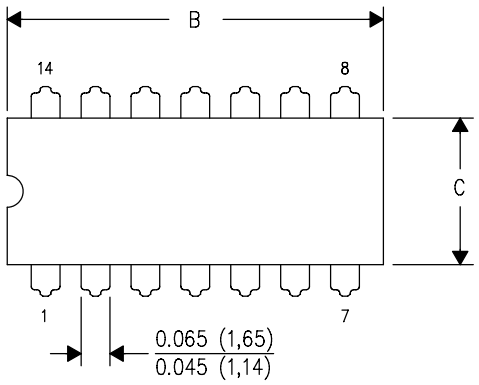
NOTE: Qualified Version Definitions:

- Military - QML certified for Military and Defense Applications
- Space - Radiation tolerant, ceramic packaging and qualified for use in Space-based application

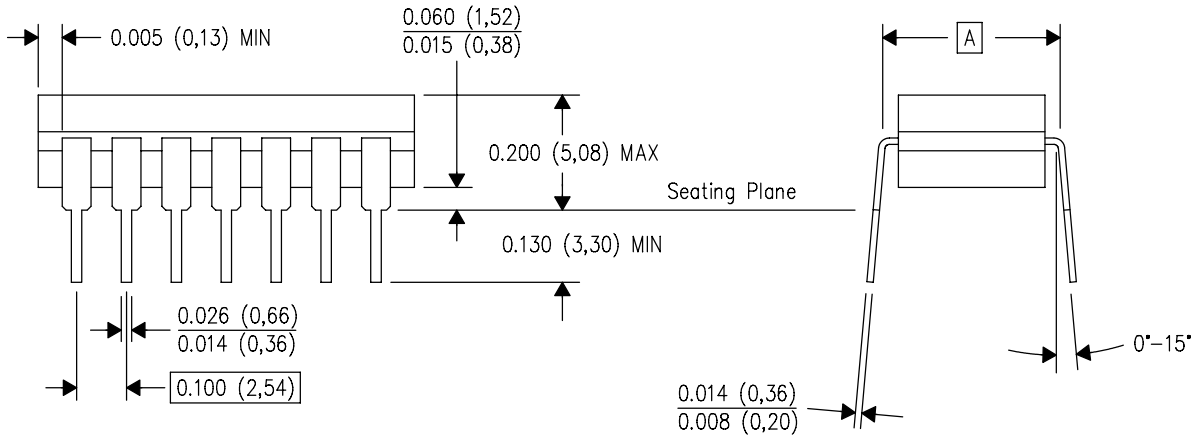
J (R–GDIP–T**)

14 LEADS SHOWN

CERAMIC DUAL IN–LINE PACKAGE



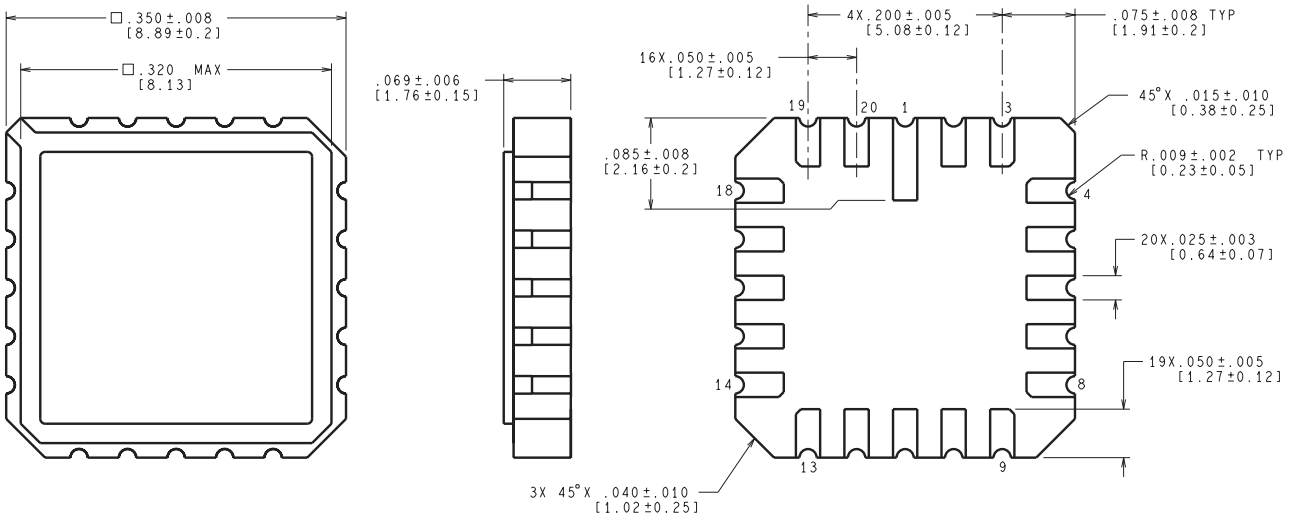
DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

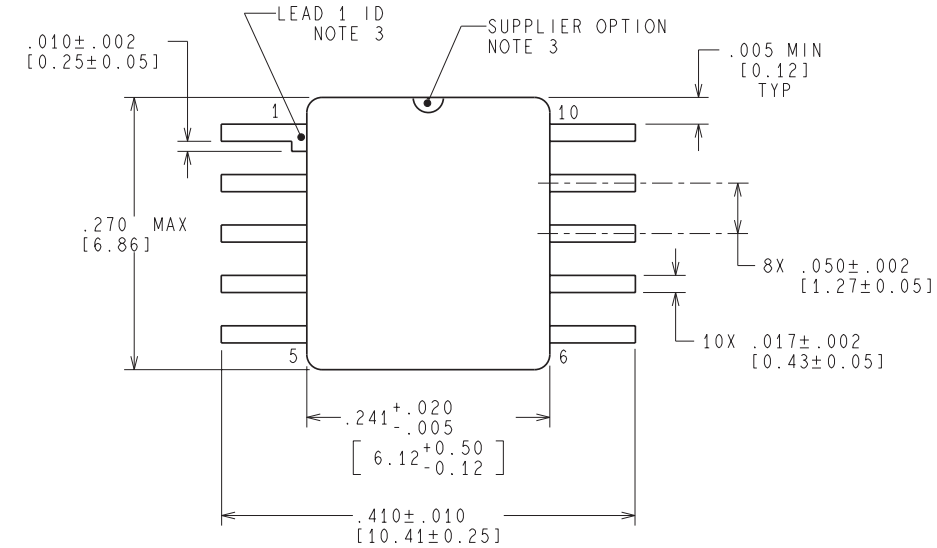
NAJ0020A

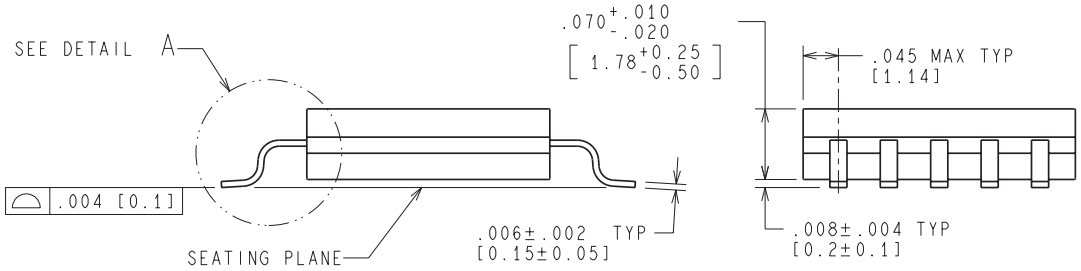


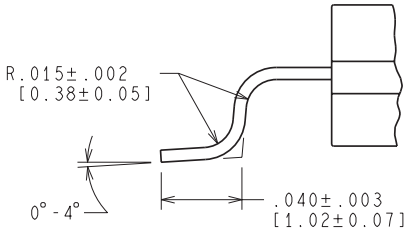
CONTROLLING DIMENSION IS INCH
VALUES IN [ ] ARE MILLIMETERS

E20A (Rev F)

NAC0010A





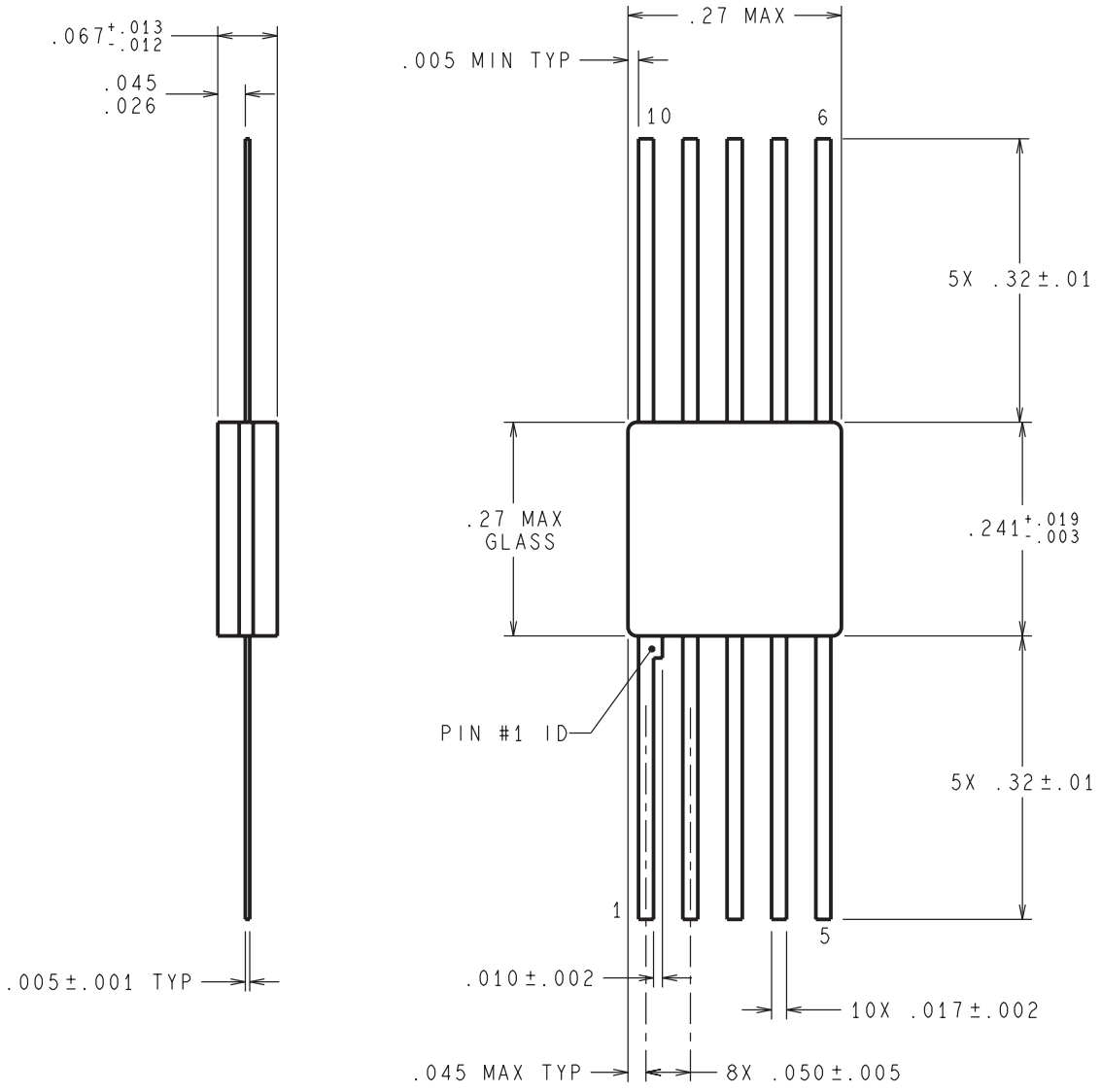


DETAIL A
TYPICAL

MIL-PRF-38535
CONFIGURATION CONTROL

WG10A (Rev H)

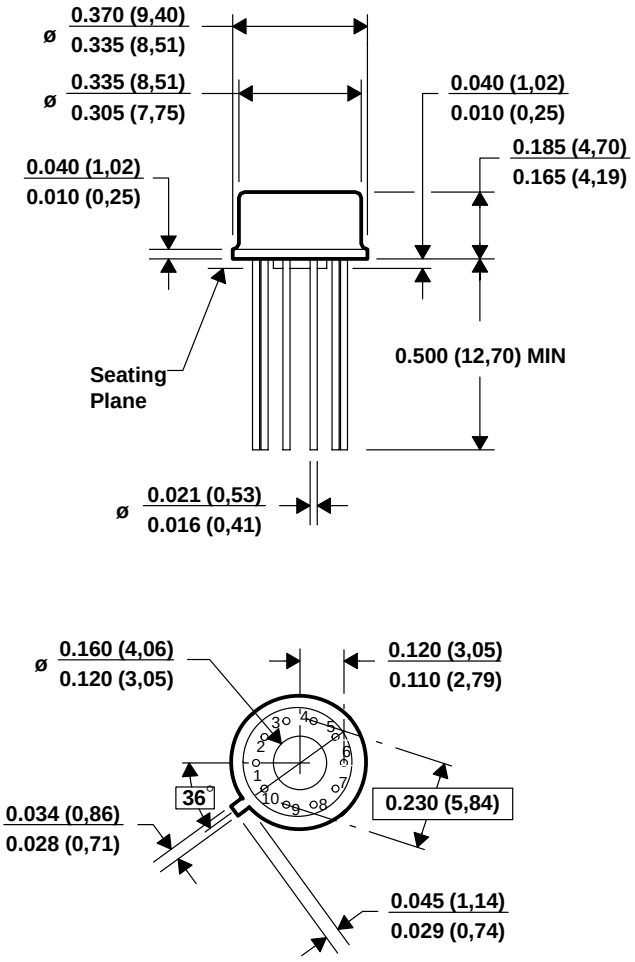
NAD0010A



DIMENSIONS ARE IN INCHES

W10A (Rev H)

LME (O–MBCY–W10) **METAL CYLINDRICAL PACKAGE**



4202488/A 03/01

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Leads in true position within 0.010 (0,25) R @ MMC at seating plane.
D. Pin numbers shown for reference only. Numbers may not be marked on package.
E. Falls within JEDEC MO–006/TO-100.

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Only those TI components which TI has specifically designated as military grade or “enhanced plastic” are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have ***not*** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

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