LM1572 1.5A, 500kHz Step-down Voltage Regulator

Check for Samples: LM1572

FEATURES

- **500kHz Clock Allows Small, Surface Mount Components**
- **150mΩ MOSFET Switch**
- **Ensured Load Current of 1.5A**
- **Current Mode Control**
- **Programmable Soft-Start**
- **Internally Set Slope Compensation**
- **TTL Compatible Shutdown**
- **Fixed 5V, 3.3V or Adjustable Output**
- **Low Shutdown Supply Current of 26µA**
- **Cycle-by-Cycle Current Limit**
- **Short-Circuit Protection and Thermal Protection**
- **TSSOP Package**

APPLICATIONS

- **LCD Monitors and TVs**
- **Set-Top Boxes**
- **Cable Modems**
- **Down Conversion from 12V in Local/Distributed Systems**

DESCRIPTION

The LM1572 is a 500kHz step-down (buck) switching voltage regulator capable of driving up to 1.5A in to a load while occupying a very small PCB area. Current Mode Control results in superior transient response and regulation over a wider range of operating conditions. TI's advanced analog bipolar, CMOS plus DMOS process enables high efficiency at high switching frequency, and the internal 150mΩ MOSFET switch provides more power from a smaller package.

The LM1572 has programmable soft-start and frequency foldback to limit the inrush current, and a TTL compatible shutdown for easy sequencing. It draws 2.3mA of supply current in standby mode, and only 26µA in shutdown mode. The LM1572 is available in a TSSOP package with an adjustable output or fixed outputs of 5V and 3.3V. The adjustable version can be set between 2.42V and 5V.

Typical Applications (Fixed/Adjustable Voltage Parts)

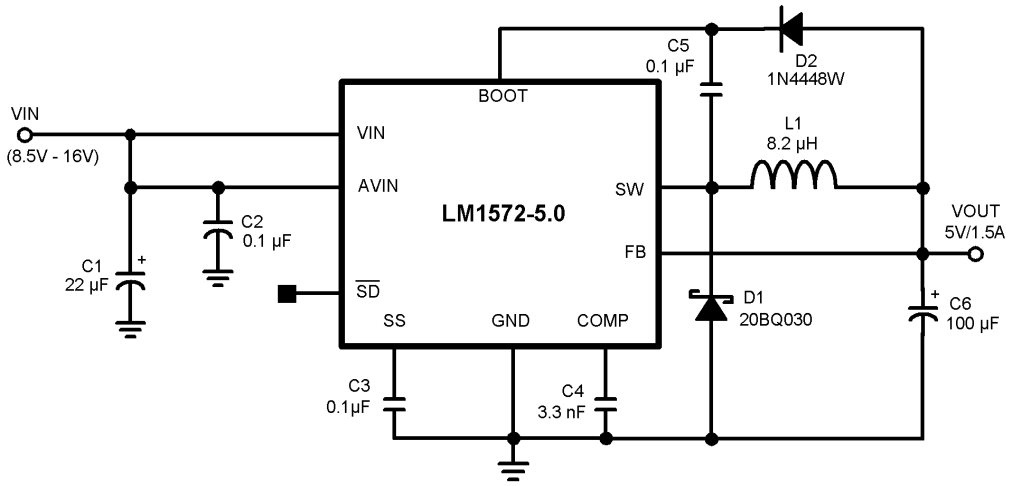


Figure 1.

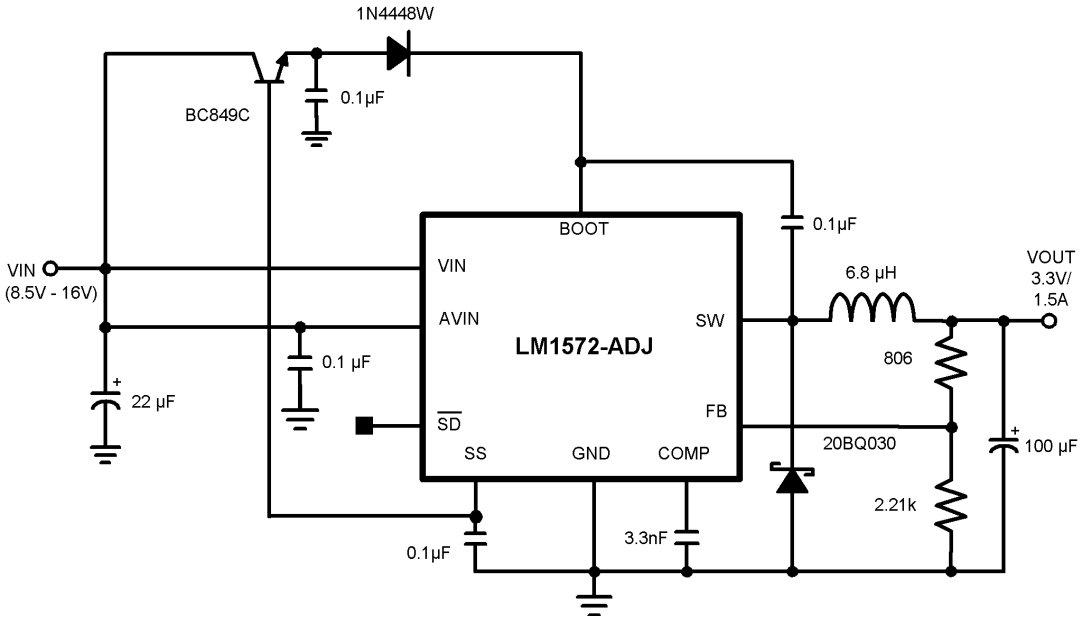
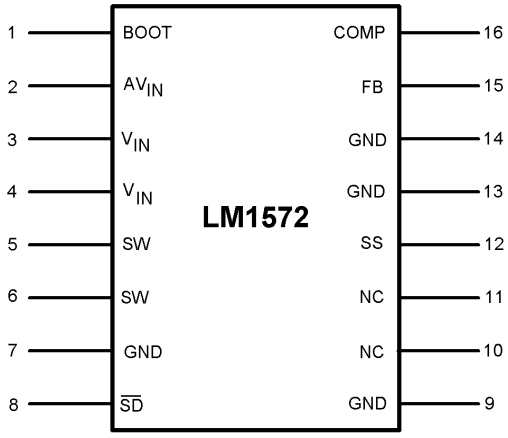


Figure 2.

Connection Diagram



16-Lead TSSOP
See Package Number PW

PIN DESCRIPTION

BOOT (Pin 1) - Bootstrap pin. It provides the upper rail for the floating driver stage of the internal MOSFET switch, the lower rail being the switching node (Pins 5 and 6). A small decoupling capacitor (typically 0.1µF-0.22µF) is therefore connected between the Bootstrap pin and the switching node. This capacitor should be 0.18µF-0.22µF for applications with an output voltage greater than 3.3V, if the minimum load (including the current drawn by internal/external feedback resistor divider) is less than 1mA. Additional drive voltage is provided by connecting this pin directly to the 5V output rail via a diode as shown in the Typical Application Circuit for the fixed voltage part. The same method can be used for an adjustable part provided the part is adjusted for an output of 5V. For other output voltages (between 2.42V to 5V) a more general method of providing this external drive voltage is illustrated in the Typical Application Circuit for the adjustable part. Note that the NPN signal transistor shown, must have a specified hfe greater than 400. Damage can occur to Pin 1 if it is connected (via a diode) to any external voltage source greater than 6V.

AV_{IN} (Pin 2) - This is the Analog V_{IN} and provides the supply to the internal control circuitry, the (Power) V_{IN} pins (Pins 3,4) providing the supply to the internal power stage. In the simplest layout scheme, the Analog V_{IN} pin can simply be connected to the V_{IN} pins directly on the pads where the IC is mounted. But for better noise rejection the trace to Pin 2 can be routed separately from the (Power) V_{IN} trace, starting from the positive terminal of the input capacitor. A simple RC filter solution can also be used for better results, particularly at low input voltages. This consists of a 10Ω resistor connected between Analog V_{IN} and V_{IN}, and a 0.47µF capacitor between Analog V_{IN} and Ground. Note that if this RC filter is used, a 1MΩ resistor between Pin 1 and Ground is also required.

V_{IN} (Pins 3,4) - This is the input supply to the power stage (connected to the Drain of the switching MOSFET). To aid thermal dissipation from the die, two pins are used for this function. Both these pins must be connected together, very close to the IC, onto a large PCB copper plane.

SW (Pins 5,6) - This is the Source of the internal switching MOSFET and forms the 'switching node' of the buck converter. These two pins should be connected together on the PCB close to the IC. The length of the trace from this node to the cathode of the catch diode, and from the anode of the diode to the IC ground must be kept very small. The maximum inductance connected to the switching node (for any application) is recommended to be 15µH. See the Inductor Selection procedure for more details.

GND (Pins 7,9,13,14) - This is the Ground for the IC and for the input and output rails of the buck converter. To aid thermal dissipation from the die, four pins are used for this function. Connect as many as possible of these ground pins together, close to the IC onto a large PCB copper plane. A two-sided PCB with one side serving as a 'ground plane' is strongly recommended. The ground pins must then connect to the ground plane very close to the IC through several vias. The vias also serve to transfer heat to the other side of the board for better thermal management.

SD (Pin 8) - Shutdown/Standby/UVLO Pin. This pin actually has two thresholds. If it is taken below 2.38V (typical), the switch turns off and the output of the converter falls to zero.This is the 'standby mode'. The internal circuitry of the IC remains active, continuing to draw about 2.3mA from the input. If the voltage on this pin is lowered below 1V (typical), the IC enters 'shutdown mode' drawing only 26 µA from the input. Above 2.38V, the switching action resumes, and so this pin can also be used to set an undervoltage lockout threshold (UVLO) for the input rail. If this pin is not intended to be used actively, it can be left floating to allow continuous switching. The voltage on this pin should not exceed 7V to avoid damage.

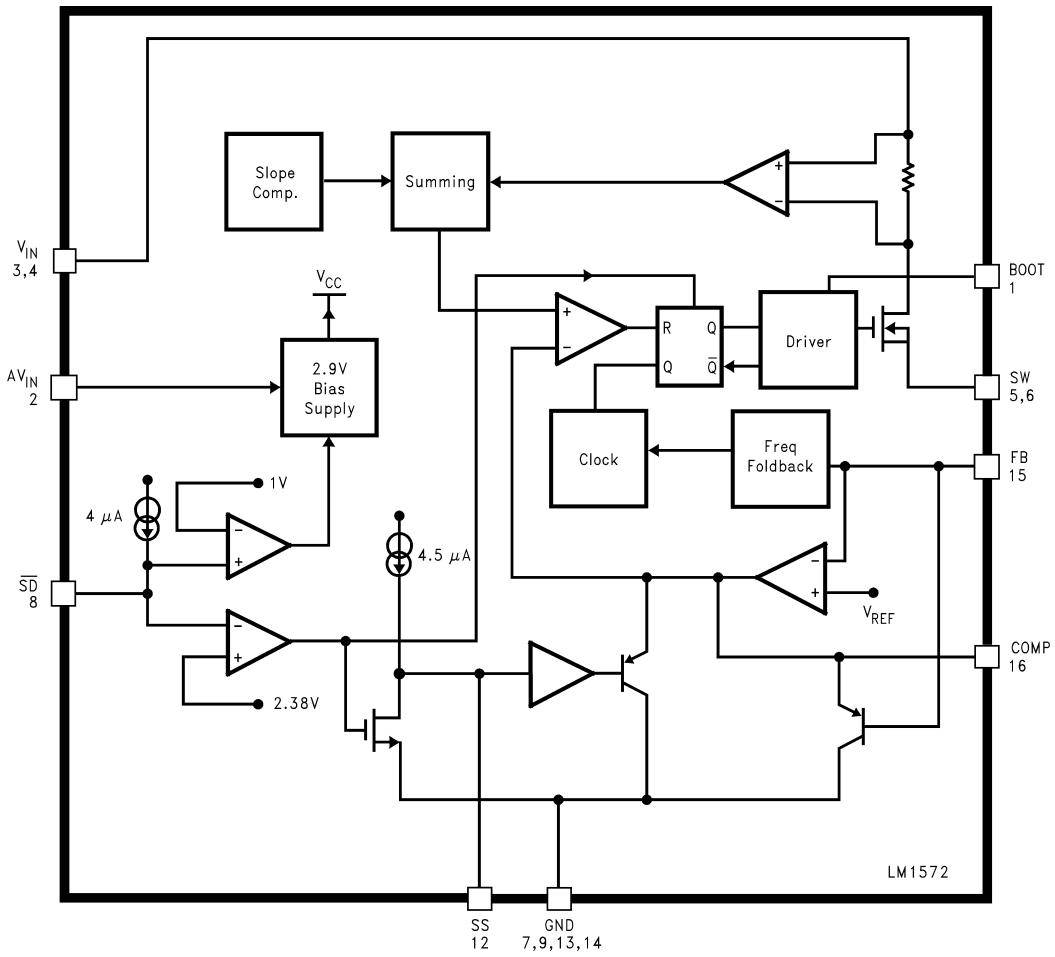
NC (Pins 10,11) - No Internal Connection.

SS (Pin 12) - Softstart pin. A small capacitor connected from this pin to ground programs the amount of softstart. This capacitor charges up by means of an internal 4.5µA current source, during power-up, and also whenever the output of the converter is enabled. The allowed duty cycle increases slowly as the capacitor charges, reaching the maximum allowed when the voltage on this pin approaches 2V. The capacitor continues to charge, finally reaching 6V, at which level it is internally clamped. This pin is internally forced to ground (to discharge the softstart capacitor and to reset the softstart function) whenever the shutdown pin is taken below 2.38V. If the softstart feature is not required, the softstart pin can be left floating.

FB (Pin 15) - This is the feedback pin for the IC and is used to set the output of the converter to regulate to the desired value. For the fixed voltage part this pin is normally connected directly to the output. For the adjustable part, a resistive divider is used between the output and ground, so that the voltage on this pin is 2.42V when the output is at the required level. For fixed voltage parts, the internal divider draws about 0.5mA, a consideration possibly affecting the choice of the bootstrap capacitor (see description of Pin 1 above).

COMP (Pin 16) - This is the output of the error transconductance amplifier and is used for frequency compensation of the feedback loop. A small capacitor from this pin to ground (about 3.3nF to 6.8nF) provides the simplest loop compensation, but a series resistor-capacitor combination (R between 1k to 1.5k) may also be used to improve the phase margin/crossover frequency of the loop. The voltage on this pin is at about 1V at very light loads. Under very heavy loads or under output short-circuit, the voltage on this pin clamps to 2V, and the converter enters protective foldback. The IC automatically recovers from this mode when the load is reduced.

Block Diagram



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings(1)(2)

ESD Tolerance(3)	2kV
Input Voltage	17V
SD Pin Voltage	7V
FB Pin Voltage (All Options)	7V
Storage Temp. Range	−65°C to 150°C
Junction Temperature	150°C

(1) Absolute maximum ratings indicate limits beyond which damage to the device may occur. Operating ratings indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For ensured specifications and the test conditions, see the Electrical Characteristics.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office / Distributors for availability and specifications.
(3) This is for the human body model, which is a 100pF capacitor discharged through a 1.5k resistor into each pin.

Operating Ratings

Supply Voltage (V_{IN})(1)	8.5V to 16V
Junction Temperature Range	−40°C to +125°C
Package Thermal Resistance (TSSOP)(2)	130°C/W

(1) Minimum input voltage is defined as the voltage where internal bias lines are still regulated so that the reference voltage and oscillator remain constant. Actual minimum input voltage to maintain output in regulation depends on output voltage and load current. In particular, the required duty cycle must be less than the lowest possible upper duty cycle limit of the controller (D_{MAX} = 0.86). The maximum input voltage will also depend on output voltage and load current. In particular, the required duty cycle must be greater than the lowest possible duty cycle limit of the controller (D_{MIN} = 0.15), estimated from the typical minimum on-time, which is about 300ns.
(2) Junction to Ambient thermal resistance with the TSSOP package soldered on a 1oz. printed circuit board with copper area of approximately 1in^2.

Electrical Characteristics

Unless otherwise specified, all limits are ensured for T_A = 25°C, V_{IN} = 15V, V_{COMP} = 1.5V, V_{SD} = 5V, I_{LOAD} = 0A, unless otherwise noted. **Boldface** apply over the temperature extremes. 'V_{FB} low (high)' is 0.95 (1.05) times the nominal value at regulation.

Symbol	Parameter	Conditions		Min(1)	Typ(2)	Max(1)	Units
V_{FB_ADJ}	Voltage on Feedback pin (Adjustable version in regulation)			2.37 **2.35**	2.42	2.49 **2.5**	V
V_{FB_5}	Voltage on Feedback pin (Fixed 5V version in regulation)			4.85 **4.8**	5.0	5.15 **5.2**	V
$V_{FB\_3.3}$	Voltage on Feedback pin (Fixed 3.3V version in regulation)			3.22 **3.16**	3.3	3.4 **3.44**	V
$\Delta V_{FB}/V_{IN}$	Feedback Voltage Line Regulation	V_{IN} = 8.5V to V_{IN} = 16V		−0.05	0	0.05	%/V
I_{FB_REG}	Feedback Pin Bias Current (Adjustable Part)	V_{FB} at regulation		**0**	0.5	**1.5**	µA
AV_{ERROR}	Error Amplifier Voltage Gain(3)				350		
gm_{EA}	Error Amplifier Transconductance(3)			1100 **800**	2000	2700 **3200**	µMho
gm_{COMP_SW}	Comp Pin to Switch Current Transconductance				2		A/V
I_{EA_SOURCE}	Error Amplifier Source Current	V_{FB} low		**50**	200	**300**	µA
I_{EA_SINK}	Error Amplifier Sink Current	V_{FB} high			2.4		mA
V_{COMP_TH}	Comp Pin Switching Threshold	Duty Cycle = 0			0.9		V
V_{COMP_LIM}	Comp Pin High Clamp				2		V
I_{CLIM}	Switch Current Limit	V_{BOOT} = V_{SW} + 5V, Comp Open, V_{FB} low	D≤ 0.5	**2.0**	2.7	**3.2**	A
			D = 0.8	**1.75**	2.4	**3**	
R_{DS}	Switch ON Resistance	I_{SW} = 1.5A,V_{BOOT} = V_{IN} + 5V			0.15	0.4 **0.5**	Ω
D_{MAX}	Maximum Duty Cycle(4)	Comp Open, V_{FB} low		**86**	94		%
f_{SW}	Switch Frequency	V_{FB} low,V_{COMP} = 1V,	Full Temp. Range	**400**	500	**570**	kHz
			-20°C ≤ T_J ≤ 125°C	440		560	
f_{REG}	Switch Frequency Line Regulation	V_{IN} = 8.5V and V_{IN} = 16V,V_{FB} low,V_{COMP} = 1V			0.01		%/V
$\Delta f_{FOLDBACK}$	Foldback Frequency shift (Adjustable part)	V_{FB} = 0.8V, V_{COMP} = 1V		20	90	160	kHz
I_{SS}	Softstart Pin Current	V_{SS} = 1V,V_{FB}=0V		**2.5**	4.5	**8**	µA
I_{SD}	Shutdown Supply Current	V_{SD} = 0V,V_{COMP} = 1V,V_{FB} low			26	52 **75**	µA
I_{STDBY}	Standby Supply Current	V_{SD} = 1.5V, Comp Open			2.3	4 **4.3**	mA
V_{UVLO}	Undervoltage Lockout Threshold	Comp Open, V_{FB} low		**2.2**	2.38	**2.5**	V
V_{SD}	Shutdown Threshold	Comp Open, V_{COMP} = 1V,V_{FB} low		**0.75**	1.0	**1.28**	V

(1) All limits specified at room temperature (standard face type) and at **temperature extremes (bold face type)**. All room temperature limits are 100% production tested. All limits at **temperature extremes** are ensured via correlation using Statistical Quality Control (SQC) methods. All limits are used to calculate Average Outgoing Quality Level (AOQL).
(2) Typical numbers are at 25°C and represent the most likely norm.
(3) Transconductance and voltage gain refer to the internal amplifier, excluding any voltage divider as is present on the fixed voltage parts. To calculate the gain and transconductance for the fixed voltage parts, divide values shown in table by the ratio V_{FB_5}/2.42 = 2.07 for the 5V part and by $V_{FB\_3.3}$/2.42 = 1.36 for the 3.3V part.
(4) To ensure stable operation, the maximum recommended operating duty cycle is 80%.

Typical Performance Characteristics

Efficiency ($3.3V_{OUT}$)

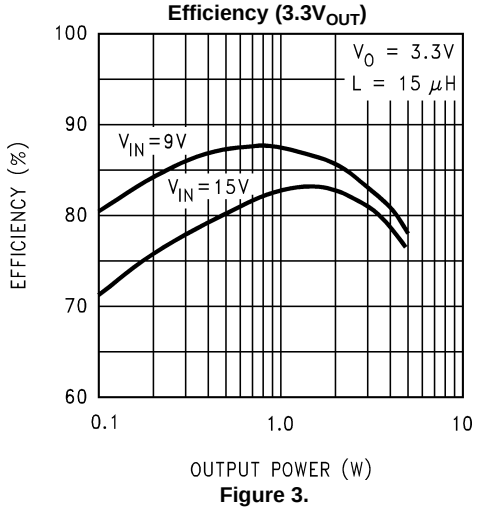


Figure 3.

Characteristics of Switch

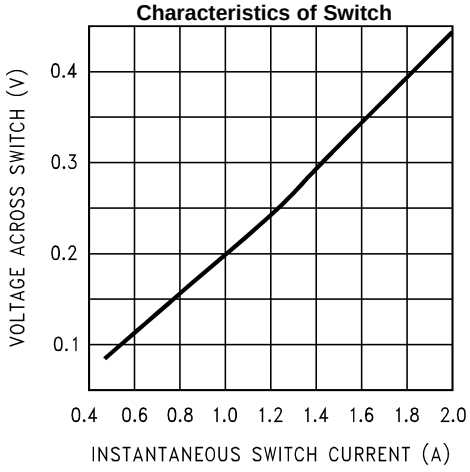


Figure 4.

Efficiency ($5V_{OUT}$)

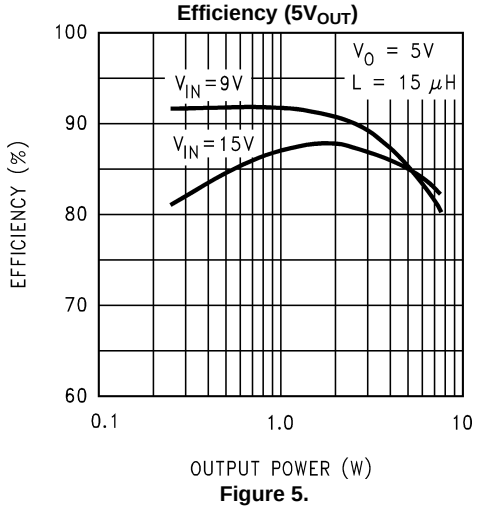


Figure 5.

Supply Current vs Load

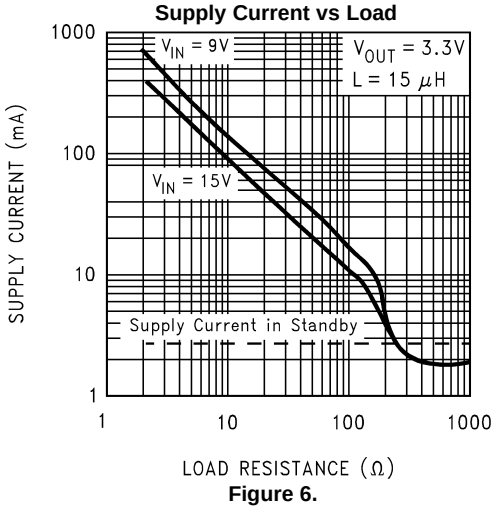


Figure 6.

Supply Current vs Voltage on Shutdown Pin

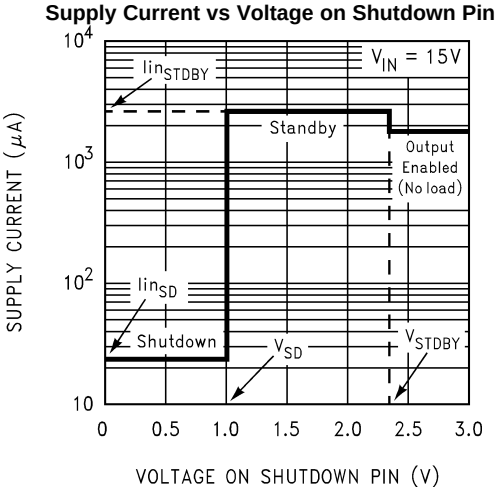


Figure 7.

Characteristics of Shutdown Pin

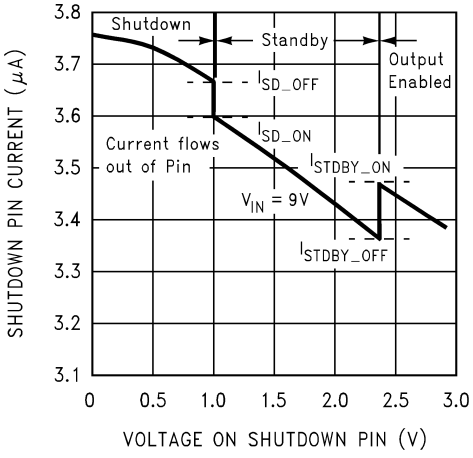


Figure 8.

Typical Performance Characteristics (continued)

Shutdown Pin Current at Shutdown Threshold

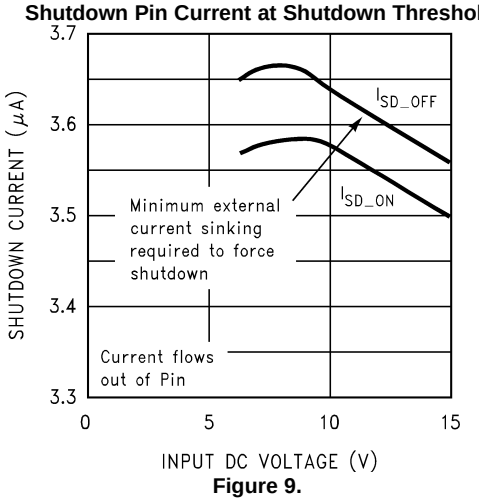


Figure 9.

Shutdown Supply Current vs Input Voltage

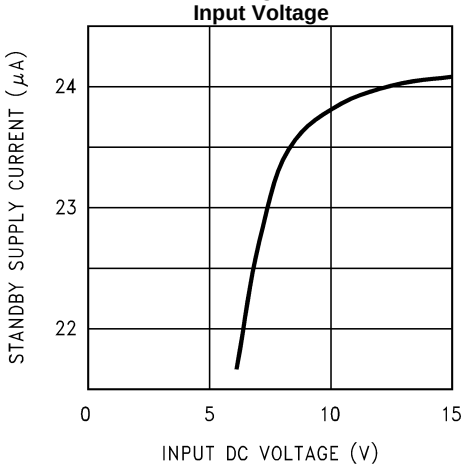


Figure 10.

Frequency Foldback

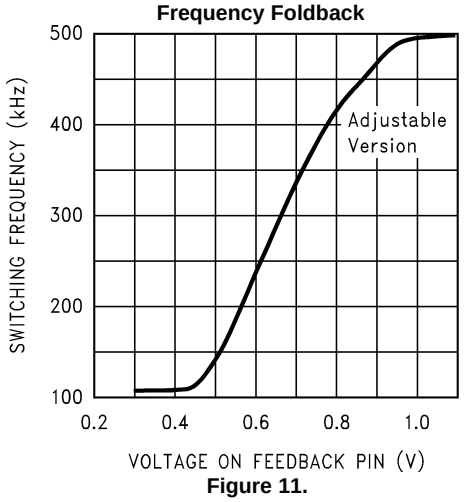


Figure 11.

Characteristics of Feedback Pin

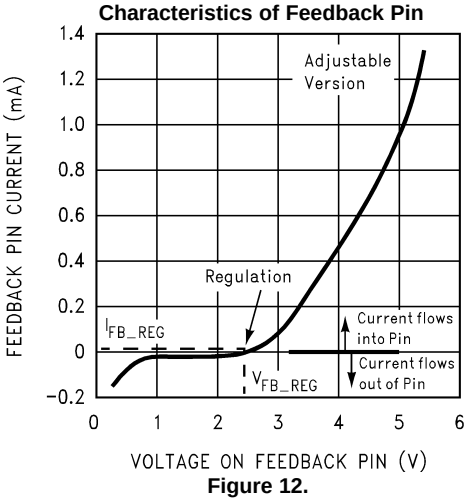


Figure 12.

Operating Feedback Pin Current vs Input Voltage

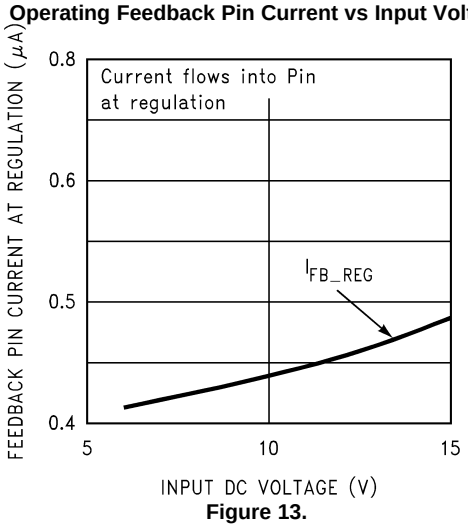


Figure 13.

APPLICATION INFORMATION

Resistive Divider Calculation

For the adjustable part, the voltage on the feedback pin is set to 2.42V under regulation. This is achieved by means of a resistive divider, as indicated in the Typical Applications for the adjustable part. Designating the upper resistor as 'R_2' (connected to the output) and the lower resistor as 'R_1' (connected to ground), the following equation (Equation 1) relates R_1, R_2 and the output voltage level V_O :

$$R_2 = R_1 \cdot \left[\frac{V_O}{2.42} - 1 \right] \quad (1)$$

Setting the lower resistor to 2.21k (which is a standard resistance value), the upper resistor is chosen as 806 ohms for a 3.3V output and as 2.37k for a 5V output. This should suffice for most applications. However the more experienced designer may like to know more about the rather overlooked intricacy of selecting resistors especially in regard to the resultant error in the output voltage. It is also helpful to consider the other factors affecting the tolerance of the output voltage. This is discussed under 'Tolerance of set Output Voltage' at the end of 'Application Information'. Note that if the lower resistor is set to 2.21k, the divider current is greater than 1mA, so a 0.1µF boostrap will always suffice (see for Pin 1 and Pin 15 above).

Inductor Selection

Inductor selection for buck converters is discussed in great detail in AN-1197 (SNVA038), to which the reader can refer to for a deeper understanding. It must be understood that though the scope of the above Application Note is limited to buck converters that rely on voltage mode control, all the considerations contained therein also apply to buck converters relying on current mode control, such as the LM1572. In fact, with current mode control, there are additional considerations that may apply which need to be discussed here.

The basic requirement for any converter is that it should be able to deliver the required power without hitting the current limit of the switch. This is ensured by having an inductance large enough to limit the peak current (this is obviously not feasible if the required load current is very close to or larger than the current limit!). In the LM1572, a 'slope compensation' ramp is also summed-in with the switch current ramp, for duty cycles greater than 0.5. The reason for this slope compensation will be explained later below, here it suffices to realize that it affects the effective current limit for duty cycles greater than 0.5. From the Electrical Characteristics it can be seen that the current limit I_{CLIM} is stated as two terms: one for D less than (or equal to) 0.5, and one for D = 0.8. Since the current limit falls off at high duty cycles/low input voltage due to the slope compensation, a peak power calculation should generally be done both at the highest and the lowest input voltage, so as to ensure that the inductance is large enough to cover the entire desired operating input voltage range.

The overall strategy here is to determine various 'minimum inductances' based on all different considerations (as applicable), and to then pick the largest of all the 'minimums' so as to satisfy each of the conditions.

It is noted here that there can also be an 'optimum' value for the inductance, one which offers a compromise solution for reducing the overall size of the power converter, the magnetics and capacitors included. However, since the primary reason for going to higher switching frequencies is to reduce the size of the magnetics alone, 'optimization' may be relegated to a lower priority, as in the example to follow.

In (peak) current mode control, the main additional consideration is the phenomenon of subharmonic instability (also called alternate cycle or half-frequency oscillations). This is fundamental to the topology, and no amount of 'tweaking' the compensation resistor/capacitor values will circumvent it. The well known solution is to add a certain amount of 'slope compensation', the value of which is directly related to the inductance being used. Higher inductance requires smaller slope compensation. If the slope compensation is fixed, as for the LM1572, it is the inductance that needs to be controlled. Then higher slope compensation requires smaller inductance. This defines a 'minimum' value of inductance required to avoid subharmonic instability. The value can therefore be exceeded. If for example the first priority in a given application is not the size of the inductor, but the reduction of output ripple, a higher than the minimum inductance may be selected. But too high an inductance, for a given slope compensation (or equivalently too much of slope compensation for a given inductance), will cause the loop response to become more and more that of voltage mode control, eventually making it slower and harder to compensate. For any LM1572 design therefore, the maximum recommended inductance is 15µH, irrespective of input or output conditions.

For the LM1572, the slope compensation can vary (from device to device) over the range 0.42 to 0.75 A/µs. A little thought will lead to the conclusion that any calculation for the minimum inductance (required to avoid subharmonic instability), must be carried out at its 'worst-case': which is the lower limit of the slope compensation (i.e. 0.42 A/µs). This also happens to be the value used for peak power calculation since it corresponds to the lower limit of current limit (2A). The value of 0.75 A/µs can be used to check if the slope compensation is not 'excessive' in the sense discussed above.

The effective current limit, 'I_{CLIM}' (see Electrical Characteristics) is the sum of two terms. The first is the basic preset current limit (the flat part) , which we call 'I_{CL}' here, and is the value given for 'I_{CLIM}' for D ≤ 0.5). Superimposed on this is the effect of slope compensation. This causes the current limit to fall (almost linearly) for D > 0.5. In general, the slope compensation can be expressed as 'm_C' in units of A/µs. From D = 0.5 to a projected value of D = 1 (a time interval of 1µs), the current limit would therefore fall exactly by m_C Amps. At D = 0.8 the current limit falls by 3/5th of this i.e. by m_C*0.6. So the current limit at D = 0.8 would be $I_{CL} - (0.6*m_C)$. This value ('I_{CLIM}' for D = 0.8) is also given in the Electrical Characteristics tables.

As mentioned, the inductance must be chosen to be higher than the minimum value corresponding to the condition of peak calculated switch current equal to the current limit. The worst case must be used here: i.e. the 'min' of current limit values in the Electrical Characteristics (not 'typ'). Further, it should be confirmed over the entire input voltage range (or duty cycle) that the peak current does not attempt to exceed the effective current limit. This is easily carried out using the same general strategy: by calculating the minimum inductance at both input voltage extremes, and then choosing the greater of the two calculated 'minimum' inductances.

It should also be remembered that subharmonic instability can only occur when several conditions are simultaneously satisfied: (peak) current mode control, duty cycle greater than (or around) 0.5, and continuous conduction mode. Subharmonic instability is not of concern if any one or more of the above conditions are not true. And in that case, the inductor selection considerations become identical to those for voltage mode control. Note that the worst case condition to check for subharmonic instability, and/or to choose an inductance large enough to prevent these oscillations, is at the lowest desired input voltage.

Designing for discontinuous conduction mode is clearly an attractive option for some experienced designers. One reason for this is that subharmonic instability is then of no concern. However discontinuous mode is possible only if the maximum load is less than half the current limit. Further, the design procedure is rather complicated and iterative too. Therefore it is considered out of the scope of this section.

The required equation (Equation 2) (for Continuous Conduction Mode, 'CCM') is

$$L_{MIN\_CL\_CCM} = \frac{(V_O + V_D) \cdot (1 - D_{CCM}) \cdot 10^6}{2 \cdot f \cdot (I_{CLIM} - I_O)} \ \mu H \quad (2)$$

where the duty cycle is:

$$D_{CCM} = \frac{V_O + V_D}{V_{IN} - V_{SW} + V_D} \quad (3)$$

V_{SW} and V_D are the forward drops across the switch and the diode respectively. A sample calculation follows.

Example: The input voltage range is 8.5-16V. The output is 5V @ 1.5A. It can be assumed that both the switch forward drop and diode drop are 0.5V, by default.

Step 1: Current Limit at maximum input

The duty cycle at 16V input is

$$D_{CCM} = \frac{5 + 0.5}{16 - 0.5 + 0.5} \quad (4)$$

$D_{CCM} = 0.344$

I_{CL} = 2A (min value), so the required minimum inductance is

$$L_{MIN\_CL\_CCM} = \frac{(5 + 0.5) \cdot (1 - 0.344) \cdot 10^6}{2 \cdot 500000 \cdot (2 - 1.5)} \ \mu H \quad (5)$$

$L_{MIN\_CL\_CCM} = 7.2\mu H$ (6)

Step 2: Current Limit at maximum input

The calculation is repeated at the lowest desired input voltage of 8.5V. The duty cycle at this point is

$$D_{CCM} = \frac{5 + 0.5}{8.5 - 0.5 + 0.5} = 0.65 \quad (7)$$

The current limit at this duty cycle is

$$I_{CLIM} = I_{CL} - \{(m_C \bullet T) \bullet (D - 0.5)\}\ A \quad (8)$$

$$I_{CLIM} = 2 - \{(0.42 \bullet 2) \bullet (0.65 - 0.5)\}\ A \quad (9)$$

$$I_{CLIM} = 1.87A \quad (10)$$

So the minimum inductance at this point is

$$L_{MIN\_CL\_CCM} = \frac{(5 + 0.5) \cdot (1 - 0.65) \cdot 10^6}{2 \cdot 500000 \cdot (1.87 - 1.5)}\ \mu H \quad (11)$$

$$L_{MIN\_CL\_CCM} = 5.2\mu H \quad (12)$$

There is one more possible influence on the value of minimum inductance, which is now discussed.

Step 3: Subharmonic Instability

The LM1572 is current mode controlled. If the minimum input voltage is less than roughly twice the output voltage, the duty cycle is close to or greater than 0.5. That makes two of the three conditions required for subharmonic instability. Therefore also assuming continuous conduction mode, the value of inductance must be large enough to prevent these oscillations (occurring at f/2). The relevant equation (Equation 13) is

$$L_{MIN\_f/2} = (V_{IN} - V_{SW} + V_D) \cdot \frac{\frac{1}{\pi \cdot Q} + D_{CCM} - 0.5}{m_c}\ \mu H \quad (13)$$

On the left is the minimum inductance required. The right side contains 'Q, which is the quality factor of the half frequency peaking prior to the outbreak of subharmonic oscillations. Q should typically not be greater than 2, or subharmonic oscillations become increasingly likely. Further, to avoid voltage mode control type of response (excessive slope compensation), neither must Q be less than about 0.2. Very large values of L lead to smaller and smaller Q. So acceptable values of Q usually lie within the range 0.2 to 2. This calculation should always be done at the worst case: i.e. the minimum input voltage.

$$D_{CCM} = \frac{5 + 0.5}{8.5 - 0.5 + 0.5} = 0.65 \quad (14)$$

$$L_{MIN\_f/2} = (8.5 - 0.5 + 0.5) \cdot \frac{\frac{1}{\pi \cdot 2} + 0.65 - 0.5}{0.4}\ \mu H \quad (15)$$

$$LMIN\_f/2 = 6.2\mu H \quad (16)$$

But what is the optimum value? This is examined next.

Step 4: Optimum Inductance

The designer should be clear that choosing smaller inductance values may not necessarily lead to smaller sized inductors. The relationship between inductance and inductor size is not always intuitive. The size of an inductor is determined by its energy handling requirement which is $\frac{1}{2} * L * I_P^2$. So very small inductors may lead to excessively high peak currents, which can also increase the size of the input and output capacitors. The reader is referred to AN-1197 (SNVA038) for further details. There it is shown that 'r' , the current ripple ratio, should be around 0.4. Using this as the yardstick, the 'optimum' value of inductance is

$$L_{OPT} = \frac{V_O + V_D}{I_O \cdot r \cdot f} \cdot (1 - D_{CCM}) \cdot 10^6\ \mu H \quad (17)$$

This calculation must always be done at the maximum input voltage, which is 16V for this example

$$L_{OPT} = \frac{5 + 0.5}{1.5 \cdot 0.4 \cdot 500000} \cdot (1 - 0.344) \cdot 10^6\ \mu H \quad (18)$$

$$L_{OPT} = 12\mu H \quad (19)$$

Step 5: Conclusions

Several 'minimum inductances' were calculated: 7.2, 5.2 and 6.2µHs. The optimum value is 12µH. A standard value higher than all the 'minimums can be picked. Here, a standard 8.2µH/1.5A was chosen so as to provide the smallest sized inductor for the application. 10µH is a more widely available standard value, and very close to the optimum value too, and would therefore be a good choice too. Note that inductances larger than 15µH are not recommended in general.

To more accurately predict how the selected off-the-shelf part will actually perform in the real application, the designer is referred to AN-1197 (SNVA038). The procedure contained therein could greatly help in correctly choosing the lowest acceptable current/energy rating of the inductor, and thereby reducing its size further.

Input Capacitor Selection

At the input, the first requirement is a high frequency (preferably ceramic) decoupling capacitor, of value 0.1µF, placed very close to, and between the V_{IN} pins and the Ground Pins of the IC. This provides the triangular pulsed current waveform that flows through the switch. In addition, a bulk capacitor is also required, which replenishes the decoupling capacitor, and may be placed slightly further away if necessary. The rating and selection of this capacitor is discussed below.

In general a standard low-esr aluminum electrolytic is recommended at the input ('esr' refers to the equivalent series resistance hereafter). There are several reasons for this. Firstly, tantalum capacitors have inherent input surge-current limitations. So when the input surge current comes from a very low impedance source (such as a high current lab DC power supply), there is a chance that the capacitor may not survive several such repeated high dV/dt events. In any case, even using 'surge-tested' tantalums (like TPS series from AVX) a 50% voltage derating is recommended in such conditions. Therefore hypothetically, a 35V tantalum must be used for the preceding example, in which the maximum input was 16V. The second reason for avoiding very low esr input capacitors is that there is a possibility of severe input oscillations. The elements involved in this resonance are the inductance of the input leads, the input capacitance and the (negative) input impedance of the switching stage. It is known that the esr of the input capacitor actually serves a useful purpose in damping out these oscillations.

These oscillations can only be seen clearly under lab conditions if the output of the lab DC power supply is ON/Output-Enabled and then the lead from the converter stage is physically connected to the output terminals of the DC power supply. Just turning the DC power supply ON/OFF (or with an Output-Enable button) does not generate the high dV/dt required to provoke these oscillations. Under a real situation, input oscillations can become severe enough to cause the maximum voltage rating of the IC to be exceeded. The ringing can in turn, also feed in to the Analog sections of the LM1572, causing strange behavior and possibly device failure.

The designer needs to therefore monitor the input ramp close to the input of the converter, preferably with a digitizing oscilloscope set to about 10-20µs/div and using the single acquisition mode. Once the ramp is being captured, it will be seen that large input capacitances 'slow' the dV/dt considerably, thereby reducing the overshoot and the input oscillations. However, besides the capacitance itself, the esr of the input capacitor is a major contributor too. Therefore, in a typical comparison of a 10µF aluminum electrolytic vs. a 10µF tantalum electrolytic (tantalum has lower esr), it was seen that there was an almost 50% overshoot in the peak input voltage for the tantalum capacitor (accompanied by severe ringing), whereas for the aluminum capacitor, the overshoot was only about 10% (plus the waveform was that of a well damped system). The designer should also be aware that some older DC power supplies actually exacerbate the problem, while apparently trying to 'correct' the output voltage. The situation gets even worse if the DC power supply has a remote-sense which is being used to apparently 'correct' the input voltage at the input of the converter. Therefore, it is always a good idea to try out another available DC power supply to see how severe the problem is in reality, or whether it is just a 'bad' lab supply.

If because of size constraints the designer must use tantalums, a minimum capacitance of 22µF is recommended for any application, irrespective of input/output conditions. This 'softens' up the input dV/dt significantly and reduces the ringing.

The basic electrical criterion for selecting an input capacitor is the input RMS current. The equation (Equation 20) for this is

$$I_{IN} = I_O \cdot \sqrt{D \cdot \left[1 - D + \frac{r^2}{12}\right]} \text{ A} \quad (20)$$

where

- 'r' is the current ripple ratio.

It is given by:

$$r = \frac{V_O + V_D}{I_O \cdot L \cdot f} \cdot (1 - D) \cdot 10^6 \quad (21)$$

where L is in µH and f in Hz. This calculation should be done at the worst case condition for this parameter, which corresponds to 50% duty cycle. If the application never 'sees' 50% duty cycle over its entire operating range, then the worst case is simply the closest duty cycle to 50%. This can, in general, occur at either of the input voltage extremes, and therefore both ends must then be examined. In the example, it was seen that the duty cycle varies from 34.4% to 65%. So it is clear that there does exist an input voltage point within the range, at which the duty cycle is 50%. At this worst-case condition, for the chosen inductor, 'r' at D=0.5 is

$$r = \frac{5 + 0.5}{1.5 \cdot 8.2 \cdot 500000} \cdot (1 - 0.5) \cdot 10^6 \quad (22)$$

$$r = 0.45 \quad (23)$$

At this point the input RMS current in the capacitor is

$$I_{IN} = 1.5 \cdot \sqrt{0.5 \cdot \left[1 - 0.5 + \frac{0.37^2}{12}\right]} \, A \quad (24)$$

$$I_{IN} = 0.76A \quad (25)$$

Therefore, this is also the minimum required RMS current rating of any input capacitor to be used. Now, a typical 25V aluminum capacitor would need to be around 470-1000µF just to be able to handle this current. It would also take up valuable space on the board. Therefore for the example, the choice is tantalum 22µF/35V TPS series AVX capacitor, Part Number TPSE226K035S0200, rated for 0.812A at 85°C. Though it is also possible to use a Panasonic surface mount aluminum 470µF/25V FK series, Part Number EEVFK1E471P, rated for 0.85A at 105°C.

Output Capacitor Selection

In voltage mode control, the esr of the output capacitor plays an important role in the feedback loop. Therefore in such cases, it is usually cautioned against reducing the esr too much. But keeping the esr high enough to ensure loop stability has several 'side-effects': it prevents the use of ceramic capacitors at the output, it also keeps the dissipation in the output capacitor 'high' (since this is I_P^2*esr), and it also keeps the output voltage ripple 'high' (which too is proportional to esr). Note that a post LC filter therefore becomes necessary with voltage mode controllers, if really low output voltage ripple is required.

With current mode control, the feedback loop is different, and so the output esr can be reduced significantly. Therefore the main criterion for selection of the output capacitor is based on the acceptable output voltage ripple. In the example, assuming that ±75mV of ripple is acceptable (i.e. 150mV peak to peak), the peak to peak current is

$$I_{PP} = I_O \bullet r \quad (26)$$

The worst case condition for this parameter is at minimum duty cycle (max input). At this point, with the chosen inductor

$$r = \frac{V_O + V_D}{I_O \cdot L \cdot f} \cdot (1 - D) \cdot 10^6 \quad (27)$$

$$r = \frac{5 + 0.5}{1.5 \cdot 8.2 \cdot 500000} \cdot (1 - 0.344) \cdot 10^6 \quad (28)$$

$$r = 0.59 \quad (29)$$

So peak to peak current is

$$I_{PP} = 1.5 \bullet 0.59 = 0.88A \quad (30)$$

For a maximum 150mV ripple the esr must be less than

$$esr = 0.150/0.88 = 0.17\Omega \quad (31)$$

The RMS current capability should also be checked. The RMS output current is

$$I_{OUT} = I_O \cdot \frac{r}{\sqrt{12}} \quad (32)$$

The worst case condition for this parameter is at highest input voltage. So

$$I_{OUT} = 1.5 \cdot \frac{0.59}{\sqrt{12}} = 0.25\,A \quad (33)$$

Therefore a close fit is tantalum 100µF/10V TPS series AVX capacitor, Part Number TPSY010K010S0150, esr of 0.15Ω, rated for RMS current 0.822A at 85°C. An alternative is Panasonic surface mount aluminum 330µF/10V FK series, Part Number EEVFK1A331P, esr of 0.16Ω, rated for RMS 0.6A at 105°C. Note that the esr (and allowed output voltage ripple) played the dominant rule in the selection here. If very low output ripple is demanded, it would point in the direction of larger and larger capacitances. However, it must be kept in mind that a very large output capacitance can lead to startup problems, because of the huge charging current (and its duration). The choice of tantalum at the output will permit a much lower capacitance to be used, which leads to a smaller energy inrush ($\frac{1}{2}*C*V^2$) and no startup problems. Therefore when using 'low cost' aluminum capacitors at the output, (which always end up having a larger capacitance than tantalums for the same esr), softstart is recommended so as to prevent startup problems.In addition, very low esr (irrespective of whether capacitor is aluminimum, tantalum etc.), can lead to loop instability and therefore a Bode plot is recommended to ensure adequate phase margin.

Sequencing

This section may be skipped if the SD pin is floating, or tied high. It is of concern only if the Designer intends to use the Shutdown pin in an active manner.

The following scenario explains the situation: if the input voltage is applied and the converter has been running for some time (SD pin high), the bootstrap capacitor is (as is normal) charged up to about 5V. Now if the input is disconnected, and then reconnected immediately, while holding the SD pin low, the following can happen: the output which is expected to be zero, may go 'high' (no regulation). It returns to regulation only when the SD pin is taken high (over 2.38V). This mode occurs only under the above set of conditions, and only if the applied input ramp has an extremely high slope. Then the dV/dt of the ramp injects stray charge through the Drain-Gate capacitance of the internal Fet drivers, causing the gate voltage to go high, and may eventually cause the switching Fet to turn on spuriously. The switch will then stay in full conduction, till the next level shift command comes from the SD pin. Several options exist so as to avoid this:

1. The SD pin must not be held low during the instant that the reapplied input voltage is ramping up across the input of the converter.
2. Or the input dV/dt must be kept low. One way is to increase the input capacitance (and/or esr), as mentioned earlier. Therefore, it is recommended that if the SD pin is expected to be used actively (not floating or high), the input capacitor should always be an aluminum electrolytic. This will automatically lead to a larger capacitance value and esr, as desired. Further, the oscillations and overshoot at the input, described earlier, which are also contributory factors to this spurious turn-on, will also be suppressed.
3. Or the Bootstrap capacitor must be discharged. Now, since the voltage across the bootstrap capacitor happens to be the supply for the internal driver, if this capacitor is discharged before the input is reapplied, there will be no problem: no supply, no drive! To implement this, it is recommended that the bootstrap capacitance used is reduced to 0.01µF and in addition, a 1M-4.7M resistor placed from the bootstrap pin to ground. This provides a discharge path for the bootstrap capacitor. The RC time constant is about 10-50ms, and so a 'wait period' of like amount is recommended before input power is reapplied. This will allow sufficient time for the bootstrap capacitor to discharge, and the spurious turn-on will be prevented.

Overload Protection

The LM1572 incorporates a useful protection feature called 'frequency foldback'. When the voltage on the feedback node starts falling to zero below a certain threshold, the IC commands a progressive reduction in switching frequency from 500kHz to 100kHz. The reader is referred to the relevant curve in Typical Performance Characteristics of this datasheet. The pulse width also decreases to the minimum width of 300ns (typical). These actions help protect not only the IC, but also the external power components and the load. It can be shown that this protection feature is vital to avoiding overstress during overload and even under normal startup/powerup.

Consider what happens if the output of a buck converter is at zero volts with the maximum input voltage applied at the input. This 'zero output volts' condition represents the natural initial condition at normal powerup/startup but could also be a forced condition in the form of an output short. Then for the LM1572, almost the full input of 16V can find iself across the inductor during the on time of the switch. During the off time, the voltage across the inductor reverses but the magnitude of this voltage is only 0.5V (which comes from the 'typical' Schottky forward drop).This leads to the problem: depite having a 'current limit', in fact there is absolutely no effective current limit in this condition. Because if the switch turns on, it has a minimum pulse width of about 300ns before it can actually respond to any information about having exceeded the current limit. This minimum pulse width is unavoidable due to various internal delays, propagation intervals, and also the internal blanking time carefully set

for rejection of transition noise, as required with current mode control. Therefore using V=L*dI/dt is can be shown that for a switching frequency of 500kHz, and say with an inductance of 8.2µH, the current ramps up by about 0.58A during the minimum switch on time of 0.3µs. During the off time of 1.7µs, it ramps down, but only by about 0.1A. Therefore the current peak will incrementally increase or staircase upwards by a net 0.48A every cycle. And in a few cycles this could blow the switch. Increasing the inductance will not help, as it will only affect the rate of the current staircasing, not necessarily its peak. In the absence of any other effective measure, the only way out in the current situation is to 'hope and pray' that the the output voltage rises fast enough before damage occurs. For a normal power up, the output rail would rise eventually, at a rate which would be dependent on the value of the output capacitance. However for a short on the output, it would never rise. In either case we have a potentially destructive situation. Now it can also be shown that if the frequency was immediately reduced to 100kHz following the 'zero output volts' condition, the off time is increased to 10-0.3=9.7µs. This will cause the calculated current ramp-down to be 0.59A instead of 0.1A. Since this is greater than the current ramp-up of 0.58A the current will actually return to zero every cycle, and there will be no staircasing. This is how the LM1572 frequency foldback protection works, thus avoiding this potentially dangerous condition altogether. We consider the two possible situations for 'zero output volts condition' in more detail below, to understand it better.

By definition, an 'overload' is where the switch current limit has been reached, and then any attempt to increase the load further, causes the output voltage rail to 'droop', though the load current remains virtually constant during this time. If an attempt is made to increase the load even further, the voltage on the feedback pin will fall low enough to cause the LM1572 to start lowering its switching frequency. At the same time the output of the error amplifier clamps high (at 2V), and this causes the LM1572 to suddenly reduce the on-time to the minimum pulse width. The foldback frequency is now 100 kHz, and with this minimum pulse width, the effective duty cycle is 3%. It can be easily shown by calculation that at the highest input voltage (worst case), assuming a typical Schottky catch diode drop, a 3% duty cycle produces a very low (almost zero) output voltage (ignoring switch voltage drop here). However if the frequency had remained at 500 kHz, the duty cycle would have been 15%, and this would have led to a calculated output voltage of (16*0.15)-0.5=2V, though we are forcing the output to zero. This therefore represents a 'struggle', which manifests itself as an overstress condition. In this condition parasitics like inductor winding resistance etc. will be called upon to control the situation, and to stabilize the situation. For the lower frequency case, with a duty cycle of 3%, since the calculated output voltage is commensurate with the external condition of a short-circuit on the output, the converter does not 'struggle' to maintain this condition. However even with the foldback protection as it is present on the LM1572, the Designer is cautioned that the actual load current which can flow with a short-circuit on the output, depends on various factors. For example, high current Schottky diodes will be found to lead to higher short-circuit currents than modestly rated diodes. This is because it can be shown that if the diode drop is lower than 'typical' (as is the case for for high current diodes), it requires a duty cycle even lower than 3% to keep the calculated output voltage really close to 'zero'. Therefore it may not be a good idea for example, to use say a 5A/30V Schottky diode for a 1.5A application. The selected diode in the typical application circuit is correctly sized to be a 2A/30V Schottky from IRF.

Under startup, the frequency foldback effectively limits the inrush current spike. The soft start feature, acting on its own, cannot suppress the current spike at all. The role of softstart is to gradually raise the duty cycle and thereby to bring up the output rail slowly. But the inrush spike, which is mainly the initial charging current of the output capacitors, occurs at the moment of application of input power, even before the voltage across the output capacitors has really started to rise significantly. At this instant, soft start would call out for minimum on time, but as seen above, this is just not enough to limit the current. However, with foldback of frequency to 100kHz, the startup duty cycle falls from 15% to 3%. This leaves enough off time for the current to subside every cycle, as explained above, and there is no cumulative current buildup, or 'staircasing'.

Layout Guidelines

Refer to the sample PCB layout provided. The Bill of Material is also provided. The board is based on the schematic in Typical Applications (Fixed/Adjustable Voltage Parts) for the fixed voltage part. The design is based on the worked example presented in this datasheet. The input voltage can vary between 8.5V to 16V. The output rail is 5V and the peak current is 1.5A. The inductor is however sized to handle only 1A continuous current. If higher continuous rating is required (this depends on ambient temperature range too), an appropriately rated inductor, possibly a higher series from the same vendor (keeping inductance unchanged) can be selected.

Considering the critical aspects of the layout, it is recommended that the routing and positioning of the 0.1µF input decoupling capacitor, C2, be kept the same as shown, and also the catch diode D1. The rest are not critical, and may be changed. Note however that the trace to the feedback pin is routed through the quiet ground plane on the bottom side. This helps prevent noise pickup and maintain correct output voltage. Note that vias are provided, for example directly below the IC to the ground plane, and this helps not only in transferring heat to the other side of the board, but references the IC ground directly to the ground plane.

Loop Compensation

Since the LM1572 uses current mode control, the loop response does not involve the inductor. The error amplifier can be modeled as a transconductance amplifier with a large output impedance of 200k of resistance in parallel with 12pF of output capacitance. In practical applications, the impedance of the external compensation network from the Comp pin to ground dominates completely, and the error amplifier characteristics do not contribute any significant phase shift to the loop. Therefore the error amplifier can for all practical purposes be considered simply as a 2000µMhos of transconductance, the loop phase/gain being determined externally.

The simplest recommended compensation is a 3.3nF capacitor from comp pin to ground. This provides a pole at 240Hz. The overall loop then has a low frequency gain of about 62dB at 1.5A, with a crossover at about 15kHz, and a phase margin of about 33°. A resistor may be added in series with this capacitor to improve the loop phase margin/crossover frequency. Recommended values for this are 1k to 1.5k. If the loop response needs to be further improved, by increasing the value of this resistor, then a small capacitor of about 470pF is required across the RC. Its purpose is to limit the ripple on the Comp pin to within 100mV_{PP}, which can otherwise cause problems with the behavior of the LM1572.

Loop compensation must be further validated by a bench measurement, using standard Bode plot/spectrum analyzer equipment. Step load transient response can also be tested and should not reveal excessive ringing on the output of the converter.

Tolerance of set Output Voltage

This section may be skipped altogether, unless the designer wants to get a more precise understanding of the possible variation or 'spread' on the output voltage and how this can be controlled better.

This 'basic resistive divider design equation' seems to suggest that R_2 is always a certain fixed 'ratio' to R_1, for a given output voltage. For example, referring to the Typical Application Circuit (Figure 1), where the values shown are R_2=806 and R_1= 2.21k, it may have been thought that using the following values: R_2=8.06k and R_1= 22.1k, would have been equally acceptable. But the simple equation is just that: an 'ideal' equation that unrealistically assumes zero current into or out of the feedback pin. It can be easily shown that the effect of any 'real' current, flowing into the feedback pin for example, is to raise the output voltage slightly from the 'ideal' calculation. This is considered to be an output voltage 'error', and this needs to be understood and quantified.

Now, as mentioned, had the selection been: R_2=8.06k and R_1= 22.1k, (possibly with the intention of reducing the dissipation in the resistive divider by a factor of 10), it would also have increased the error in the output voltage by almost the same factor. A compromise can always be considered if efficiency at light loads is a key concern, but first it must be understood how to actually design the resistive divider for a certain (maximum) error.

As can be seen from the Typical Performance Characteristics curves and tables of Electrical Characteristics for the LM1572,a current of about 0.5µA (typical value) flows into the feedback pin at regulation (I_{FB_REG}). Since V_{FB} = 2.42V, it may have been thought appropriate to 'modify' the basic resistive divider equation by simply modeling this current in by an 'internal resistor' between feedback pin and ground. Its value would be 2.42V/0.5µA = 4.84MΩ . In fact this would have been acceptable had the current been a constant. But as seen from the Electrical Characteristics, this current can be as high as 1.5µA. This would mean that this internal resistor can actually be 3 times lower i.e. 4.84/3 = 1.6MΩ. Therefore, it is not the feedback pin current itself, but its variability that poses the problem: a single fixed known value of feedback pin current can be easily modeled, not a spread of values.

The most direct approach to the problem is as follows: to continue to use the basic ('ideal') resistive divider equation as the basic design equation, but to also use the equation which 'models in' a 1.6MΩ resistor as representing the worst case error, then to compare these two equations to calculate what the error is. Conclusions on how to reduce this error would follow.

So proceeding in this manner, the worst-case resistive divider equation (Equation 34) (modified to include 1.6MΩ resistor in parallel with R_1) is

$$R_2 = \left[\frac{R_1 \cdot 1.6M}{R_1 + 1.6M}\right] \cdot \left[\frac{V_O}{2.42} - 1\right] \quad (34)$$

Comparing this with the basic equation provides the following error equation (Equation 35)

$$\frac{\Delta V_O}{V_O} = \left[1 - \frac{1.6M}{R_1 + 1.6M}\right] \cdot 100\% \quad (35)$$

Note that the right hand side depends on R_1 (not R_2, nor the output voltage directly). So for a given maximum allowed error, first R_1 is calculated. Then the basic resistive divider equation is invoked and used to calculate R_2.

The effect of R_1 is now considered.

If R_1 was say 5k, the error is about 0.3%. This error is in the '+' direction as mentioned earlier, for the case of current flowing into the pin. The error is reduced to 0.14% for the value R_1 = 2.21k as used in the Typical Application circuit. In general it can be concluded that to restrict the error to within 0.25%, R_1should be 4k (or less).

If R_1 is 4.02k (a standard value), R_2 as calculated from the basic resistive divider design equation is 4.286k for a 5V output and is 1.462k for a 3.3V output.

There is an alternative way of stating the error, in terms of current rather than resistance. Since if R_1=4k, the current flowing through the resistive divider is 2.42/4k=0.6mA, therefore it can also be stated that the divider current should be 0.6mA or less. This will restrict the error (due to the feedback pin current and its variation) to less than 0.25%. This 'thumbrule' does not depend on input or output conditions, and is typical for most applications.

The other related problem is that to get an exact value for R_1 or R_2 from standard resistor values may not be easy. Any one of the two resistors can of course be selected to be a standard value, but the other value as calculated from the equation, will more likely than not, not correspond to any standard value. The so called 'EIA standard values' are the E6, E12, E24, E48, E96 and E192 series, listed in most resistor catalogs. E12 for example has 12 values in every decade of resistance. The reader can for example do a search within a typical vendor's index home page e.g. http://www.vishay.com/ with the keyword **E96** for the table of standard values.

The available tolerances should also be checked out as they govern what can be considered a 'standard' value for a certain requirement. Therefore for example, if 1% resistors are required, it will be almost impossible to find such a resistor in the E12 or E24 series, for which 10% and 5% respectively are more commonly available tolerances. E48 is normally 2%, E96 is 1%, and E192 is 0.5%/ 0.1%. Further, each series is usually 'devoted' to its tolerance.Therefore a value like 221Ω which exists in E96 and E192 may not be readily available as a 2% resistor, simply because in E48 (which is usually for 2% resistors), the nearest standard values are 215Ω and 226Ω. One could always pay more for better resistors than required, but the question is one of 'optimum' design here. 'Optimum' means a correct consideration/compromise between several factors: cost, tolerance of the resistors, and the output error (from all related sources). All these indicate that the task of correctly selecting a resistive divider is usually under-estimated or down-played.

Looking at the standard value series, it should also be noted that every series is a subset of the next higher series. However there are two distinct sets. Therefore E6 is a subset of E12 and E24, and E48 is a subset of E96 and E192. However no E24 value can be found in E48 (or higher). As an example, the 'well-known' resistance value of 220Ω is available in E6, E12 and E24. But this value does not exist in the higher (more modern) series.There the closest 'standard' values are 215Ω and 226Ω in E48, and also 221Ω in the more expensive series as discussed above. The following example will make these considerations clearer.

Example: It is required to set an output voltage of 5V using the adjustable part. R_1 is taken to be a 4.02k (E48 series) standard resistor value (for a 0.25% error expected on account of the feedback pin current). So using the basic divider equation (Equation 36)

$$R_2 = 4.02 \cdot \left[\frac{5}{2.42} - 1\right] = 4.286\ k\Omega \quad (36)$$

This is, as expected, not a standard resistance value. The closest is 4.32k (E96). Using that value for R_2 would give an additional error of (4.32−4.286)/4.286 = 0.8% (on top of the errors due to other causes). If this is unacceptable, an additional resistor can be placed in parallel with the 4.32k. Checking to see if a 'standard' 560k resistor would do the job: this gives an effective value of (4.32*560)/(4.32 + 560) = 4.287k, which is almost exactly the required value of 4.286k! More on the choice of the 560k will follow below.

Final recommended values here are

R_1 = 4.02k, and R_2 = 4.32k ‖ 560k (37)

Note that the effect of other tolerances have not been considered, including the possible spread on V_{FB} itself (this adds another +,- 1.25% of error as indicated by the Electrical Characteristics tables). Another significant source of error to consider is the tolerance of the resistors themselves. For a majority of applications these are generally chosen to be of 1% tolerance. But they can be chosen to be 0.5% or 0.1% in critical applications, or even 2% in less sensitive applications.

The percentage error in the output voltage is $2*(V_O-V_{FB})*Tol/V_O$. So for example with 1% resistors being used to set the output to 5V, the maximum error on the output on account of the resistor tolerance is 2*(5-2.42)*1/5=1%. (This is actually +,-1% since the tolerance of the resistors to start with was also +,-1%). For a 3.3V output, the error is about +,-0.5% with 1% resistors. Similarly, the output error (on this account) is reduced by a factor of 10, if 0.1% resistors are used instead.

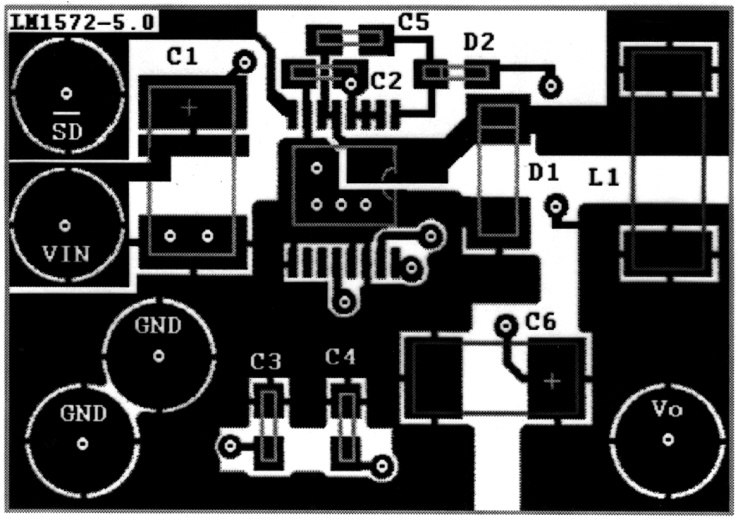
As for the shunt resistor of 560k (in parallel to R_2), it is not really necessary to have a very tight tolerance for this resistor. Since the entire effect of this resistor is to add a slight 'trim' to the output voltage, the effect of its tolerance on the output is proportionally small too. The proportionality factor here is the ratio R_2/560k. Therefore, the 560k can be a 5% resistor in almost all applications. This was actually kept in mind well in advance, when the value 560k was initially proposed. Because 560k happens to be a standard value in the 5% series (E24), though it does not exist in the higher (expensive) series. Cost was clearly of concern here.

Concluding this discussion, there is a last observation to make concerning the fixed voltage part. Here the output is normally connected to the feedback pin directly. The resistive divider is therefore internal. The relevant design information here is that for the 5V part the effective resistance (R_1 + R_2) from feedback pin to ground is 10k. For the 3.3V part this resistance is 6.6k. This gives a current of 0.5mA passing through the divider. This is a satisfactory choice, since it was seen to limit the contribution of the feedback node current on the output to less than 0.3%. The error due to the 'tolerance' of the resistive divider is almost negligible for fixed voltage parts. To understand this, the reason for the error from an external divider, as used in an adjustable part, must first be clarified. There the worst case situation is where one resistor is at the lower end of its tolerance band, while at the same time the other resistor is at the upper end of the tolerance band. This gives the worst case error on the output. However if both the upper and lower resistors were simultaneously say 'x%' higher (or lower) than their nominal, their 'ratio' would remain unchanged. It was earlier indicated that if the ratio of the resistances in a resistive divider is maintained, then theoretically there is no change in the output voltage. This is the situation in the case of the internal resistive divider. Because the two resistors are in the same package, any drift or tolerance will affect both of them almost equally. It is expected, and borne out, that their 'relative tolerance' is typically almost 10 times better than the (absolute) tolerance of each. Therefore, the effect of the tolerance of the resistors in an internal resistive divider, as in fixed voltage parts, can be ignored.

Bill of Material for LM1572 Evaluation Board

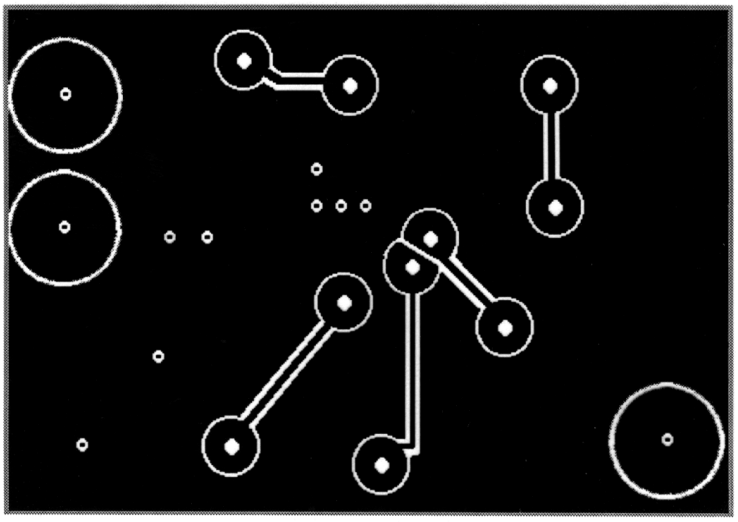
Designator	Description	Manufacturer	Part Number	Qty.
U1	LM1572-5.0	Texas Instruments	LM1572-5.0	1
D1	2A/30V Schottky	International Rectifier	20BQ030	1
D2	SS diode	General Semiconductor	1N4448W	1
L1	8.2µH	Gowanda	SMP3013-821K*	1
C1	22µF/35V	Vishay-Sprague	595D226X0035R2T	1
C2, C3, C5**	0.1µF/50V	Vishay-Vitramon	VJ0805Y104KXAAR	3
C4	3.3nF/50V	Vishay-Vitramon	VJ0805Y332KXAAR	1
C6	100µF/10V	Vishay-Sprague	594D107X0010C2T	1

PCB Layout



(Refer to schematic in 'Typical Application' for fixed voltage part)

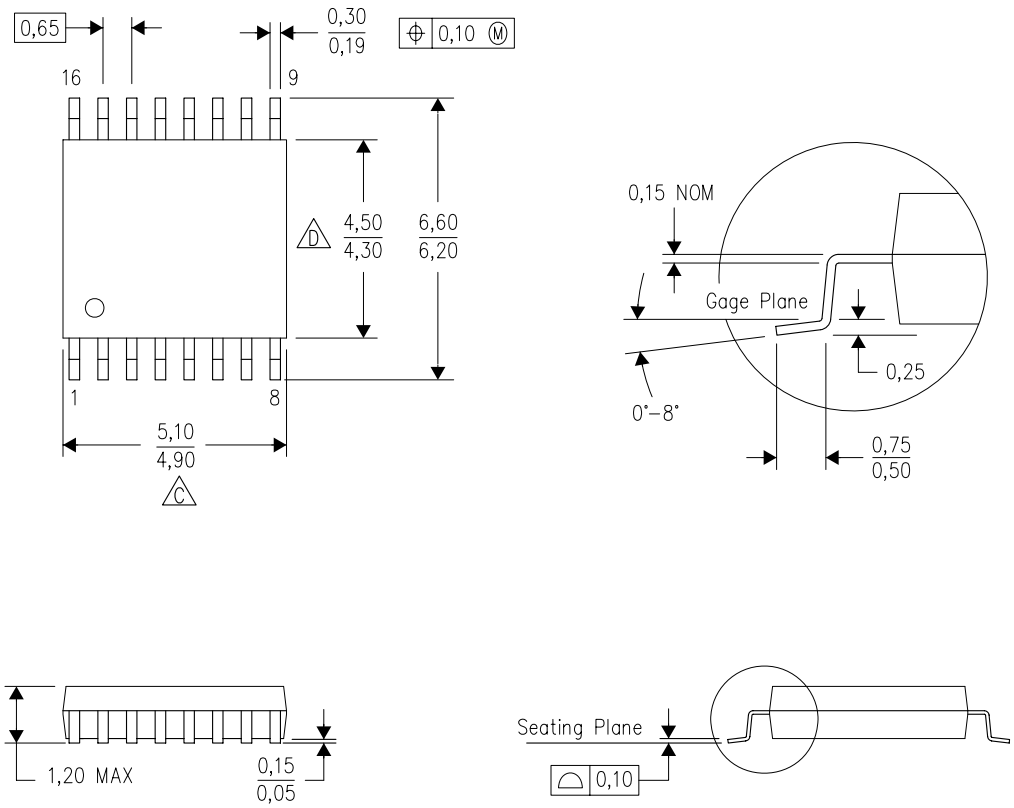
Figure 14. Top Layer



(Refer to schematic in 'Typical Application' for fixed voltage part)

Figure 15. Bottom Layer

PW (R–PDSO–G16) PLASTIC SMALL OUTLINE



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NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

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