National Semiconductor Corporation

LM1851 Ground Fault Interrupter

General Description

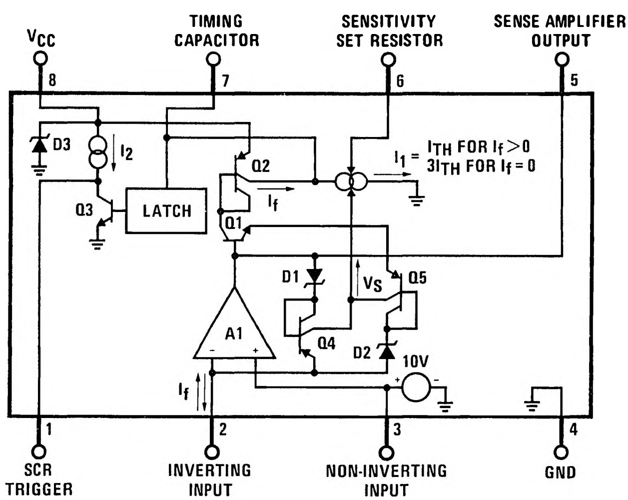
The LM1851 is designed to provide ground fault protection for AC power outlets in consumer and industrial environments. Ground fault currents greater than a presettable threshold value will trigger an external SCR-driven circuit breaker to interrupt the AC line and remove the fault condition. In addition to detection of conventional hot wire to ground faults, the neutral fault condition is also detected.

Full advantage of the U.S. UL943 timing specification is taken to insure maximum immunity to false triggering due to line noise. Special features include circuitry that rapidly resets the timing capacitor in the event that noise pulses introduce unwanted charging currents and a memory circuit that allows firing of even a sluggish breaker on either half-cycle of the line voltage when external full-wave rectification is used.

Features

- Internal power supply shunt regulator
- Externally programmable fault current threshold
- Externally programmable fault current integration time
- Direct interface to SCR
- Operates under line reversal; both load vs line and hot vs neutral
- Detects neutral line faults

Block and Connection Diagram



TOP VIEW

TL/H/5177-1

Order Number LM1851M or LM1851N
See NS Package Number M08A or N08E

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Current	19 mA
Power Dissipation (Note 1)	1250 mW
Operating Temperature Range	−40°C to +70°C
Storage Temperature Range	−55°C to +150°C

Soldering Information	
Dual-In-Line Package (10 sec.)	260°C
Small Outline Package	
Vapor Phase (60 sec.)	215°C
Infrared (15 sec.)	220°C

See AN-450 "Surface Mounting and Their Effects on Product Reliability" for other methods of soldering surface mount devices.

DC Electrical Characteristics $T_A = 25°C, I_{SS} = 5$ mA

Parameter	Conditions	Min	Typ	Max	Units
Power Supply Shunt Regulator Voltage	Pin 8, Average Value	22	26	30	V
Latch Trigger Voltage	Pin 7	15	17.5	20	V
Sensitivity Set Voltage	Pin 8 to Pin 6	6	7	8.2	V
Output Drive Current	Pin 1, With Fault	0.5	1	2.4	mA
Output Saturation Voltage	Pin 1, Without Fault		100	240	mV
Output Saturation Resistance	Pin 1, Without Fault		100		Ω
Output External Current Sinking Capability	Pin 1, Without Fault, $V_{pin\ 1}$ Held to 0.3V (Note 4)	2.0	5		mA
Noise Integration Sink Current Ratio	Pin 7, Ratio of Discharge Currents Between No Fault and Fault Conditions	2.0	2.8	3.6	μA/μA

AC Electrical Characteristics $T_A = 25°C, I_{SS} = 5$ mA

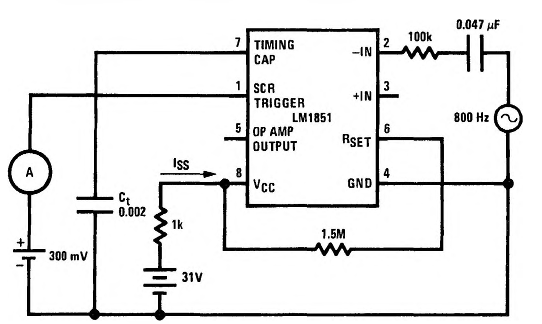
Parameter	Conditions	Min	Typ	Max	Units
Normal Fault Current Sensitivity	*Figure 1* (Note 3)	3	5	7	mA
Normal Fault Trip Time	500Ω Fault, *Figure 2* (Note 2)		18		ms
Normal Fault with Grounded Neutral Fault Trip Time	500Ω Normal Fault, 2Ω Neutral, *Figure 2* (Note 2)		18		ms

Note 1: For operation in ambient temperatures above 25°C, the device must be derated based on a 125°C maximum junction temperature and a thermal resistance of 80°C/W junction to ambient for the DIP and 162°C/W for the SO Package.

Note 2: Average of 10 trials.

Note 3: Required UL sensitivity tolerance is such that external trimming of LM1851 sensitivity will be necessary.

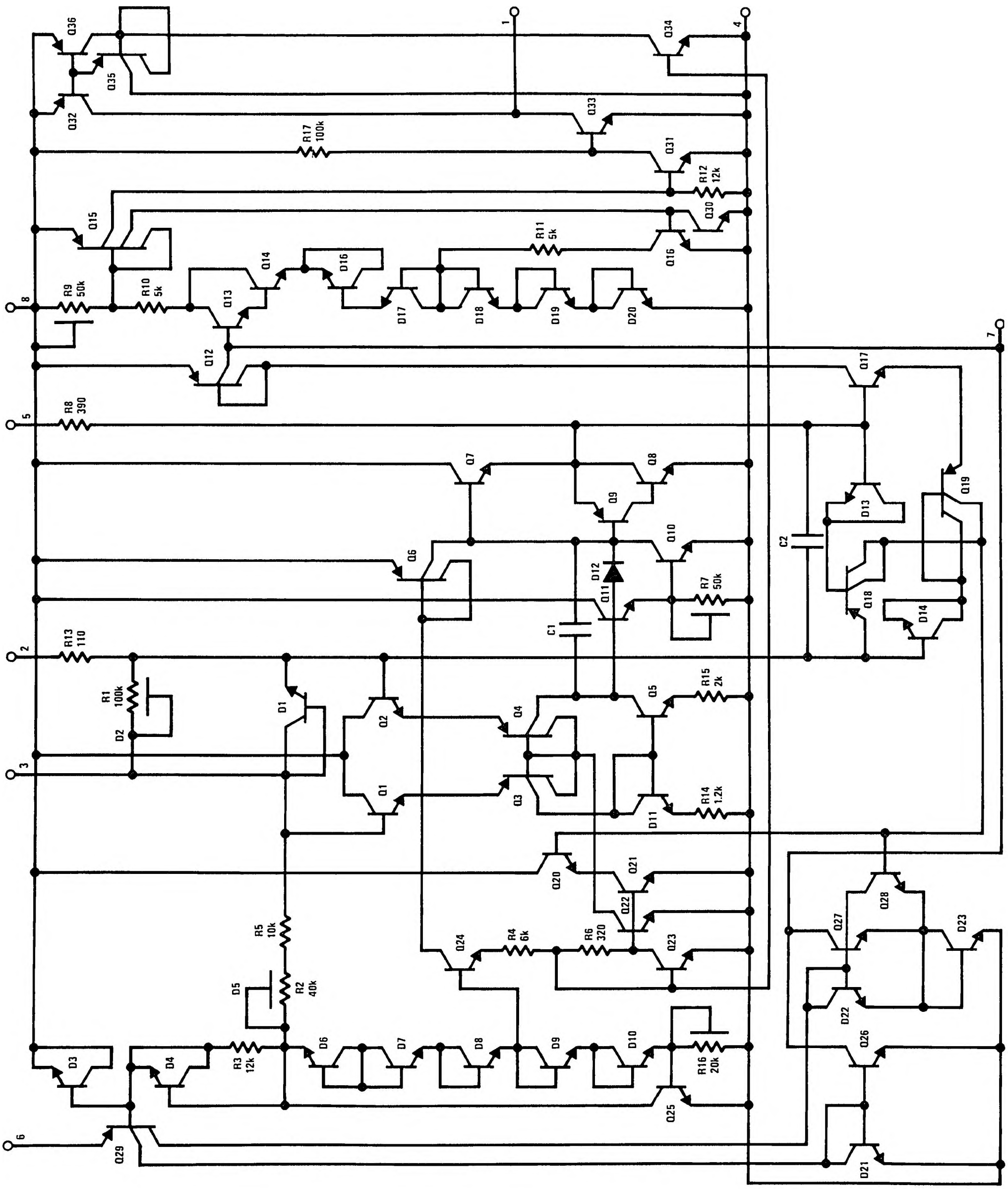
Note 4: This externally applied current is in addition to the internal "output drive current" source.



TL/H/5177-2

FIGURE 1. Normal Fault Sensitivity Test Circuit

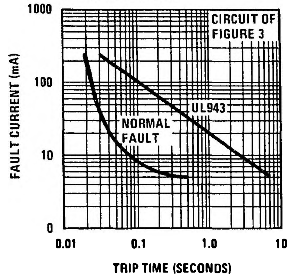
Internal Schematic Diagram



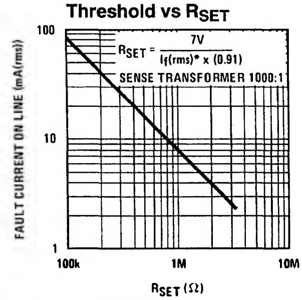
TL/H/5177–3

Typical Performance Characteristics

Average Trip Time vs Fault Current

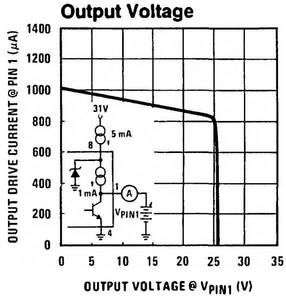


Normal Fault Current Threshold vs R_{SET}

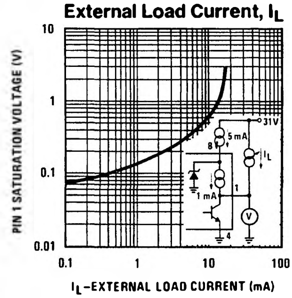


* See Block Diagram

Output Drive Current vs Output Voltage



Pin 1 Saturation Voltage vs External Load Current, I_L



TL/H/5177-4

Circuit Description

(Refer to Block and Connection Diagram)

The LM1851 operates from 26V as set by an internal shunt regulator, D3. In the absence of a fault ($I_f = 0$) the feedback path status signal (V_S) is correspondingly zero. Under these conditions the capacitor discharge current, I_1, sits quiescently at three times its threshold value, I_{TH}, so that noise induced charge on the timing capacitor will be rapidly removed. When a fault current, I_f, is induced in the secondary of the external sense transformer, the operational amplifier, A1, uses feedback to force a virtual ground at the input as it extracts I_f. The presence of I_f during either half-cycle will cause V_S to go high, which in turn changes I_1 from $3I_{TH}$ to I_{TH}. Although I_{TH} discharges the timing capacitor during both half-cycles of the line, I_f only charges the capacitor during the half-cycle in which I_f exits pin 2. Thus during one half-cycle $I_f - I_{TH}$ charges the timing capacitor, while during the other half-cycle I_{TH} discharges it. When the capacitor voltage reaches 17.5V, the latch engages and turns off Q3 permitting I_2 to drive the gate of an SCR.

Application Circuits

A typical ground fault interrupter circuit is shown in *Figure 2*. It is designed to operate on 120 V_{AC} line voltage with 5 mA normal fault sensitivity.

A full-wave rectifier bridge and a 15k/2W resistor are used to supply the DC power required by the IC. A 1 μF capacitor at pin 8 used to filter the ripple of the supply voltage and is also connected across the SCR to allow firing of the SCR on either half-cycle. When a fault causes the SCR to trigger, the circuit breaker is energized and line voltage is removed from the load. At this time no fault current flows and the IC discharge current increases from I_{TH} to $3I_{TH}$ (see Circuit Description and Block Diagram). This quickly resets both the timing capacitor and the output latch. At this time the circuit breaker can be reset and the line voltage again supplied to the load, assuming the fault has been removed. A 1000:1 sense transformer is used to detect the normal fault. The fault current, which is basically the difference current between the hot and neutral lines, is stepped down by 1000 and fed into the input pins of the operational amplifier through a 10 μF capacitor. The 0.0033 μF capacitor between pin 2 and pin 3 and the 200 pF between pins 3 and 4 are added to obtain better noise immunity. The normal fault sensitivity is determined by the timing capacitor discharging current, I_{TH}. I_{TH} can be calculated by:

$$I_{TH} = \frac{7V}{R_{SET}} \div 2 \qquad (1)$$

At the decision point, the average fault current just equals the threshold current, I_{TH}.

$$I_{TH} = \frac{I_{f(rms)}}{2} \times 0.91 \qquad (2)$$

where $I_{f(rms)}$ is the rms input fault current to the operational amp and the factor of 2 is due to the fact that I_f charges the timing capacitor only during one half-cycle, while I_{TH} discharges the capacitor continuously. The factor 0.91 converts the rms value to an average value. Combining equations (1) and (2) we have

$$R_{SET} = \frac{7V}{I_{f(rms)} \times 0.91} \qquad (3)$$

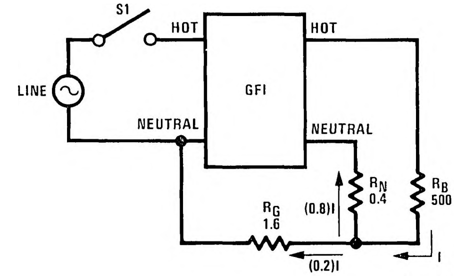
For example, to obtain 5 mA(rms) sensitivity for the circuit in *Figure 2* we have:

$$R_{SET} = \frac{7V}{\dfrac{5\text{ mA} \times 0.91}{1000}} = 1.5\text{M }\Omega \qquad (4)$$

The correct value for R_{SET} can also be determined from the characteristic curve that plots equation (3). Note that this is an approximate calculation; the exact value of R_{SET} depends on the specific sense transformer used and LM1851 tolerances. Inasmuch as UL943 specifies a sensitivity "window" of 4 mA–6 mA, provision should be made to adjust R_{SET} on a per-product basis.

Independent of setting sensitivity, the desired integration time can be obtained through proper selection of the timing capacitor, C_t. Due to the large number of variables involved, proper selection of C_t is best done empirically. The following design example, then should only be used as a guideline.

Assume the goal is to meet UL943 timing requirements. Also assume that worst case timing occurs during GF1 start-up (S1 closure) with both a heavy normal fault and a 2Ω grounded neutral fault present. This situation is shown diagramatically below.



TL/H/5177–5

UL943 specifies ≤25 ms average trip time under these conditions. Calculation of C_t based upon charging currents due to normal fault only is as follows:

≤25 ms Specification

−3 ms GFI turn-on time (15k and 1 μF)

−8 ms Potential loss of one half-cycle due to fault current sense of half-cycles only

−4 ms Time required to open a sluggish circuit breaker

≤10 ms Maximum integration time that could be allowed

8 ms Value of integration time that accommodates component tolerances and other variables

$$C_t = \frac{I \times T}{V} \qquad (5)$$

where T = integration time

V = threshold voltage

I = average fault current into C_t

$$I = \underbrace{\left(\frac{120\ V_{AC(rms)}}{R_B}\right)}_{\substack{\text{heavy fault}\\\text{current generated}\\\text{(swamps } I_{TH})}} \times \underbrace{\left(\frac{R_N}{R_G + R_N}\right)}_{\substack{\text{portion of}\\\text{fault current}\\\text{shunted}\\\text{around GFI}}}$$

$$\times \underbrace{\left(\frac{1\text{ turn}}{1000\text{ turns}}\right)}_{\substack{\text{current}\\\text{division of}\\\text{input sense}\\\text{transformer}}} \times \underbrace{\left(\frac{1}{2}\right)}_{\substack{C_t\text{ charging}\\\text{on half-}\\\text{cycles only}}} \times \underbrace{(0.91)}_{\substack{\text{rms to}\\\text{average}\\\text{conversion}}} \qquad (6)$$

therefore:

$$C_t = \frac{\left[\left(\frac{120}{500}\right) \times \left(\frac{0.4}{1.6+0.4}\right) \times \left(\frac{1}{1000}\right) \times \left(\frac{1}{2}\right) \times (0.91)\right] \times 0.0008}{17.5} \qquad (7)$$

$C_t =$ 0.01 μF

Application Circuits (Continued)

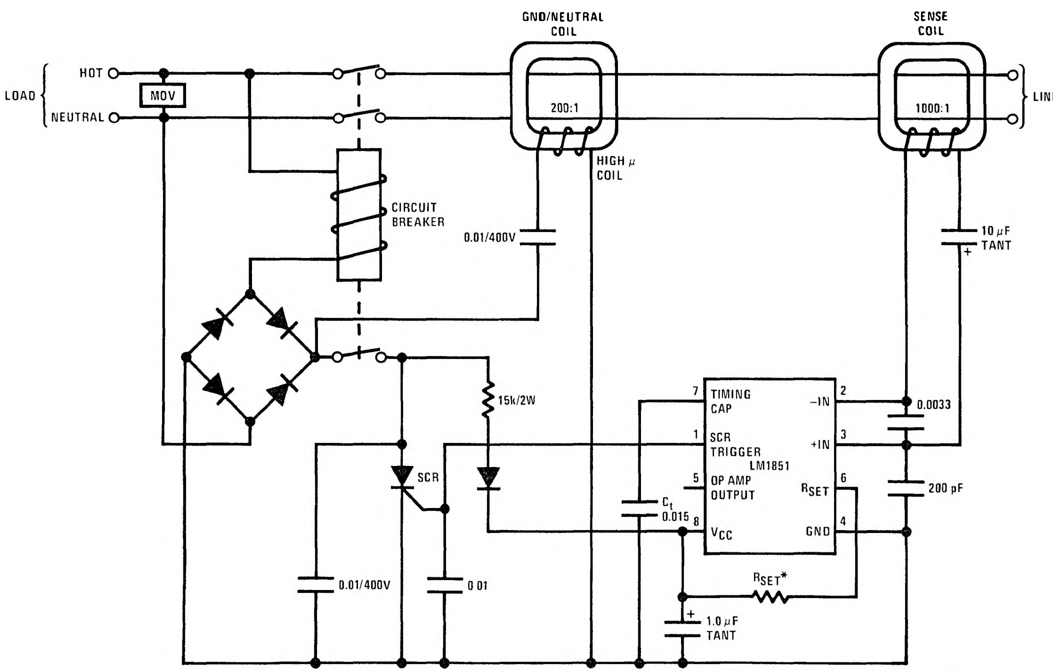
in practice, the actual value of C1 will have to be modified to include the effects of the neutral loop upon the net charging current. The effect of neutral loop induced currents is difficult to quantize, but typically they sum with normal fault currents, thus allowing a larger value of C1.

For UL943 requirements, 0.015 μF has been found to be the best compromise between timing and noise.

For those GFI standards not requiring grounded neutral detection, a still larger value capacitor can be used and better noise immunity obtained. The larger capacitor can be accommodated because R_N and R_G are not present, allowing the full fault current, I, to enter the GFI.

In *Figure 2*, grounded neutral detection is accomplished by feeding the neutral coil with 120 Hz energy continuously and allowing some of the energy to couple into the sense transformer during conditions of neutral fault.

Typical Application



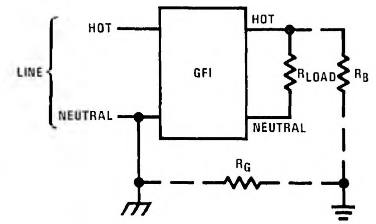
*Adjust R_{SET} for desired sensitivity

TL/H/5177-6

FIGURE 2. 120 Hz Neutral Transformer Approach

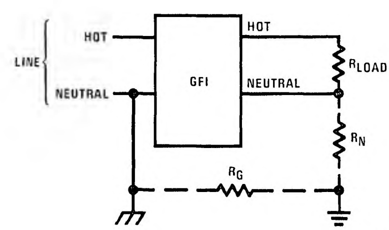
Definition of Terms

Normal Fault: An unintentional electrical path, R_B, between the load terminal of the hot line and the ground, as shown by the dashed lines.



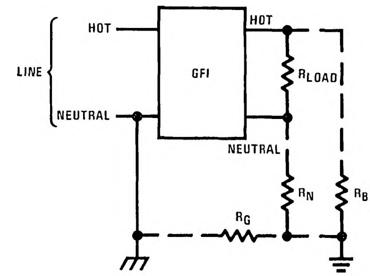
TL/H/5177-7

Grounded Neutral Fault: An unintentional electrical path between the load terminal of the neutral line and the ground, as shown by the dashed lines.



TL/H/5177-8

Normal Fault plus Grounded Neutral Fault: The combination of the normal fault and the grounded neutral fault, as shown by the dashed lines.



TL/H/5177-9