LM25101A/B/C 3A, 2A and 1A High Voltage High-Side and Low-Side Gate Drivers

Check for Samples: LM25101, LM25101A, LM25101B, LM25101C

FEATURES

- **Drives both a high-side and low-side N-Channel MOSFETs**
- **Independent high and low driver logic inputs**
- **Bootstrap supply voltage up to 100V DC**
- **Fast propagation times (25 ns typical)**
- **Drives 1000 pF load with 8 ns rise and fall times**
- **Excellent propagation delay matching (3 ns typical)**
- **Supply rail under-voltage lockout**
- **Low power consumption**
- **Pin compatible with HIP2100/HIP2101**

TYPICAL APPLICATIONS

- **Current Fed push-pull converters**
- **Half and Full Bridge power converters**
- **Synchronous buck converters**
- **Two switch forward power converters**
- **Forward with Active Clamp converters**

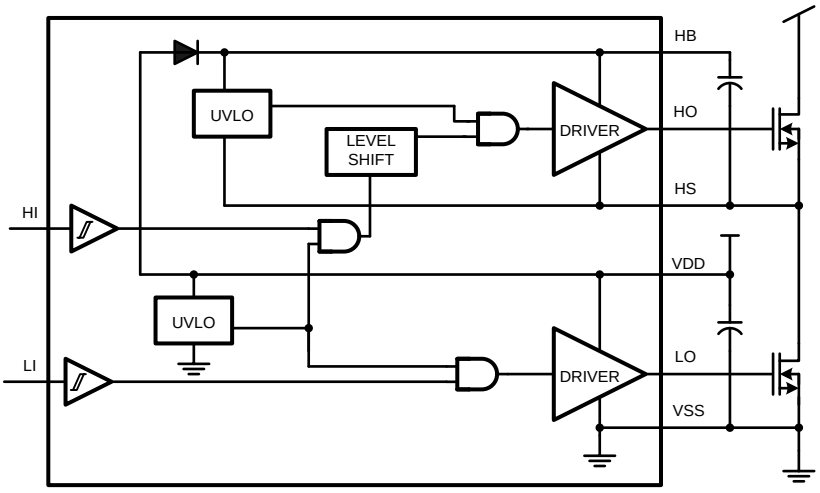
DESCRIPTION

The LM25101A/B/C High Voltage Gate Drivers are designed to drive both the high-side and the low-side N-Channel MOSFETs in a synchronous buck or a half-bridge configuration. The “A” versions provide a full 3A of gate drive while the “B” and “C” versions provide 2A and 1A respectively. The outputs are independently controlled with TTL input thresholds. An integrated high voltage diode is provided to charge the high-side gate drive bootstrap capacitor. A robust level shifter operates at high speed while consuming low power and providing clean level transitions from the control logic to the high-side gate driver. Under-voltage lockout is provided on both the low-side and the high-side power rails. These devices are available in the standard SOIC-8 pin and HSOP-8 pin packages.

Package

- SOIC-8
- HSOP-8

Simplified Block Diagram

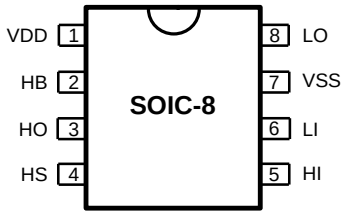


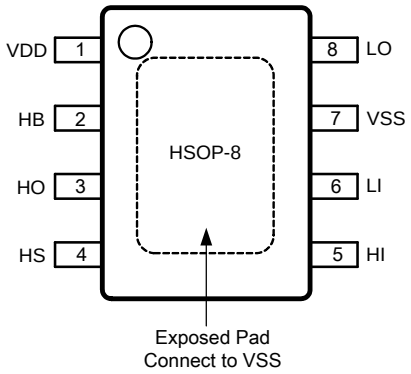
Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

Table 1. Input/Output Options

Part Number	Input Thresholds	Peak Output Current
LM25101A	TTL	3A
LM25101B	TTL	2A
LM25101C	TTL	1A

Connection Diagrams





Pin Descriptions

Pin #		Name	Description	Application Information
SOIC-8	HSOP-8			
1	1	VDD	Positive gate drive supply	Locally decouple to VSS using low ESR/ESL capacitor located as close to the IC as possible.
2	2	HB	High-side gate driver bootstrap rail	Connect the positive terminal of the bootstrap capacitor to HB and the negative terminal to HS. The bootstrap capacitor should be placed as close to the IC as possible.
3	3	HO	High-side gate driver output	Connect to the gate of high-side MOSFET with a short, low inductance path.
4	4	HS	High-side MOSFET source connection	Connect to the bootstrap capacitor negative terminal and the source of the high-side MOSFET.
5	5	HI	High-side driver control input	The LM25101A/B/C inputs have TTL type thresholds. Unused inputs should be tied to ground and not left open.
6	6	LI	Low-side driver control input	The LM25101A/B/C inputs have TTL type thresholds. Unused inputs should be tied to ground and not left open.
7	7	VSS	Ground return	All signals are referenced to this ground.
8	8	LO	Low-side gate driver output	Connect to the gate of the low-side MOSFET with a short, low inductance path.
	EP	EP	Exposed pad	Solder to the ground plane under the IC to aid in heat dissipation.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings[1]

VDD to VSS	−0.3V to +18V
HB to HS	−0.3V to +18V
LI or HI Input	−0.3V to V_{DD} +0.3V
LO Output	−0.3V to V_{DD} +0.3V
HO Output	V_{HS} −0.3V to V_{HB} +0.3V
HS to VSS[2]	−5V to +100V
HB to VSS	100V
Junction Temperature	+150°C
Storage Temperature Range	−55°C to +150°C
ESD Rating, HBM[3]	2 kV

(1) Absolute Maximum Ratings indicate limits beyond which damage to the component may occur. Operating Ratings are conditions under which operation of the device is guaranteed. Operating Ratings do not imply guaranteed performance limits. For guaranteed performance limits and associated test conditions, see the Electrical Characteristics tables.
(2) In the application the HS node is clamped by the body diode of the external lower N-MOSFET, therefore the HS node will generally not exceed -1V. However, in some applications, board resistance and inductance may result in the HS node exceeding this stated voltage transiently. If negative transients occur, the HS voltage must never be more negative than VDD-15V. For example if VDD = 10V, the negative transients at HS must not exceed -5V.
(3) The Human Body Model (HBM) is a 100 pF capacitor discharged through a 1.5kΩ resistor into each pin. 2 kV for all pins except Pin 2, Pin 3 and Pin 4 which are rated at 1000V for HBM. Machine Model (MM) rating is 100V.

Recommended Operating Conditions

VDD	+9V to +14V
HS	−1V to 100V - VDD
HB	V_{HS} +8V to V_{HS} +14V
HS Slew Rate	< 50 V/ns
Junction Temperature	−40°C to +125°C

Electrical Characteristics

Limits in standard type are for T_J = 25°C only; limits in boldface type apply over the junction temperature (T_J) range of -40°C to +125°C. Minimum and Maximum limits are guaranteed through test, design, or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. Unless otherwise specified, V_{DD} = V_{HB} = 12V, V_{SS} = V_{HS} = 0V, No Load on LO or HO [1].

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
SUPPLY CURRENTS						
I_{DD}	VDD Quiescent Current, LM25101A/B/C	LI = HI = 0V		0.25	**0.4**	mA
I_{DDO}	VDD Operating Current	f = 500 kHz		2.0	**3**	mA
I_{HB}	Total HB Quiescent Current	LI = HI = 0V		0.06	**0.2**	mA
I_{HBO}	Total HB Operating Current	f = 500 kHz		1.6	**3**	mA
I_{HBS}	HB to VSS Current, Quiescent	HS = HB = 100V		0.1	**10**	µA
I_{HBSO}	HB to VSS Current, Operating	f = 500 kHz		0.4		mA
INPUT PINS						
V_{IL}	Input Voltage Threshold LM25101A/B/C	Rising Edge	**1.3**	1.8	**2.3**	V
V_{IHYS}	Input Voltage Hysteresis LM25101A/B/C			50		mV
R_I	Input Pulldown Resistance		**100**	200	**400**	kΩ
UNDER VOLTAGE PROTECTION						
V_{DDR}	VDD Rising Threshold		**6.0**	6.9	**7.4**	V
V_{DDH}	VDD Threshold Hysteresis			0.5		V
V_{HBR}	HB Rising Threshold		**5.7**	6.6	**7.1**	V
V_{HBH}	HB Threshold Hysteresis			0.4		V
BOOT STRAP DIODE						

(1) Min and Max limits are 100% production tested at 25°C. Limits over the operating temperature range are guaranteed through correlation using Statistical Quality Control (SQC) methods. Limits are used to calculate National's Average Outgoing Quality Level (AOQL).

Electrical Characteristics (continued)

Limits in standard type are for T_J = 25°C only; limits in boldface type apply over the junction temperature (T_J) range of -40°C to +125°C. Minimum and Maximum limits are guaranteed through test, design, or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. Unless otherwise specified, V_{DD} = V_{HB} = 12V, V_{SS} = V_{HS} = 0V, No Load on LO or HO (1).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DL}	Low-Current Forward Voltage	I_{VDD-HB} = 100 µA		0.52	**0.85**	V
V_{DH}	High-Current Forward Voltage	I_{VDD-HB} = 100 mA		0.8	**1**	V
RD	Dynamic Resistance LM25101A/B/C	I_{VDD-HB} = 100 mA		1.0	1.65	Ω
LO & HO GATE DRIVER						
V_{OL}	Low-Level Output Voltage LM25101A	I_{HO} = I_{LO} = 100 mA		0.12	**0.25**	V
	Low-Level Output Voltage LM25101B			0.16	**0.4**	
	Low-Level Output Voltage LM25101C			0.28	**0.65**	
V_{OH}	High-Level Output Voltage LM25101A	I_{HO} = I_{LO} = 100 mA V_{OH} = VDD– LO or V_{OH} = HB - HO		0.24	**0.45**	V
	High-Level Output Voltage LM25101B			0.28	**0.60**	
	High-Level Output Voltage LM25101C			0.60	**1.10**	
I_{OHL}	Peak Pullup Current LM25101A	HO, LO = 0V		3		A
	Peak Pullup Current LM25101B			2		
	Peak Pullup Current LM25101C			1		
I_{OLL}	Peak Pulldown Current LM25101A	HO, LO = 12V		3		A
	Peak Pulldown Current LM25101B			2		
	Peak Pulldown Current LM25101C			1		
THERMAL RESISTANCE						
θ_{JA}	Junction to Ambient (2)	SOIC-8		170		°C/W
		HSOP-8		40		

(2) The θ_{JA} is not a given constant for the package and depends on the printed circuit board design and the operating environment.

Switching Characteristics

Limits in standard type are for T_J = 25°C only; limits in boldface type apply over the junction temperature (T_J) range of -40°C to +125°C. Minimum and Maximum limits are guaranteed through test, design, or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. Unless otherwise specified, $V_{DD} = V_{HB}$ = 12V, $V_{SS} = V_{HS}$ = 0V, No Load on LO or HO (1).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{LPHL}	LO Turn-Off Propagation Delay	LI Falling to LO Falling		22	**56**	ns
t_{LPLH}	LO Turn-On Propagation Delay	LI Rising to LO Rising		26	**56**	ns
t_{HPHL}	HO Turn-Off Propagation Delay	HI Falling to HO Falling		22	**56**	ns
t_{HPLH}	LO Turn-On Propagation Delay	HI Rising to HO Rising		26	**56**	ns
t_{MON}	Delay Matching: LO on & HO Off			4	**10**	ns
t_{MOFF}	Delay Matching: LO on & HO Off			4	**10**	ns
t_{RC}, t_{FC}	Either Output Rise/Fall Time	C_L = 1000 pF		8		ns
t_R	Output Rise Time (3V to 9V) LM25101A	C_L = 0.1 µF		430		ns
	Output Rise Time (3V to 9V) LM25101B			570		
	Output Rise Time (3V to 9V) LM25101C			990		
t_F	Output Fall Time (3V to 9V) LM25101A	C_L = 0.1 µF		260		ns
	Output Fall Time (3V to 9V) LM25101B			430		
	Output Fall Time (3V to 9V) LM25101C			715		
t_{PW}	Minimum input pulse duration that changes the output			50		ns
t_{BS}	Bootstrap diode reverse recovery time	I_F = 100 mA, I_R = 100 mA		37		ns

(1) Min and Max limits are 100% production tested at 25°C. Limits over the operating temperature range are guaranteed through correlation using Statistical Quality Control (SQC) methods. Limits are used to calculate National's Average Outgoing Quality Level (AOQL).

Typical Performance Characteristics

Peak Sourcing Current vs VDD

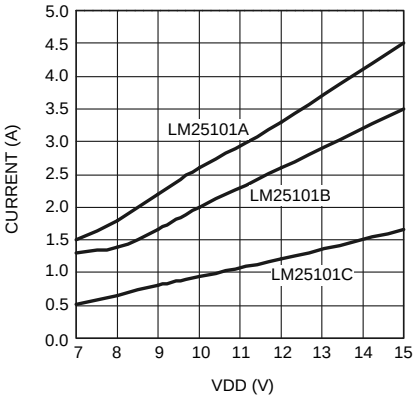


Figure 1.

Peak Sinking Current vs VDD

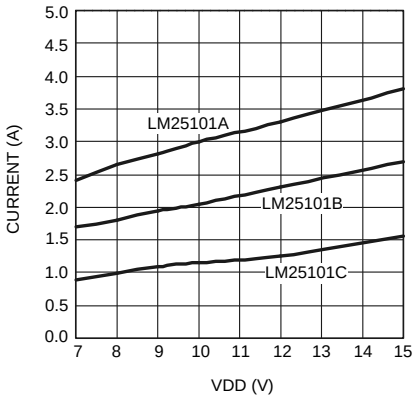


Figure 2.

Sink Current vs Output Voltage

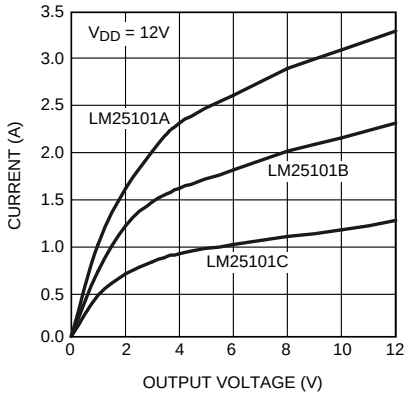


Figure 3.

Source Current vs Output Voltage

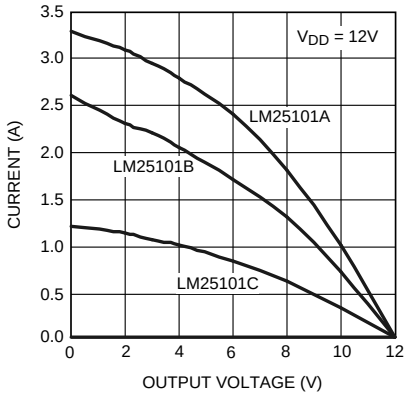


Figure 4.

LM25101A/B/C I_{DD} vs Frequency

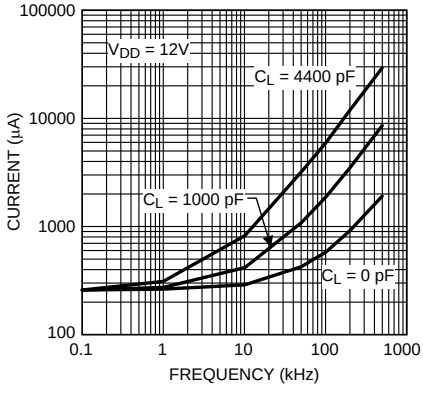


Figure 5.

Operating Current vs Temperature

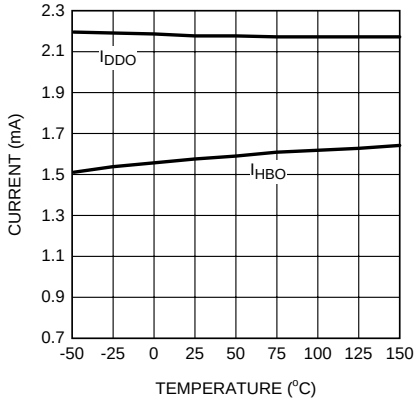


Figure 6.

Typical Performance Characteristics (continued)

I_{HB} vs Frequency

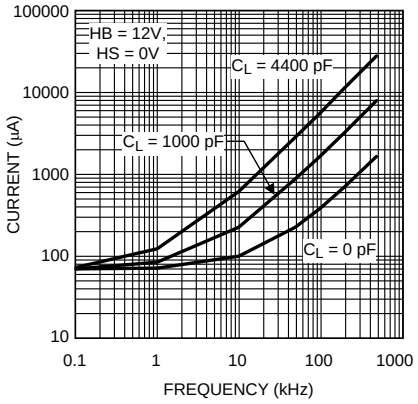


Figure 7.

Quiescent Current vs Supply Voltage

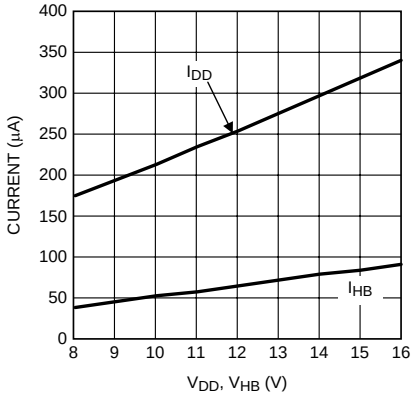


Figure 8.

Quiescent Current vs Temperature

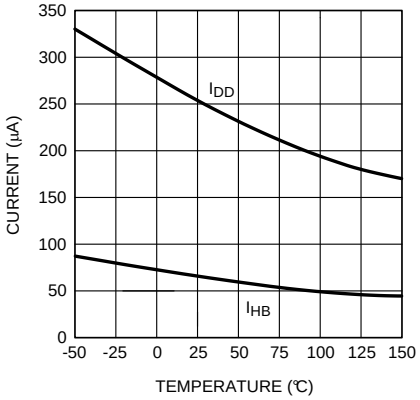


Figure 9.

Undervoltage Rising Thresholds vs Temperature

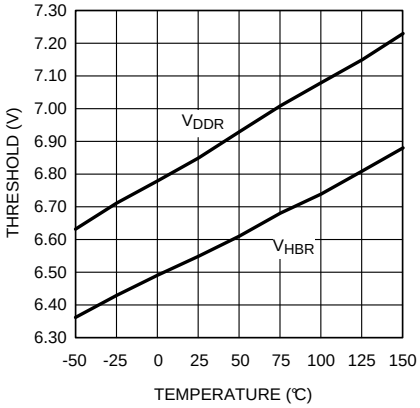


Figure 10.

Undervoltage Threshold Hysteresis vs Temperature

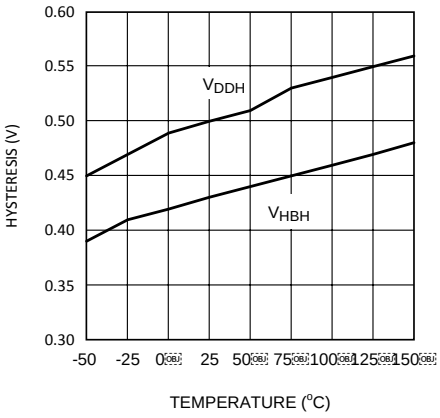


Figure 11.

Bootstrap Diode Forward Voltage

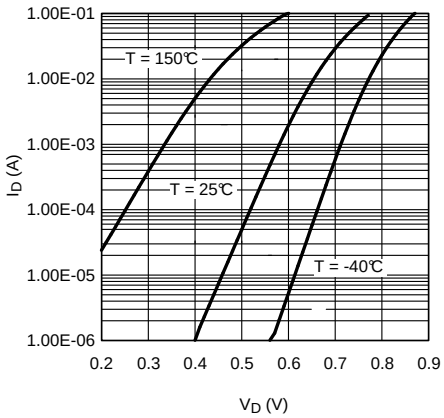


Figure 12.

Typical Performance Characteristics (continued)

LM25101A/B/C Input Threshold vs Temperature

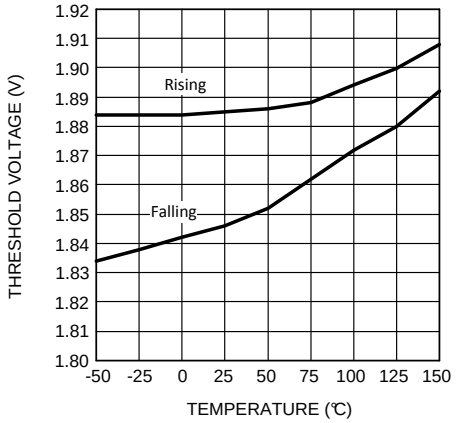


Figure 13.

LM25101A/B/C Input Threshold vs VDD

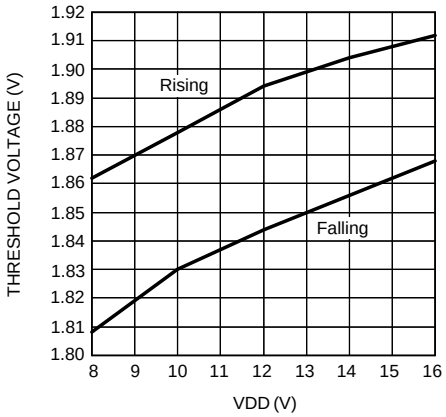


Figure 14.

LM25101A/B/C Propagation Delay vs Temperature

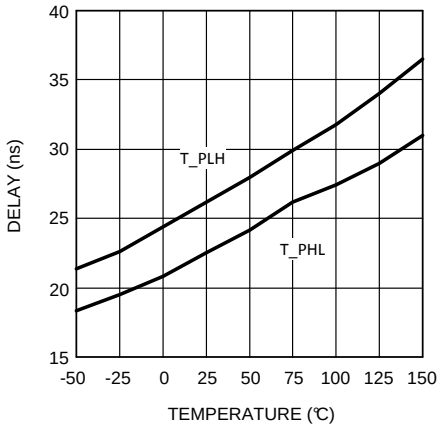


Figure 15.

LO & HO Gate Drive - High Level Output Voltage vs Temperature

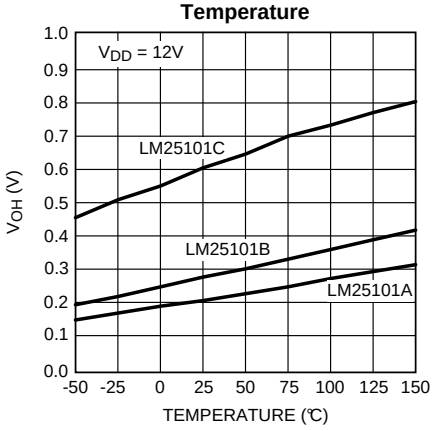


Figure 16.

LO & HO Gate Drive - Low Level Output Voltage vs Temperature

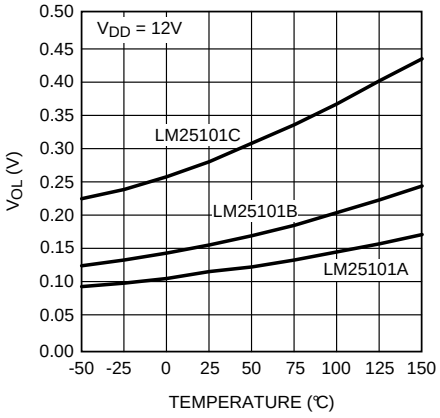


Figure 17.

LO & HO Gate Drive - Output High Voltage vs VDD

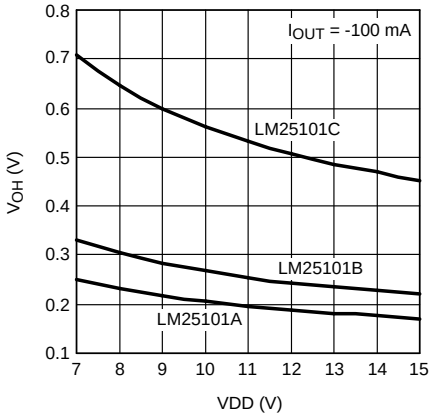


Figure 18.

Typical Performance Characteristics (continued)

LO & HO Gate Drive - Output Low Voltage vs VDD

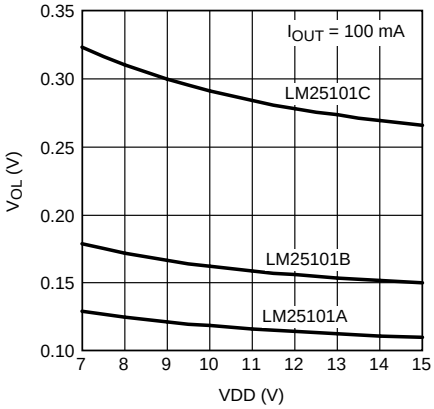
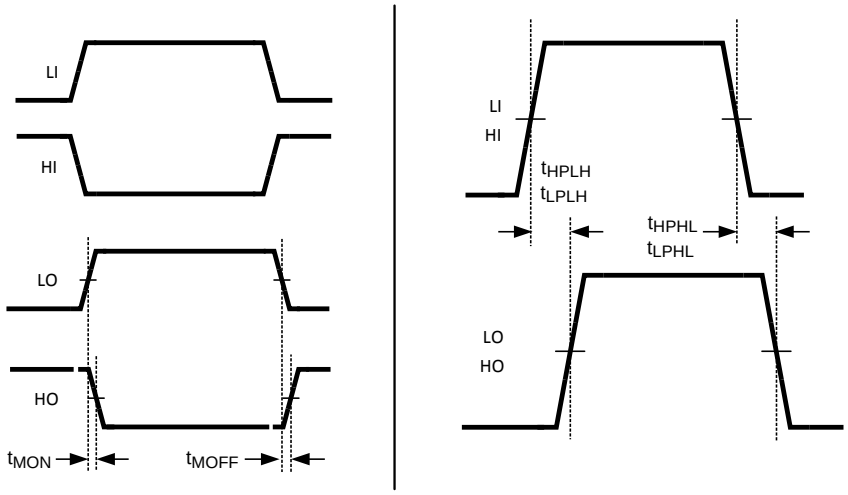


Figure 19.

TIMING DIAGRAM



Layout Considerations

The optimum performance of high and low-side gate drivers cannot be achieved without taking due considerations during circuit board layout. Following points are emphasized.

1. Low ESR / ESL capacitors must be connected close to the IC, between VDD and VSS pins and between the HB and HS pins to support the high peak currents being drawn from VDD during turn-on of the external MOSFET.
2. To prevent large voltage transients at the drain of the top MOSFET, a low ESR electrolytic capacitor must be connected between MOSFET drain and ground (VSS).
3. In order to avoid large negative transients on the switch node (HS pin), the parasitic inductances in the source of top MOSFET and in the drain of the bottom MOSFET (synchronous rectifier) must be minimized.
4. Grounding Considerations:
   (a) The first priority in designing grounding connections is to confine the high peak currents that charge and discharge the MOSFET gate into a minimal physical area. This will decrease the loop inductance and minimize noise issues on the gate terminal of the MOSFET. The MOSFETs should be placed as close as possible to the gate driver.
   (b) The second high current path includes the bootstrap capacitor, the bootstrap diode, the local ground referenced bypass capacitor and low-side MOSFET body diode. The bootstrap capacitor is recharged on a cycle-by-cycle basis through the bootstrap diode from the ground referenced VDD bypass capacitor. The recharging occurs in a short time interval and involves high peak current. Minimizing this loop length and area on the circuit board is important to ensure reliable operation.

A recommended layout pattern for the driver is shown in Figure 20. If possible a single layer placement is preferred.

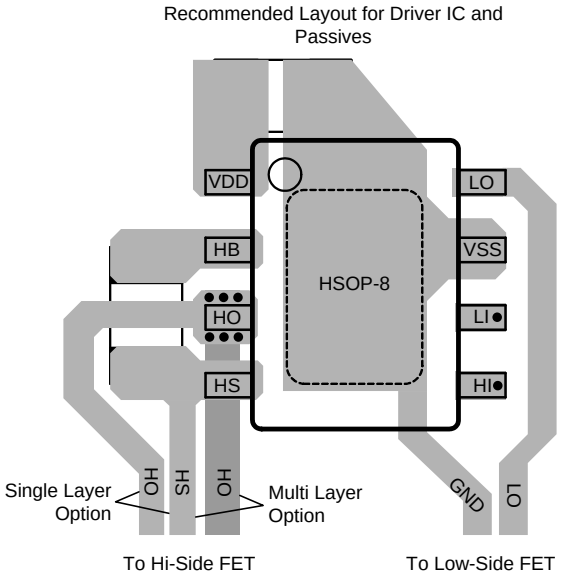


Figure 20. Recommended Layout Pattern

Power Dissipation Considerations

The total IC power dissipation is the sum of the gate driver losses and the bootstrap diode losses. The gate driver losses are related to the switching frequency (f), output load capacitance on LO and HO (C_L), and supply voltage (VDD) and can be roughly calculated as:

$$P_{DGATES} = 2 \bullet f \bullet C_L \bullet V_{DD}^2 \quad (1)$$

There are some additional losses in the gate drivers due to the internal CMOS stages used to buffer the LO and HO outputs. Figure 21 shows the measured gate driver power dissipation versus frequency and load capacitance. At higher frequencies and load capacitance values, the power dissipation is dominated by the power losses driving the output loads and agrees well with Equation 1. This plot can be used to approximate the power losses due to the gate drivers.

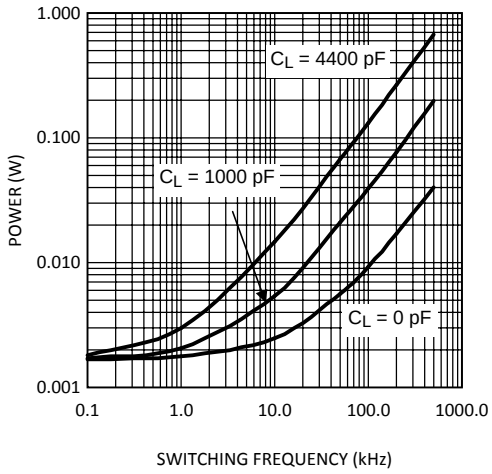


Figure 21. Gate Driver Power Dissipation (LO + HO)
V_{DD} = 12V, Neglecting Diode Losses

The bootstrap diode power loss is the sum of the forward bias power loss that occurs while charging the bootstrap capacitor and the reverse bias power loss that occurs during reverse recovery. Since each of these events happens once per cycle, the diode power loss is proportional to frequency. Larger capacitive loads require more energy to recharge the bootstrap capacitor resulting in more losses. Higher input voltages (V_{IN}) to the half bridge result in higher reverse recovery losses. Figure 22 was generated based on calculations and lab measurements of the diode recovery time and current under several operating conditions. This can be useful for approximating the diode power dissipation.

The total IC power dissipation can be estimated from the previous plots by summing the gate drive losses with the bootstrap diode losses for the intended application.

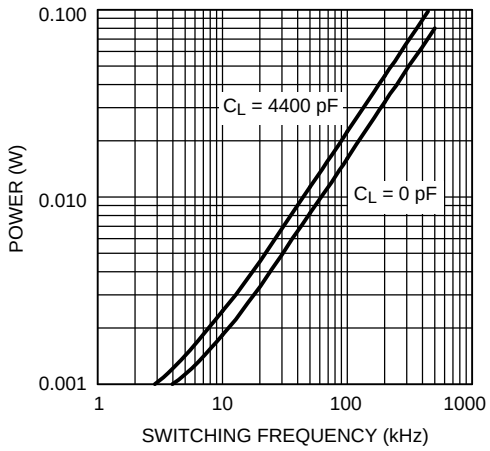
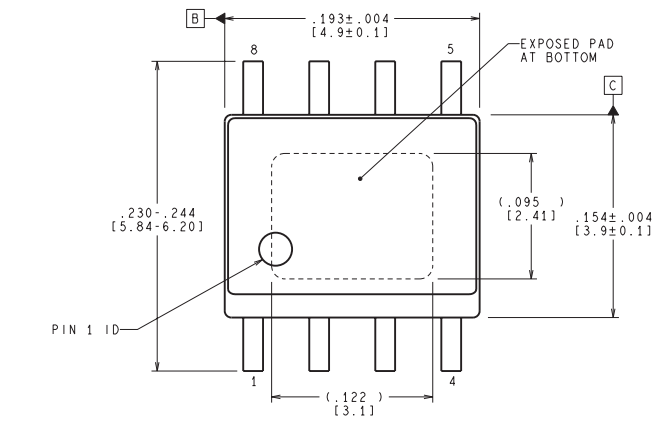
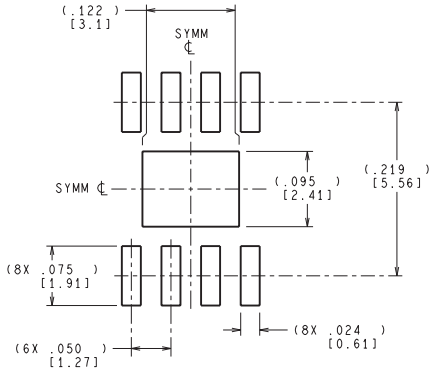


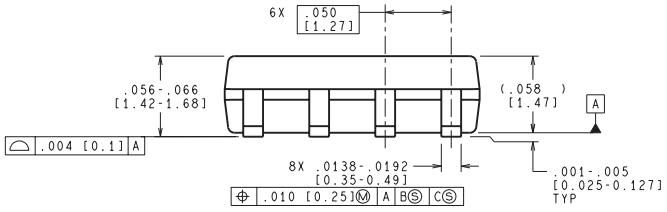
Figure 22. Diode Power Dissipation V_{IN} = 50V

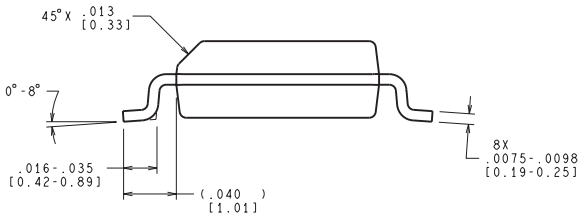
DDA0008B





RECOMMENDED LAND PATTERN

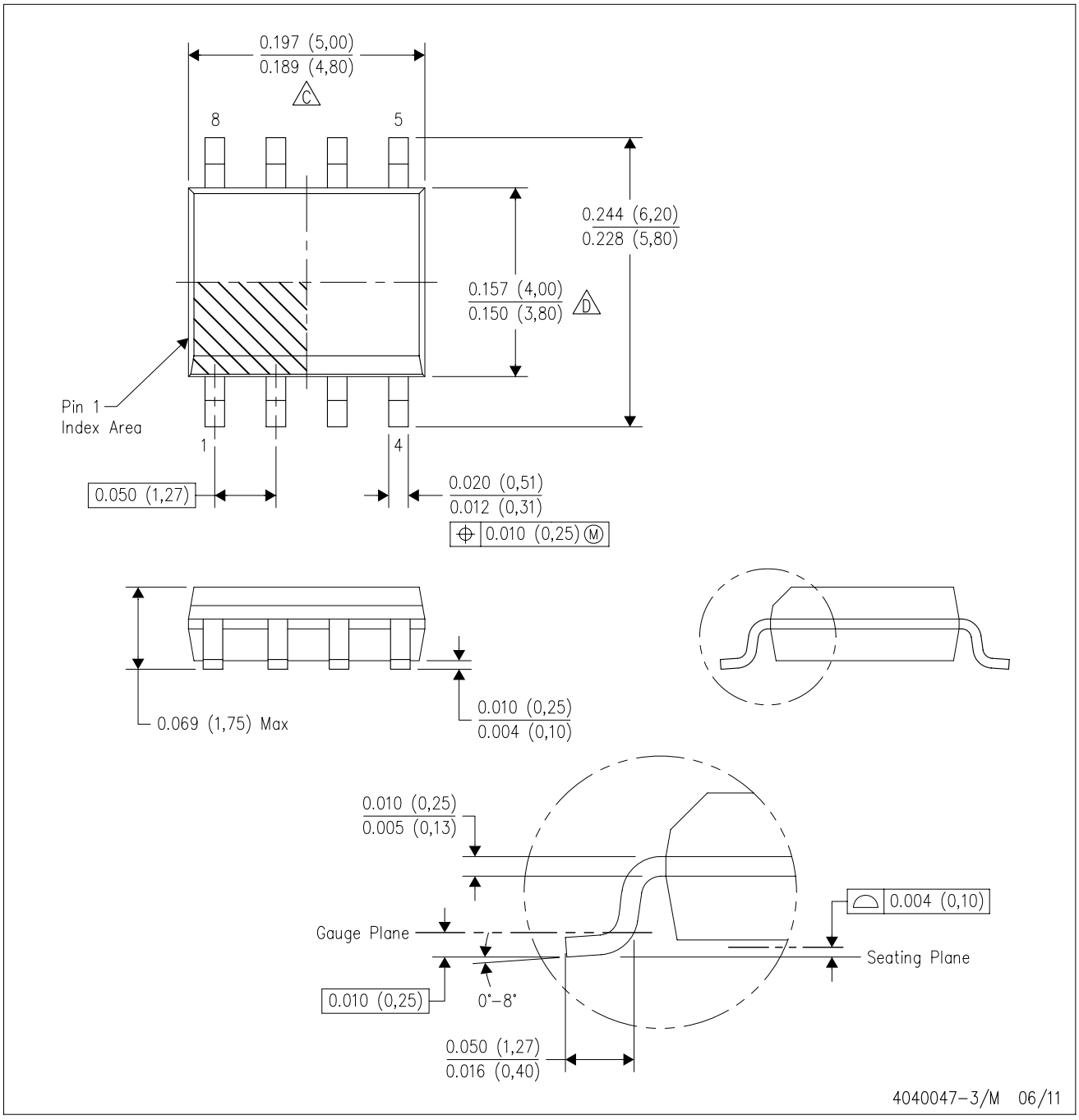




CONTROLLING DIMENSION IS INCH
VALUES IN [ ] ARE MILLIMETERS
DIMENSIONS IN ( ) FOR REFERENCE ONLY

MRA08B (Rev B)

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

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