LM2630 Synchronous Step-Down Power Supply Controller

Check for Samples: LM2630

FEATURES

- **4.5V to 30V Input Range**
- **Adjustable Output (1.8V to 6V)**
- **200 kHz to 400 kHz Adjustable Operating Frequency**
- **Externally Synchronizable**
- **On-board Power Good Function**
- **Precision 1.24V Reference Output**
- **0.8 mA Typical Quiescent Current**
- **0.1 µA Shutdown Current**
- **Thermal Shutdown**
- **Direct Current Limit Protection**
- **Input Undervoltage Lockout**
- **Output Undervoltage Shutdown Protection**
- **Programmable Soft-start Function**
- **Tiny TSSOP Package**

APPLICATIONS

- **Notebook and Subnotebook Computers**
- **Cellular Phones**
- **Portable Instruments**
- **Battery-powered Digital Devices**

DESCRIPTION

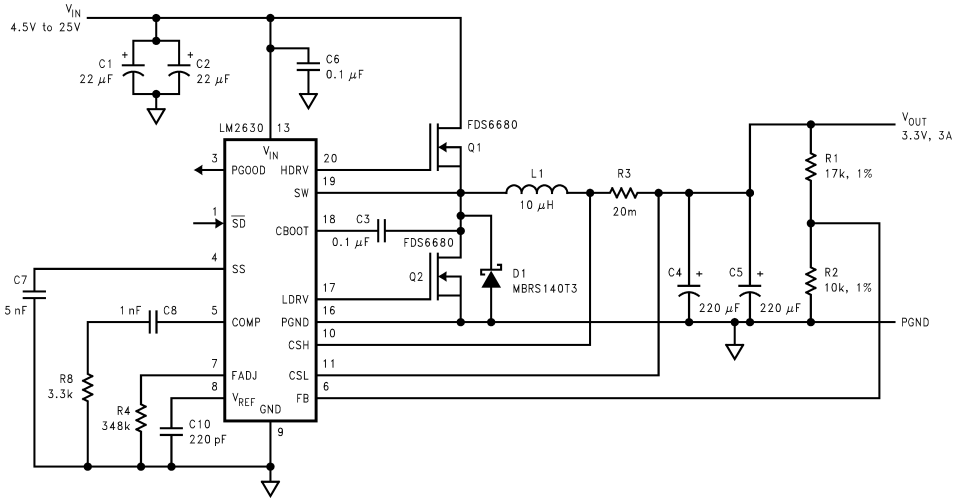
The LM2630 controller provides all the active functions for step-down (buck) switching converters. These dc-to-dc converters provide core CPU power in battery-operated systems.

High efficiency is achieved by using synchronous rectification and pulse-skipping mode operation at light load. Inexpensive N-channel MOSFETs are used to reduce system cost. Bootstrap circuit is used to drive the high-side N-channel MOSFET. Current mode control scheme is used to improve line regulation and transient response, also provides cycle-by-cycle current limiting.

The operating frequency is adjustable between 200 kHz and 400 kHz. An external shutdown pin can be used to disable the device and reduce the quiescent current to 0.1 µA. In low noise applications, bringing the FPWM pin high can force the device to operate in constant frequency mode. Other features include the external synchronization pin, and the PGOOD pin to indicate the state of the output voltage.

Protection circuitry includes thermal shutdown, undervoltage shut down, soft-start capability, and two levels of current limits: The first level simply limits the load current directly; at the second level, if the load pulls the output voltage down below 80% of the regulated value, the chip will shut down. This latched operation is disabled during startup, but an internal timer will enable it if the output does not come up in the preset time.

Typical Application Circuit



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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ABSOLUTE MAXIMUM RATINGS(1)(2)

Voltages from the indicated pins to GND and PGND:	
V_{IN}	−0.3V to 31V
CBOOT	−0.3V to 36V
$\overline{SD}$	−0.3V to 31V
SW	−0.3V to 31V
CSH, CSL	−0.3V to 7V
FPWM, SYNC	−0.3V to 10V
Power Dissipation (T_A = 70°C), (3)	720mW
Storage Temperature Range	−65°C to +150°C
Soldering Dwell Time, Temperature (4)	
Wave	4 sec, 260°C
Infrared	10 sec, 240°C
Vapor Phase	75 sec, 219°C
ESD Rating (5)	1.5 kV

(1) Absolute maximum ratings indicate limits beyond which damage to the device may occur. Electrical specifications do not apply when operating the device outside of its rated operating conditions.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.
(3) The maximum allowable power dissipation is calculated by using $P_{Dmax} = (T_{Jmax} - T_A)/\theta_{JA}$, where T_{Jmax} is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance of the specified package. The 720 mW rating results from using 160°C, 70°C, and 125°C/W for T_{Jmax}, T_A, and θ_{JA} respectively. A θ_{JA} of 125°C/W represents the worst-case condition of no heat sinking of the 20-pin TSSOP. Heat sinking allows the safe dissipation of more power. The Absolute Maximum power dissipation must be derated by 8 mW per °C above 70°C ambient. The LM2630 actively limits its junction temperature to about 160°C.
(4) See http://www.ti.com for other methods of soldering plastic small-outline packages.
(5) For testing purposes, ESD was applied using the human-body model, a 100 pF capacitor discharged through a 1.5 kΩ resistor.

OPERATING RATINGS

V_{IN}	4.5V to 30V
Junction Temperature	−40°C to +125°C

ELECTRICAL CHARACTERISTICS

Specifications in standard type face are for T_j = 25°C and those with **boldface type** apply over **full operating junction temperature range.** V_{IN} =10V, GND = PGND = 0V,unless otherwise stated. (1) (2)

Symbol	Parameter	Conditions	Typical	Limit	Units
System					
V_{IN}	Input Supply Voltage			**4.5** **30**	V(min) V(max)
V_{OUT}	Output Voltage Adjustment Range			**1.8** **6.0**	V(min) V(max)
$\Delta V_{OUT}/V_{OUT}$	Load Regulation	0 mV ≤ (CSH-CSL) ≤ 75 mV	0.3		%
$\Delta V_{OUT}/V_{OUT}$	Line Regulation	4.5 ≤ V_{IN} ≤ 30V	0.002		%/V
I_{IN}	Input Supply Current with the Switching Controller ON	V_{FB} = 1V, V_{CSH} = 2.15V, V_{CSL} = 2.1V	0.8		mA
				1.2/**1.4**	mA(max)

(1) A typical is the center of characterization data taken with $T_A = T_J$ = 25°C. Typicals are not ensured.
(2) All limits are specified. All electrical characteristics having room-temperature limits are tested during production with $T_A = T_J$ = 25°C. All hot and cold limits are specified by correlating the electrical characteristics to process and temperature variations and applying statistical process control.

ELECTRICAL CHARACTERISTICS (continued)

Specifications in standard type face are for T_j = 25°C and those with **boldface type** apply over **full operating junction temperature range.** V_{IN} =10V, GND = PGND = 0V,unless otherwise stated. (1) (2)

Symbol	Parameter	Conditions	Typical	Limit	Units
	Input Supply Current with the Switching Controller ON (Internal Rail is Supplied from CSL Pin)	V_{FB} = 1V, V_{CSH} = 5.15V, V_{CSL} = 5V	0.15		mA
	Input Supply Current with the IC Shut Down	$V_{\overline{SD}}$ = 0V, V_{IN} = 30V	0.1		µA
				3 (3)	µA(max)
	Minimum Output Voltage for CSL Providing the Internal Rail		3		V
I_{SS}	Soft Start Source Current	V_{SS} = 1.5V	10		µA
				5	µA(min)
				13	µA(max)
	Soft Start Sink Current	V_{SS} = 1.5V	20		µA
V_{CL}	Current Limit Voltage (Voltage from CSH to CSL)	V_{FB} = 1V, V_{CSL} = 1.8V	110		mV
				90/**80**	mV(min)
				130/**140**	mV(max)
	V_{IN} Undervoltage Shutdown Latch Threshold	Rising Edge	3.5		V
				2.8	V(min)
	V_{OUT} Undervoltage Shutdown Latch Threshold		80		% V_{OUT}
				65	% V_{OUT}(min)
	V_{OUT} Low Regulation Comparator Enable Threshold		97		% V_{OUT}
	Hysteresis of Low Regulation Comparator		2		% V_{OUT}
	Regulator Window Detector Thresholds (PGOOD from High to Low)		91 or 109		% V_{OUT}
	Regulator Window Detector Thresholds (PGOOD from Low to High)		97 or 103		% V_{OUT}
Gate Drive					
V_{BOOT}	Bootstrap Voltage (Voltage from CBOOT to SW)	CBOOT Sourcing 100 µA	4.5		V
				4.0	V(min)
I_{BOOT}	CBOOT Leakage Current	V_{CBOOT} = 7V	100		nA
	High Drive Source Current	V_{HDRV} = 0V, V_{CBOOT} = 5V	0.3		A
	High Drive Sink Current	HDRV Forced to 5V	0.45		A
	Low Drive Source Current	LDRV Forced to 0V	0.35		A
	Low Drive Sink Current	LDRV Forced to 5V	0.55		A
	High-Side FET On-Resistance HDRV or LDRV		8		Ω
	Low-Side FET On-Resistance HDRV or LDRV		4		Ω

(3) This limit is specified by design.

ELECTRICAL CHARACTERISTICS (continued)

Specifications in standard type face are for T_j = 25°C and those with **boldface type** apply over **full operating junction temperature range.** V_{IN} =10V, GND = PGND = 0V,unless otherwise stated. (1) (2)

Symbol	Parameter	Conditions	Typical	Limit	Units
Oscillator					
F_{OSC}	Oscillator Frequency	FADJ Open	200		kHz
				172/**162**	kHz(min)
				228/**230**	kHz(max)
	Oscillator Frequency	FADJ Sourcing 2.94 µA (4)	300		kHz
				255	kHz(min)
				345	kHz(max)
V_{FADJ}	Voltage at FADJ pin		1.03		V
D_{MAX}	Maximum Duty Cycle	FADJ Open	96		%
				92	%(min)
	Maximum Frequency of Synchronization	Low-Going 200 ns Wide Rectangular Pulses Applied at 400 kHz at the SYNC Input		400	kHz(min)
	Minimum Pulse Width of the SYNC Signal	SYNC Pulses are Low-Going		200	ns(min)
Error Amplifier					
I_{FB}	Feedback Input Bias Current	V_{FB} = 1.3V, V_{CSH} = 5.15V, V_{CSL} = 5V	100		nA
I_{COMP}	COMP Output Source Current	V_{COMP} = 0.2V, V_{FB} = 1V	50		µA
	COMP Output Sink Current	V_{COMP} = 1.2V, V_{FB} = 1.4V	50		µA
Voltage Reference					
V_{REF}	Reference Voltage (Nominal))	I_{REF} = 0µA	1.238		V
				1.213/**1.208**	V(min)
				1.263/**1.268**	V(max)
V_{REF}	Reference Voltage (Line Regulation)	4.5V < V_{IN} < 30V	1.238		V
				1.213/**1.208**	V(min)
				1.263/**1.268**	V(max)
	Reference Voltage (Load Regulation)	0 µA < I_{REF} < 50 µA	1.238		V
				1.213/**1.208**	V(min)
				1.263/**1.268**	V(max)
Logic Inputs and Outputs					
V_{IH}	Minimum High Level Input Voltage ($\overline{SD}$, FPWM and SYNC)			**2.4**	V(min)
V_{IL}	Maximum Low Level Input Voltage (FPWM and SYNC)			**0.8**	V(max)
	Maximum Low Level Input Voltage ($\overline{SD}$)			**0.5**	V(max)
	Maximum Input Leakage Curren1t ($\overline{SD}$, FPWM and SYNC)	Logic Input Voltage 0V or 5V	±0.1		µA
V_{OH}	PGOOD High Level Output Voltage	PGOOD Sourcing 50 µA	2.7		V
				2.4	V(min)
V_{OL}	PGOOD Low Level Output Voltage	PGOOD Sinking 50 µA	0		V
				0.5	V(max)

(4) Pulling 2.94 µA out of FADJ pin simulates adjusting the oscillator frequency with a 350 kΩ resistor connected from FADJ to GND.

TYPICAL PERFORMANCE CHARACTERISTICS

Efficiency vs Load Current (FPWM = Low, V_{OUT} = 3.3V)

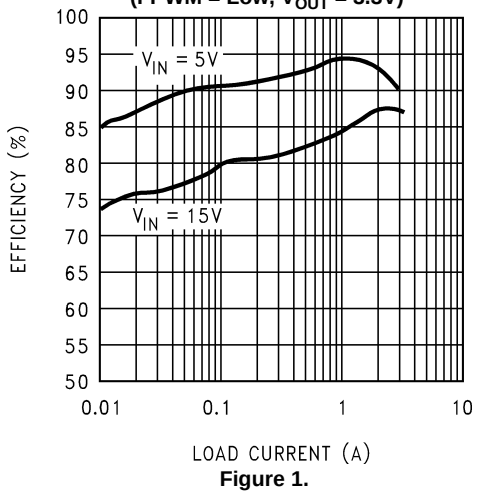


Figure 1.

Efficiency (FPWM = High, Input Voltage = 16V, V_{OUT}= 2.9V)

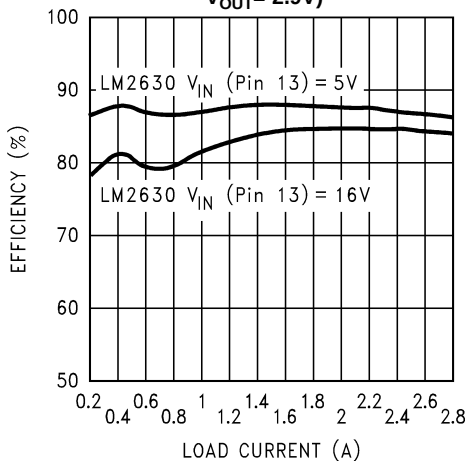


Figure 2.

Quiescent Supply Current vs Supply Voltage (Not Switching, FPWM = Low, V_{OUT} = 2.0V)

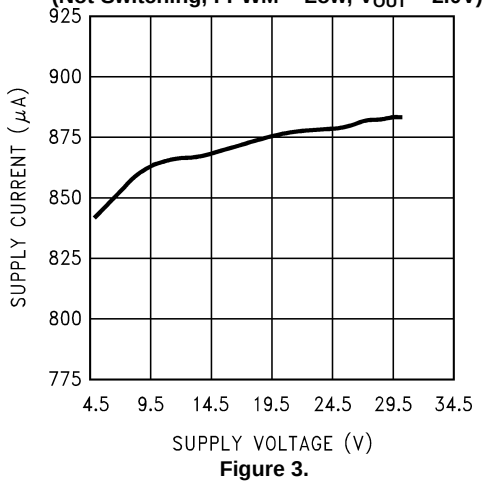


Figure 3.

Quiescent Supply Current vs Supply Voltage (FPWM = Low, V_{OUT} = 3.3V)

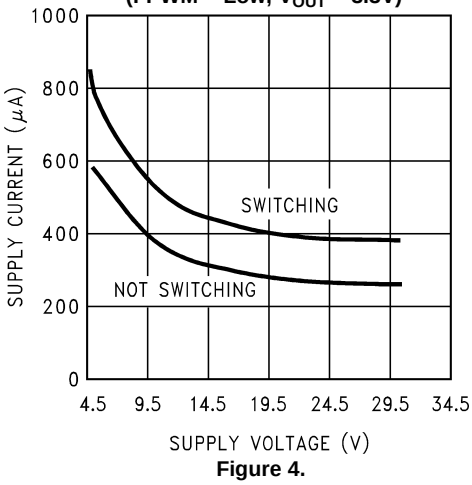


Figure 4.

Supply Current vs Oscillator Frequency (FPWM = High)

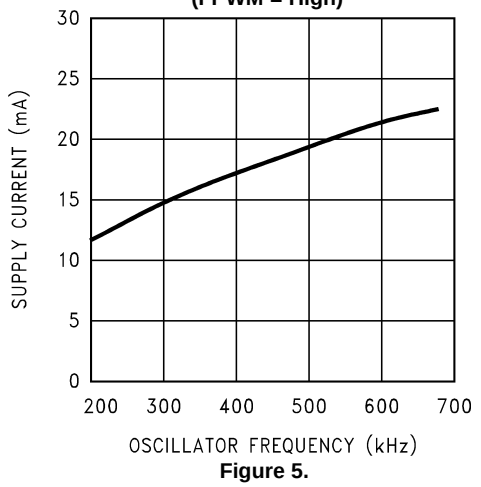


Figure 5.

Oscillator Frequency vs Adjusting Resistor

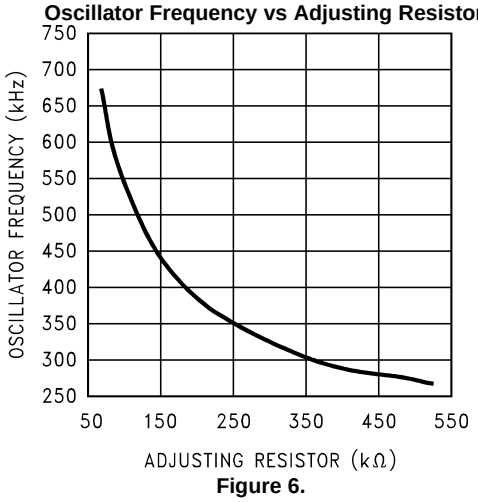


Figure 6.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Oscillator Frequency vs Junction Temperature

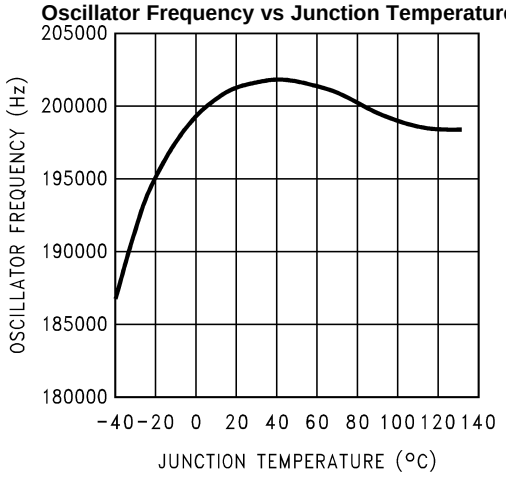


Figure 7.

Reference Voltage vs Junction Temperature

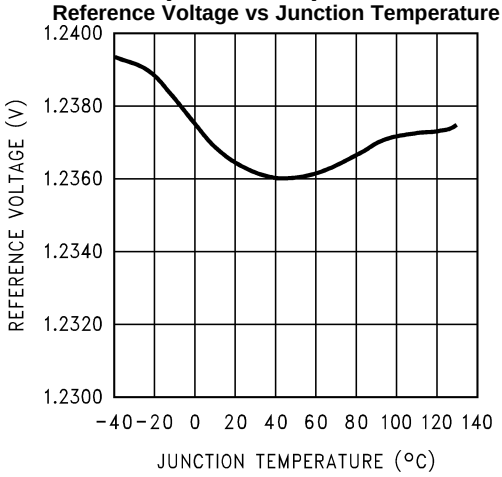


Figure 8.

CONNECTION DIAGRAM

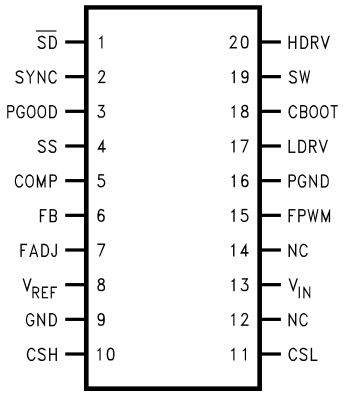


Figure 9. Top View
20-Lead TSSOP (PW)
See Package Number PW0020A

PIN DESCRIPTIONS

Pin	Name	Function
1	$\overline{SD}$	Shutdown control input, active low.
2	SYNC	Oscillator synchronization input. Connect this pin to ground if not used.
3	PGOOD	A constant monitor on the output voltage. PGOOD will go low if the output voltage exceeds ±9% of its nominal value. Once PGOOD goes low, it will go high if the output moves within ±3% of its nominal value.
4	SS	The soft-start control pin. A capacitor connected from this pin to ground sets the ramp time to full current output.
5	COMP	Compensation network connection (connected to the output of the voltage error amplifier).
6	FB	Output voltage feedback input (connected to the center of the external resistor divider).
7	FADJ	Frequency adjustment input.
8	VREF	The output of the precision reference.
9	GND	Low-noise analog ground.
10	CSH	Current-sense positive input.
11	CSL	Current-sense negative input.
12	NC	No internal connection.
13	V_{IN}	Main power supply pin.
14	NC	No internal connection.
15	FPWM	When FPWM is high, pulse-skipping mode operation at light load is disabled. The converter is forced to operate in constant frequency mode.
16	PGND	Power ground.
17	LDRV	Low-side gate-drive output.
18	CBOOT	Bootstrap capacitor connection for high-side gate drive.
19	SW	Switched-node connection, which is connected with the source of the high-side MOSFET.
20	HDRV	High-side gate-drive output. HDRV is a floating drive output that rides on SW voltage.

Block Diagram

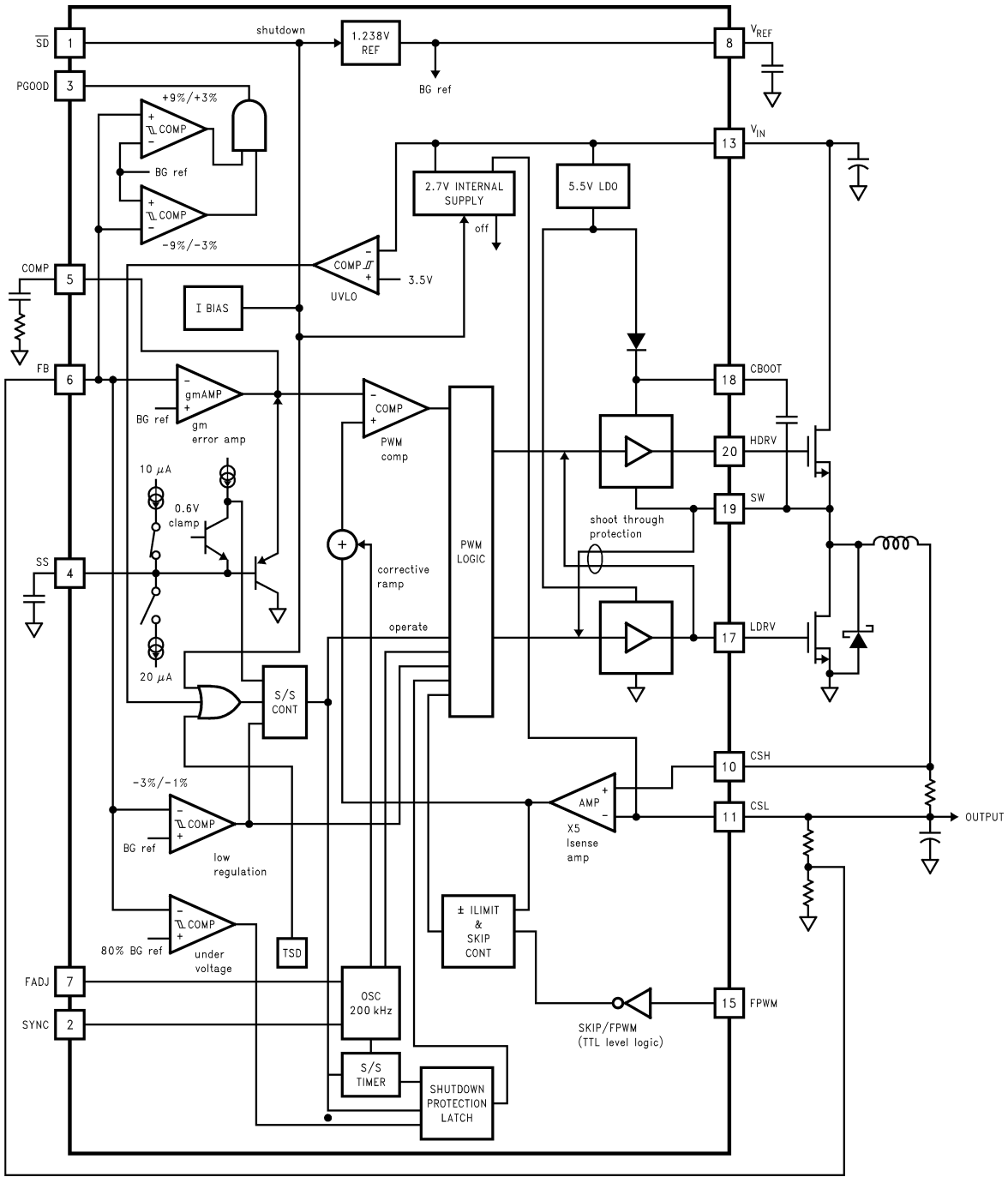


Figure 10. LM2630 Block Diagram

OPERATION

BASIC OPERATION OF THE CURRENT MODE CONTROLLED SWITCHING REGULATOR

The main control loop includes the error amplifier, the current amplifier and PWM comparator (as shown in Figure 10). During heavy load or any load with FPWM mode enabled, the controller is in constant frequency current mode operation: the high-side switch is turned on at the beginning of each clock cycle, and the output of the error amplifier is compared with the sensed inductor current ramp; once the ramp reaches the control level set by the error amplifier, the PWM comparator reset the driver logic to turn off the high-side switch; the low-side switch is turned on after certain delay (the voltage at the SW pin is sensed and the low-side switch is turned on once the SW pin voltage reaches zero. A preset maximum delay is 100 ns). The low-side switch stays on until the end of the cycle or until the inductor current reaches zero; when this occurs, the zero cross detector will disable the low-side driver to turn off the low-side switch. The zero cross detector is disabled in FPWM mode.

For any peak current mode step-down converter, a compensation ramp is needed to avoid subharmonic oscillations when the duty cycle is higher than 50%. For the LM2630, this compensation ramp is internally set to equal the maximum down slope of the current amplifier output:

$$M_c = M_{DOWN\ (MAX)} = n \times R_{SEN} \times \frac{V_{OUT\ (MAX)}}{L}$$

Where n = 5 is the gain of the current sense amplifier. The maximum output voltage equals 6V. Also, a 10 µH inductor and a 0.025Ω sense resistor are assumed to determine the internal compensation ramp. Different values of inductor and sense resistor can be used as long as the resulted M_{DOWN} (= n x R_{SEN} x V_{OUT}/L) is less than M_C.

PULSE-SKIPPING MODE AT LIGHT LOAD

Pulse-skipping mode can be enabled by pulling PFWM pin low. This mode decreases switching frequency at light loads to reduce the switching frequency related losses. If PFWM is set at low, the controller goes into the pulse-skipping mode when the sensed inductor current goes below the 25 mV threshold set by the pulse-skipping comparator. In the pulse-skipping mode, the high-side switch only turns on at the beginning of a clock cycle when the voltage at the feedback pin falls below the reference voltage. Once the switch is on, it stays on until the sensed current rises to the 25 mV threshold

FAST TRANSIENT RESPONSE

When the output voltage fails to exceed 97% of the nominal level, the low voltage regulation(LREG) comparator will set the PWM logic to turn the high-side switch on at maximum duty cycle. This improves transient response since it bypasses the error amplifier and PWM comparator. During start-up, the LREG is disabled.

BOOST HIGH-SIDE GATE DRIVE

A flying capacitor is used to bootstrap the power supply for the high-side driver as illustrated in Figure 10. The boost capacitor is charged from an internal voltage rail (about 5.5V) through an internal diode when the synchronous rectifier (low-side MOSFET) is on, and then boosts up the high-side gate voltage to turn high-side MOSFET on at the beginning of next cycle. The internal diode connecting between the VIN pin and the CBOOT pin reduces the count of external components. For low input voltage application (Vin < 5V), some external charge pump circuitry can be used to boost the gate voltage in order to reduce conduction loss. Details will be discussed in the Application Circuits section.

SUPPLY VOLTAGE FOR THE LM2630

When 5V is available, it is recommended to connect LM2630 V_{IN} (pin13) to 5V. This can improve efficiency (see the Figure 2 in Typical Performance Characteristics), and also reduce power dissipation inside the IC. Since the 5V supply is only used to power the LM2630 (including the gate charge for the external MOSFETs), it only requires a small amount of current.

REFERENCE

The 1.238V reference is of ±2.4% accuracy over temperature. A 220 pF capacitor is recommended between the V_{REF} pin and ground. The load at the V_{REF} pin should not exceed 100µA.

FREQUENCY CONTROL PIN (FADJ) AND SYNC PIN

With the FADJ pin open, the switching frequency is 200 kHz. The frequency can be increased by connecting a resistor between FADJ and ground. The device can also be synchronized with an external CMOS or TTL logic clock in the range from 200 kHz to 400 kHz. It is recommended to connect the SYNC pin to ground if not used.

PROTECTIONS

The current limit comparator provides the cycle-by-cycle current limit function by turning off the high-side MOSFET whenever the sensed current reaches 110 mV. A second level of current limit is accomplished by the 80% low voltage detector: if the load pulls the output voltage down below 80% of the nominal value, the device will turn off the high-side MOSFET and turn on the low-side MOSFET in a latched condition. This protection feature is disabled during startup. The latched condition can be reset by shutting the device down and then powering it up. Built-in input undervoltage lockout circuit will keep most of the internal function blocks off until the input voltage rises to about 3.5V.

SOFT START

A capacitor at the SS pin provides the soft start feature. When the regulator is first powered up, or when the $\overline{SD}$ pin goes high, a 10µA current source charges up the SS capacitor from the 0.6V clamping voltage. The switch duty cycle starts with narrow pulses and gradually get wider as the SS pin voltage ramps up to about 1.3V, above which the duty cycle will be controlled by the maximum current limit until the output voltage rises to the nominal value and the regulator starts to operate in the normal current mode PWM control. The LM2630 use a digital counter, referenced to the oscillator frequency, to set the soft start timeout. The timeout is dependent on the switching frequency (timeout = $4096/F_S$). If the output voltage doesn't move within the ±3% window of the nominal value during this period, the device will latch itself off.

POWER GOOD

The LM2630 provides a power good signal by monitoring the voltage at the FB pin and compared the feedback voltage with the V_{REF} voltage. Once the output voltage exceeds the ±9% window of the nominal value, the PGOOD pin goes low, and stays low until the output voltage returns to the ±3% window of the nominal value.

Design Procedure

Guidelines for selecting external components are discussed in this section.

INDUCTOR SELECTION

The most critical parameters for the inductor are the inductance, peak current and the dc resistance. The inductance is related to the switching frequency and the ripple current:

$$L = \frac{(V_{IN} - V_{OUT})\, V_{OUT}}{V_{IN} \times I_{RIPPLE} \times F_S}$$

Higher switching frequency allows smaller inductor, but reduces the efficiency. A higher value of ripple current reduces inductance, but increase the conductance loss, core loss, current stress for the inductor and switch devices, and requires a bigger output capacitor for the same output voltage ripple requirement. A reasonable value is setting the ripple current to be 30% of the dc output current. Since the ripple current increase with the input voltage, the maximum input voltage is always used to determine the inductance. The dc resistance of the inductor is a key parameter for the efficiency. Lower dc resistance is available with a bigger winding area. A good tradeoff between the efficiency and the core size is letting the inductor copper loss equal to 2% of the output power.

INPUT CAPACITOR

A low ESR aluminum or tantalum capacitor is needed between the drain of the high-side MOSFET and ground to prevent large voltage transients from appearing at the input. The capacitor is selected based on the RMS current and voltage requirements. The RMS current is given by:

$$I_{RMS} = I_{OUT} \times \frac{\sqrt{V_{OUT}\,(V_{IN} - V_{OUT})}}{V_{IN}}$$

The RMS current reaches its maximum ($I_{OUT}/2$) when V_{IN} equals $2V_{OUT}$. A parallel of several capacitors may be required to meet the RMS current rating. For an aluminum capacitor, the voltage rating should be at least 25% higher than the maximum input voltage. If a tantalum capacitor is used, the voltage rating should be about twice the maximum input voltage. The tantalum capacitor should also be surge current tested by the manufacturer. It is also recommended to put a small ceramic capacitor (0.1 µF) between the V_{IN} pin and ground.

OUTPUT CAPACITOR

The selection of C_{OUT} is driven by the maximum allowable output voltage ripple. The output ripple in FPWM mode is approximated by:

$$V_{RIPPLE} = I_{RIPPLE} \left(ESR + \frac{1}{8F_S C_{OUT}} \right)$$

The ESR term plays the dominant role in determining the voltage ripple. Low ESR aluminum electrolytic or tantalum capacitors (such as Nichicon PL series, Sanyo OS-CON, Sprague 593D, 594D, and AVX TPS) are recommended. Electrolytic capacitors are not recommended for temperature below −25°C since their ESR rises dramatically at cold temperature. Tantalum capacitors have a much better ESR specification at cold temperatures and are preferred for low temperature applications.

POWER MOSFETS

Two N-channel logic-level MOSFETs are required for this application. MOSFETs with low on-resistance and total gate charge are recommended to achieve high efficiency. The drain-source breakdown voltage ratings are recommended to be 1.2 times the maximum input voltage.

SCHOTTKY DIODE D_1

The Schottky diode D_1 is used to prevent the intrinsic body diode of the low-side MOSFET Q_2 from conducting during the dead time when both MOSFETs are off. Since the forward voltage of D_1 is less than the body diode, efficiency can be improved. The breakdown voltage rating of D_1 is preferred to be 25% higher than the maximum input voltage. Since D_1 is only on for a short period of time (about 200 ns each cycle), the average current rating for D_1 only requires to be higher than 30% of the maximum output current. It is important to place D_1 very close to the drain and source of Q_2, extra parasitic inductance in the parallel loop will slow the turn-on of D_1 and direct the current through the body diode of Q_2.

R_1 AND R_2 (PROGRAMMING OUTPUT VOLTAGE)

Use the following formula to select the appropriate resistor values:

$$V_{OUT} = V_{REF}(1 + R_1/R_2)$$

where

- V_{REF} = 1.238V

Select a value for R_2 between 10kΩ and 100kΩ. (Use 1% or higher accuracy metal film resistors).

CURRENT SENSE RESISTOR

The value of the sense resistor is determined by the minimum current limit voltage and the maximum peak current. It can be calculated as follows:

$$R_3 = \frac{V_{CL\ (MIN)}}{\left(I_{MAX} + \frac{I_{RIPPLE}}{2}\right)(1 + TF)}$$

where

- TF is the tolerance factor of the sense resistor

PCB LAYOUT CONSIDERATIONS

Layout is critical to reduce noises and ensure specified performance. The important guidelines are listed as follows:

1. Minimize the parasitic inductance in the loop of input capacitors and MOSFETS: Q1, Q2 by using wide and short traces. This is important because the rapidly switching current, together with wiring inductance can generate large voltage spikes which can cause noise problems.
2. Always minimize the high-current ground traces: such as the traces from PGND pin to the source of Q2, then to the negative terminals of the output capacitors.
3. Use dedicated (Kelvin sense) and short traces from CSH, CSL pins to the sense resistor, R3. Keep these traces away from noise traces (such as SW trace, and gate traces).
4. Minimize the traces connecting Q2 and the Schottky diode. Any parasitic inductance in the loop can delay the turn-on of the Schottky diode, which diminishes the efficiency gain from adding D1.
5. Minimize the traces from drivers (HDRV pin and LDRV pin) to the MOSFETs gates.
6. Minimize the trace from the center of the output resistor divider to the FB pin and keep it away from noise sources to avoid noise pickup. A dedicated sense trace (separated from the power trace) can be used to connect the top of the resistor divider to the output. The sense trace ensures tight regulation at the output.

Application Circuits

A typical application circuit is shown in Figure 11, with some of the components values shown in Table 1.

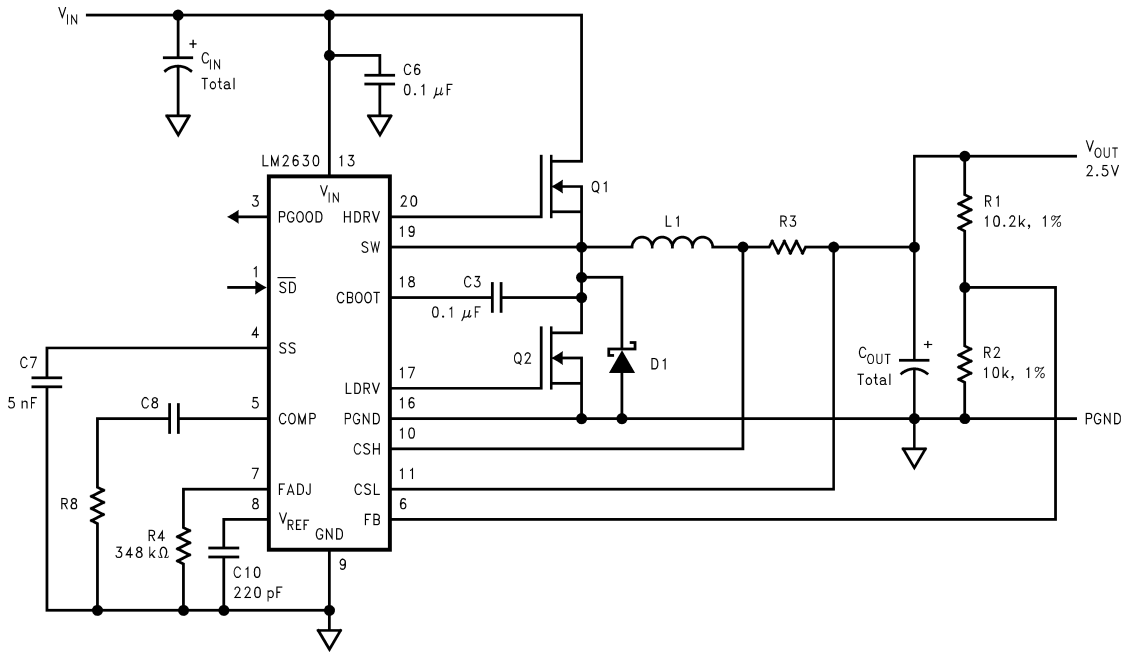
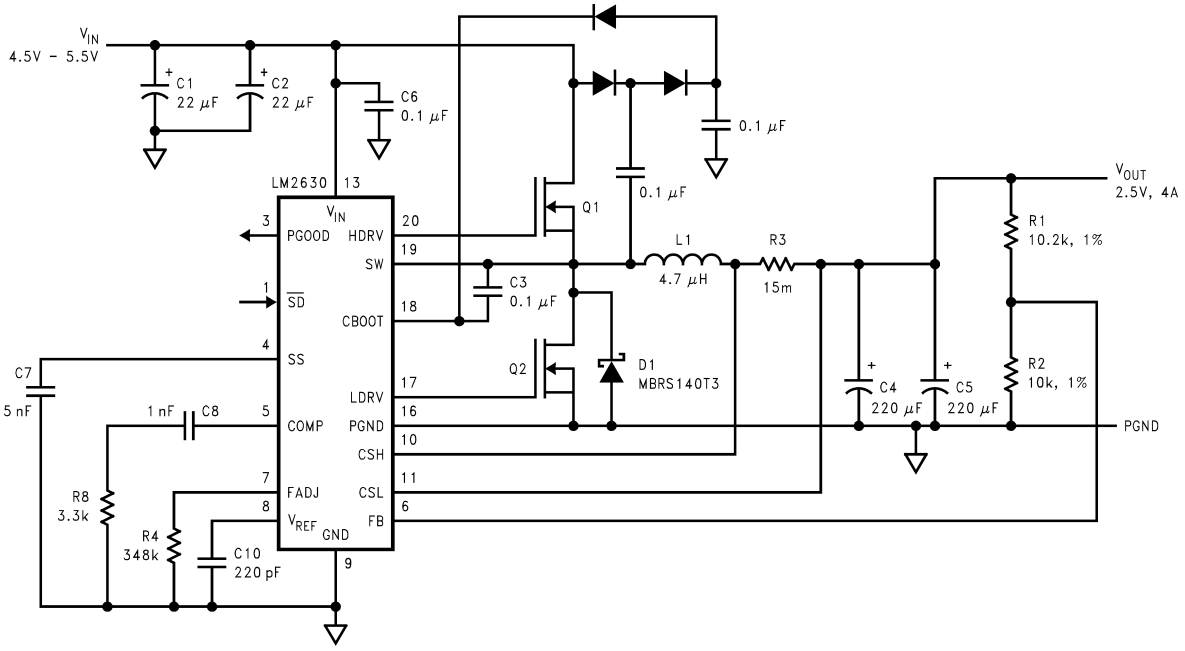


Figure 11. The Typical 2.5V Application Circuit

Table 1. Components for Typical 2.5V, 300kHz Application Circuits

Input Voltage	4.75V to 24V	4.5V to 6V
Output Current	4A	10A
Application	Notebook	Desktop
Q1 and Q2	Fairchild FDS6680; Siliconix Si4410DY; or International Rectifier IRF7805	Fairchild FDB7030L; or Motorola MTB75N03HDL
Inductor L1	Sumida CDRH127-7R6: 7.6µH, 5.9A	Pulse PE-53681: 2.5 µH, 11.4A
Input Capacitors	2 x 22µF, 35V Sprague 593D or TPS	2 x 220 µF, 10V Sanyo OS-CON SA
Output Capacitors	2 x 220µF, 10V Sprague 593D or TPS	3 x 330 µF, 6.3V Sanyo OS-CON SA
Rectifier D1	Motorola MBRS140T3	Motorola MBRS340T3
Sensing Resistor R3	15 mΩ IRC	3 x 20 mΩ IRC
Compensation components C8 and R8	R8 = 3.3 KΩ, C8 = 1 nF	R8 = 4 KΩ, C8 = 1nF

When the input voltage is low (less than 5V), the bootstrap function cannot deliver enough gate voltage to fully drive the high-side MOSFET on, which increases Rdson, and consequently reduces efficiency. An external charge-pump doubler can be added to double the CBOOT pin voltage (see Figure 12). It can also be added to the VIN pin to increase the gate drive voltage at both high-side and low-side MOSFETs.



Efficiency is 94% (typ) at 1A load.

Figure 12. High Efficiency, 300 kHz, 5V to 2.5V Converter

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