LM3208 650mA Miniature, Adjustable, Step-Down DC-DC Converter for RF Power Amplifiers

Check for Samples: LM3208

FEATURES

- **2 MHz (typ.) PWM Switching Frequency**
- **Operates from a Single Li-Ion Cell (2.7V to 5.5V)**
- **Adjustable Output Voltage (0.8V to 3.6V)**
- **Fast Output Voltage Transient (0.8V to 3.4V in 25µs typ.)**
- **650mA Maximum Load Capability**
- **High Efficiency (95% typ. at 3.9V_{IN}, 3.4V_{OUT} at 400mA)**
- **8-pin DSBGA Package**
- **Current Overload Protection**
- **Thermal Overload Protection**

APPLICATIONS

- **Cellular Phones**
- **Hand-Held Radios**
- **RF PC Cards**
- **Battery Powered RF Devices**

DESCRIPTION

The LM3208 is a DC-DC converter optimized for powering RF power amplifiers (PAs) from a single Lithium-Ion cell. However, it may be used in many other applications. It steps down an input voltage in the range from 2.7V to 5.5V to an adjustable output voltage of 0.8V to 3.6V. Output voltage is set by using a V_{CON} analog input to control power levels and efficiency of the RF PA.

The LM3208 offers superior performance for mobile phones and similar RF PA applications. Fixed-frequency PWM operation minimizes RF interference. A shutdown function turns the device off and reduces battery consumption to 0.01 µA (typ.).

The LM3208 is available in an 8-pin lead-free DSBGA package. A high switching frequency (2 MHz typ.) allows use of tiny surface-mount components. Only three small external surface-mount components, an inductor and two ceramic capacitors, are required.

TYPICAL APPLICATION

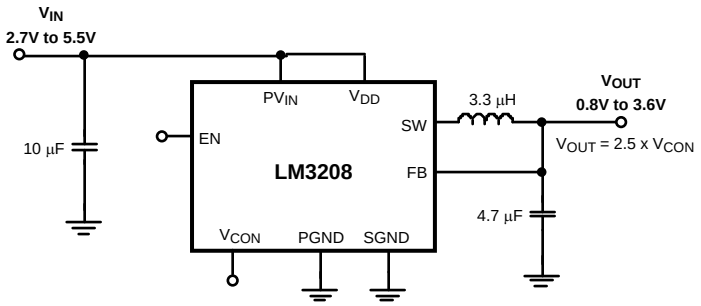
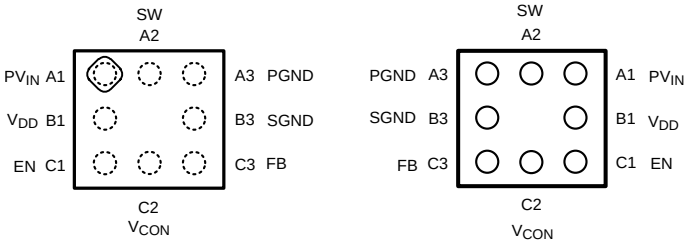


Figure 1. LM3208 Typical Application

CONNECTION DIAGRAMS



Top View **Bottom View**

Figure 2. 8-Bump Thin DSBGA Package, Large Bump
Package Number YZR0008GNA

PIN DESCRIPTIONS

Pin #	Name	Description
A1	PV_{IN}	Power Supply Voltage Input to the internal PFET switch.
B1	V_{DD}	Analog Supply Input.
C1	EN	Enable Input. Set this digital input high for normal operation. For shutdown, set this pin low.
C2	V_{CON}	Voltage Control Analog input. V_{CON} controls V_{OUT} in PWM mode.
C3	FB	Feedback Analog Input. Connect to the output at the output filter capacitor.
B3	SGND	Analog and Control Ground
A3	PGND	Power Ground
A2	SW	Switch node connection to the internal PFET switch and NFET synchronous rectifier. Connect to an inductor with a saturation current rating that exceeds the maximum Switch Peak Current Limit specification of the LM3208.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ABSOLUTE MAXIMUM RATINGS (1)(2)(3)

V_{DD}, PV_{IN} to SGND		−0.2V to +6.0V
PGND to SGND		−0.2V to +0.2V
EN, FB, V_{CON}		(SGND − 0.2V) to (V_{DD} + 0.2V) w/6.0V max
SW		(PGND − 0.2V) to (PV_{IN} + 0.2V) w/6.0V max
PV_{IN} to V_{DD}		−0.2V to +0.2V
Continuous Power Dissipation(4)		Internally Limited
Junction Temperature (T_{J-MAX})		+150°C
Storage Temperature Range		−65°C to +150°C
Maximum Lead Temperature (Soldering, 10 sec)		+260°C
ESD Rating(5)(6)	Human Body Model:	2kV
	Machine Model:	200V

(1) Absolute Maximum Ratings indicate limits beyond which damage to the component may occur. Operating Ratings are conditions under which operation of the device is ensured. Operating Ratings do not imply specified performance limits. For specified performance limits and associated test conditions, see the Electrical Characteristics tables.
(2) All voltages are with respect to the potential at the GND pins. The LM3208 is designed for mobile phone applications where turn-on after power-up is controlled by the system controller and where requirements for a small package size overrule increased die size for internal Under Voltage Lock-Out (UVLO) circuitry. Thus, it should be kept in shutdown by holding the EN pin low until the input voltage exceeds 2.7V.
(3) If Military/Aerospace specified devices are required, please contact the TI Sales Office/ Distributors for availability and specifications.
(4) Internal thermal shutdown circuitry protects the device from permanent damage. Thermal shutdown engages at T_J = 150°C (typ.) and disengages at T_J = 125°C (typ.).
(5) The Human body model is a 100pF capacitor discharged through a 1.5kΩ resistor into each pin. (MIL-STD-883 3015.7) The machine model is a 200pF capacitor discharged directly into each pin.
(6) TI recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper ESD handling procedures can result in damage.

OPERATING RATINGS(1)(2)

Input Voltage Range	2.7V to 5.5V
Recommended Load Current	0mA to 650mA
Junction Temperature (T_J) Range	−30°C to +125°C
Ambient Temperature (T_A) Range(3)	−30°C to +85°C

(1) Absolute Maximum Ratings indicate limits beyond which damage to the component may occur. Operating Ratings are conditions under which operation of the device is ensured. Operating Ratings do not imply specified performance limits. For specified performance limits and associated test conditions, see the Electrical Characteristics tables.
(2) All voltages are with respect to the potential at the GND pins. The LM3208 is designed for mobile phone applications where turn-on after power-up is controlled by the system controller and where requirements for a small package size overrule increased die size for internal Under Voltage Lock-Out (UVLO) circuitry. Thus, it should be kept in shutdown by holding the EN pin low until the input voltage exceeds 2.7V.
(3) In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be de-rated. Maximum ambient temperature (T_{A-MAX}) is dependent on the maximum operating junction temperature ($T_{J-MAX-OP}$ = 125°C), the maximum power dissipation of the device in the application (P_{D-MAX}), and the junction-to ambient thermal resistance of the part/package in the application (θ_{JA}), as given by the following equation: $T_{A-MAX} = T_{J-MAX-OP} – (\theta_{JA} \times P_{D-MAX})$.

THERMAL PROPERTIES

Junction-to-Ambient Thermal Resistance (θ_{JA}), YZR08 Package(1)	100°C/W

(1) Junction-to-ambient thermal resistance (θ_{JA}) is taken from thermal measurements, performed under the conditions and guidelines set forth in the JEDEC standard JESD51-7. A 4 layer, 4" x 4", 2/1/1/2 oz. Cu board as per JEDEC standards is used for the measurements.

ELECTRICAL CHARACTERISTICS[1][2][3]

Limits in standard typeface are for $T_A = T_J = 25°C$. Limits in **boldface** type apply over the full operating ambient temperature range ($-30°C \le T_A = T_J \le +85°C$). Unless otherwise noted, all specifications apply to the LM3208 with: $PV_{IN} = V_{DD} = EN = 3.6V$.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$V_{FB,\ MIN}$	Feedback Voltage at minimum setting	$V_{CON} = 0.32V$[3]	**0.75**	0.80	**0.85**	V
$V_{FB,\ MAX}$	Feedback Voltage at maximum setting	$V_{CON} = 1.44V$, $V_{IN} = 4.2V$[3]	**3.537**	3.600	**3.683**	V
I_{SHDN}	Shutdown supply current	EN = SW = V_{CON} = 0V,[4]		0.01	**2**	µA
I_Q	DC bias current into V_{DD}	V_{CON} = 0V, FB = 0V, No Switching[5]		0.6	**0.7**	mA
$R_{DSON(P)}$	Pin-pin resistance for Large PFET	I_{SW} = 200mA, V_{CON} = 0.5V		140	180 **210**	mΩ
$R_{DSON(P)}$	Pin-pin resistance for Small PFET	I_{SW} = 200mA, V_{CON} = 0.32V		960		mΩ
$R_{DSON(N)}$	Pin-pin resistance for NFET	I_{SW} = –200mA, V_{CON} = 0.5V		300	375 **450**	mΩ
I_{LIM} (L_PFET)	Large PFET (L) Switch peak current limit	$V_{CON} = 0.5V$[6]	**985**	1100	**1200**	mA
I_{LIM} (S_PFET)	Small PFET (S) Switch peak current limit	$V_{CON} = 0.32V$[7]	**650**	800	**900**	mA
F_{OSC}	Internal oscillator frequency		**1.8**	2.0	**2.2**	MHz
$V_{IH,EN}$	Logic high input threshold		**1.2**			V
$V_{IL,EN}$	Logic low input threshold				**0.5**	V
$I_{PIN,EN}$	EN pin pull down current			5	**10**	µA
$V_{CON,ON}$	V_{CON} Threshold for turning on switches			0.15		V
I_{CON}	V_{CON} pin leakage current	V_{CON} = 1.0V			**±1**	µA
Gain	V_{CON} to V_{OUT} Gain	$0.32V \le V_{CON} \le 1.44V$		2.5		V/V

(1) All voltages are with respect to the potential at the GND pins. The LM3208 is designed for mobile phone applications where turn-on after power-up is controlled by the system controller and where requirements for a small package size overrule increased die size for internal Under Voltage Lock-Out (UVLO) circuitry. Thus, it should be kept in shutdown by holding the EN pin low until the input voltage exceeds 2.7V.

(2) Min and Max limits are specified by design, test, or statistical analysis. Typical numbers are not specified, but do represent the most likely norm. Due to the pulsed nature of the testing $T_A = T_J$ for the electrical characteristics table.

(3) The parameters in the electrical characteristics table are tested under open loop conditions at $PV_{IN} = V_{DD} = 3.6V$ unless otherwise specified. For performance over the input voltage range and closed-loop results, refer to the datasheet curves.

(4) Shutdown current includes leakage current of PFET.

(5) I_Q specified here is when the part is not switching. For operating quiescent current at no load, refer to datasheet curves.

(6) Current limit is built-in, fixed, and not adjustable. Electrical Characteristic table reflects open loop data (FB = 0V and current drawn from SW pin ramped up until cycle by cycle limit is activated). Refer to SYSTEM CHARACTERISTICS table for maximum output current.

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SYSTEM CHARACTERISTICS

The following spec table entries are specified by design providing the component values in the typical application circuit are used (L = 3.0µH, DCR = 0.12Ω, FDK MIPW3226D3R0M; C_{IN} = 10µF, 6.3V, 0805, TDK C2012X5R0J106K; C_{OUT} = 4.7µF, 6.3V, 0603, TDK C1608X5R0J475M). **These parameters are not specified by production testing.** Min and Max values are specified over the ambient temperature range T_A = −30°C to 85°C. Typical values are specified at PV_{IN} = V_{DD} = EN = 3.6V and T_A = 25°C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$T_{RESPONSE}$	Time for V_{OUT} to rise from 0.8V to 3.4V (to reach 3.35V)	V_{IN} = 4.2V, R_{LOAD} = 5.5Ω		25	40	µs
	Time for V_{OUT} to fall from 3.4V to 0.8V	V_{IN} = 4.2V, R_{LOAD} = 15Ω		35	45	µs
C_{CON}	V_{CON} input capacitance	V_{CON} = 1V, V_{IN} = 2.7V to 5.5V, Test frequency = 100kHz		5	10	pF
C_{EN}	EN input capacitance	EN = 2V, V_{IN} = 2.7V to 5.5V, Test frequency = 100kHz		5	10	pF
V_{CON} (S>L)	$R_{DSON(P)}$ management threshold	Threshold for PFET $R_{DSON(P)}$ to change from 960mΩ to 140mΩ	0.39	0.42	0.45	V
V_{CON} (L>S)	$R_{DSON(P)}$ management threshold	Threshold for PFET $R_{DSON(P)}$ to change from 140mΩ to 960mΩ	0.37	0.40	0.43	V
$I_{OUT, MAX}$	Maximum Output Current	V_{IN} = 2.7V to 5.5V, V_{CON} = 0.45V to 1.44V, L = MIPW3226D3R0	650			mA
		V_{IN} = 2.7V to 5.5V, V_{CON} = 0.32V to 0.45V, L = MIPW3226D3R0	400			mA
Linearity	Linearity in control range 0.32V to 1.44V	V_{IN} = 3.9V (1) Monotonic in nature	–3		+3	%
			−50		+50	mV
T_{ON}	Turn on time (time for output to reach 97% of final value after Enable low to high transition)	EN = Low to High, V_{IN} = 4.2V, V_{OUT} = 3.4V, I_{OUT} ≤ 1mA		40	60	µs
η	Efficiency	V_{IN} = 3.6V, V_{OUT} = 0.8V, I_{OUT} = 90mA		81		%
		V_{IN} = 3.6V, V_{OUT} = 1.5V, I_{OUT} = 150mA		89		%
		V_{IN} = 3.9V, V_{OUT} = 3.4V, I_{OUT} = 400mA		95		%
V_{OUT}_ripple	Ripple voltage at no pulse skip condition	V_{IN} = 2.7V to 4.5V, V_{OUT} = 0.8V to 3.4V, Differential voltage = V_{IN} – V_{OUT} > 1V, I_{OUT} = 0mA to 400mA (2)		10		mVp-p
	Ripple voltage at pulse skip condition	V_{IN} = 5.5V to dropout, V_{OUT} = 3.4V, I_{OUT} = 650mA (2)		60		mVp-p
Line_tr	Line transient response	V_{IN} = 3.6V to 4.2V, T_R = T_F = 10µs, V_{OUT} = 0.8V, I_{OUT} = 100mA		50		mVpk
Load_tr	Load transient response	V_{IN} = 3.1 / 3.6 / 4.5V, V_{OUT} = 0.8V, I_{OUT} = 50mA to 150mA		50		mVpk
Max Duty cycle	Maximum duty cycle		100			%

(1) Linearity limits are ±3% or ±50mV whichever is larger.
(2) Ripple voltage should be measured at C_{OUT} electrode on a well-designed PC board and using the suggested inductor and capacitors.

TYPICAL PERFORMANCE CHARACTERISTICS

(Circuit in Figure 35, PV_{IN} = V_{DD} = EN = 3.6V and T_A = 25°C unless otherwise specified.).

Quiescent Current vs Supply Voltage (V_{CON} = 0V, FB = 0V, No Switching)

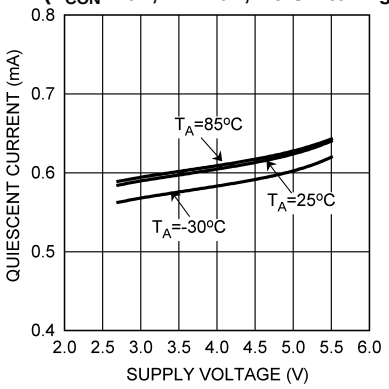


Figure 3.

Shutdown Current vs Temperature (V_{CON} = 0V, EN = 0V)

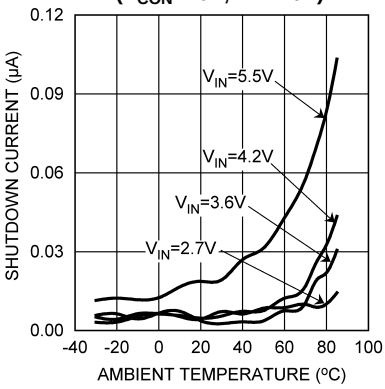


Figure 4.

Switching Frequency vs Temperature (V_{OUT} = 1.3V, I_{OUT} = 200mA)

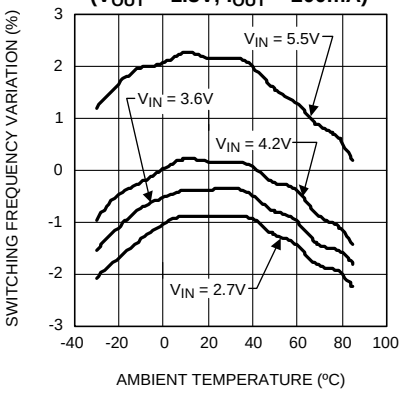


Figure 5.

Output Voltage vs Supply Voltage (V_{OUT} = 1.3V)

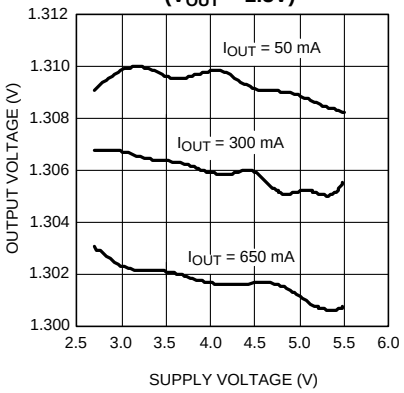


Figure 6.

Output Voltage vs Temperature (V_{IN} = 3.6V, V_{OUT} = 0.8V)

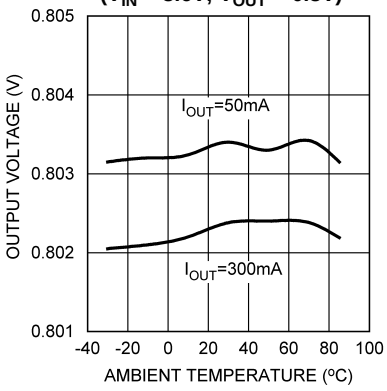


Figure 7.

Output Voltage vs Temperature (V_{IN} = 4.2V, V_{OUT} = 3.4V)

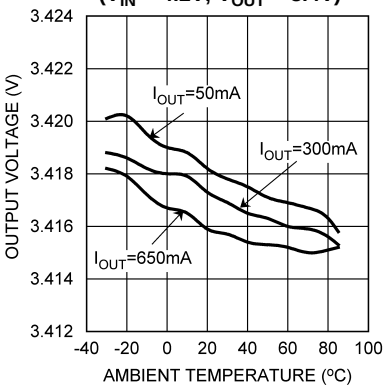


Figure 8.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

(Circuit in Figure 35, PV_{IN} = V_{DD} = EN = 3.6V and T_A = 25°C unless otherwise specified.).

Current Limit vs Temperature (Large PFET)

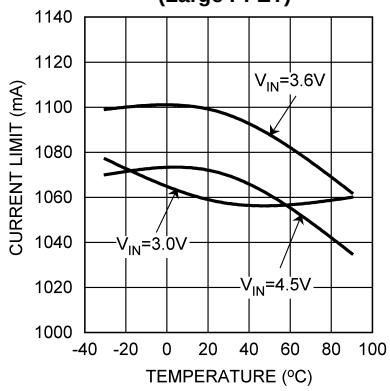


Figure 9.

Current Limit vs Temperature (Small PFET)

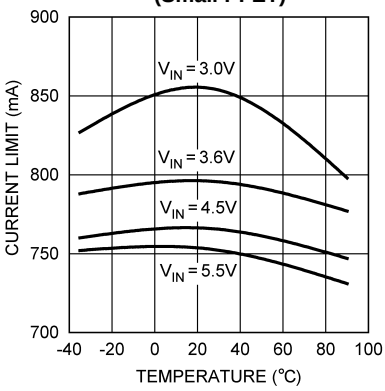


Figure 10.

V_{CON} Voltage vs Output Voltage (R_{LOAD} = 10 Ω)

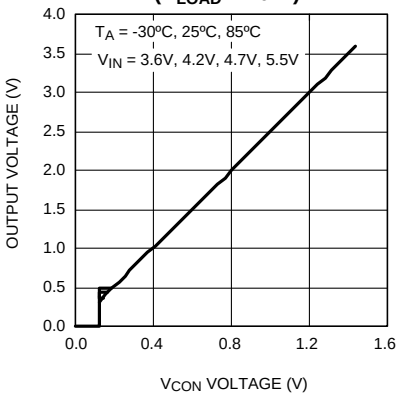


Figure 11.

V_{CON} Voltage vs Output Voltage (R_{LOAD} = 10 Ω)

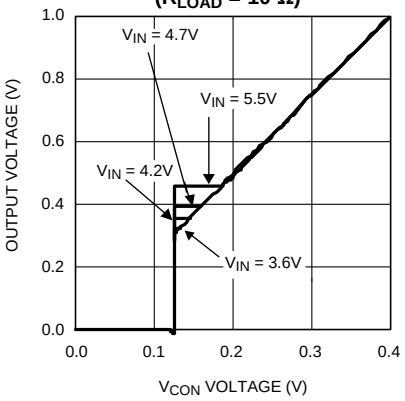


Figure 12.

Efficiency vs Output Voltage (V_{IN} = 3.9V)

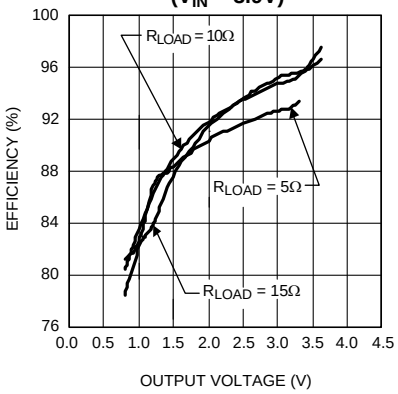


Figure 13.

EN High Threshold vs Supply Voltage

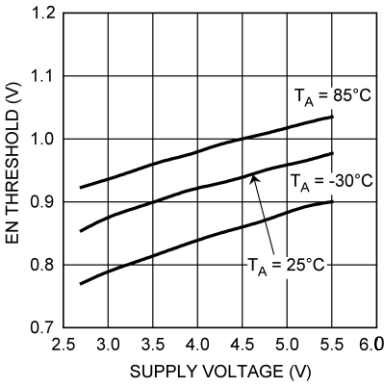


Figure 14.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

(Circuit in Figure 35, PV_{IN} = V_{DD} = EN = 3.6V and T_A = 25°C unless otherwise specified.).

Efficiency vs Output Current (V_{OUT} = 0.8V)

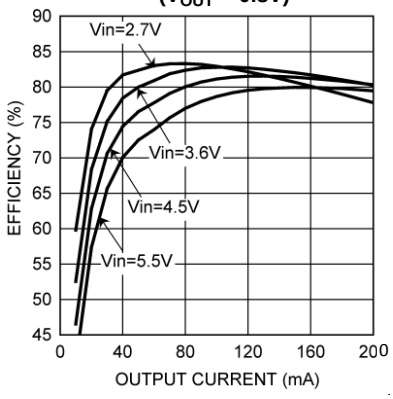


Figure 15.

Efficiency vs Output Current (V_{OUT} = 3.6V)

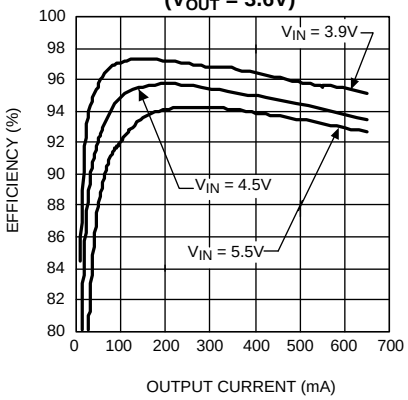
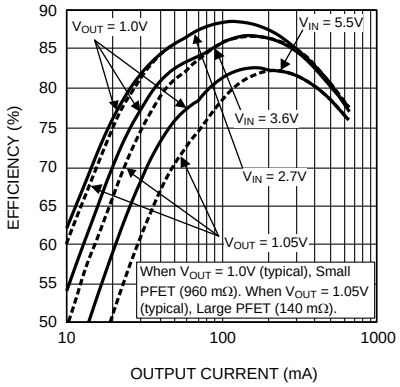


Figure 16.

Efficiency vs Output Current (R_{DSON} Management)



Dark curves are efficiency profiles of either large PFET or small PFET whichever is higher.

Figure 17.

Efficiency vs Output Current (R_{DSON} Management, V_{IN}=4.5V)

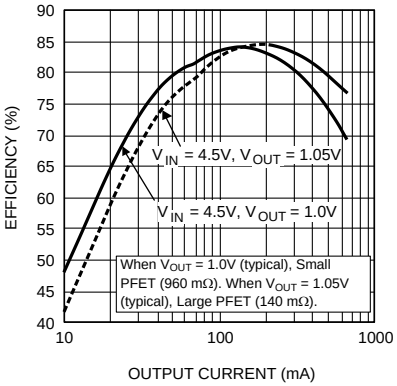


Figure 18.

R_{DSON} vs Temperature (Large PFET, I_{SW} = 200mA)

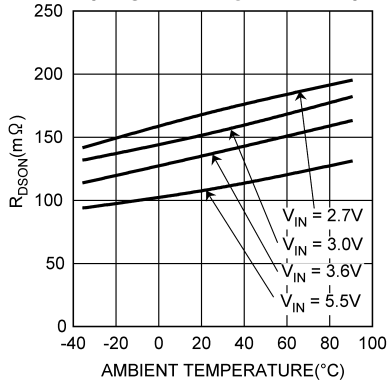


Figure 19.

R_{DSON} vs Temperature (Small PFET, I_{SW} = 200mA)

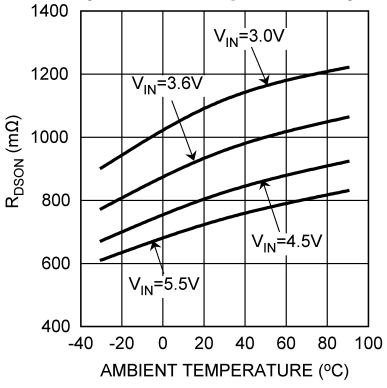


Figure 20.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

(Circuit in Figure 35, $PV_{IN} = V_{DD} = EN = 3.6V$ and $T_A = 25°C$ unless otherwise specified.).

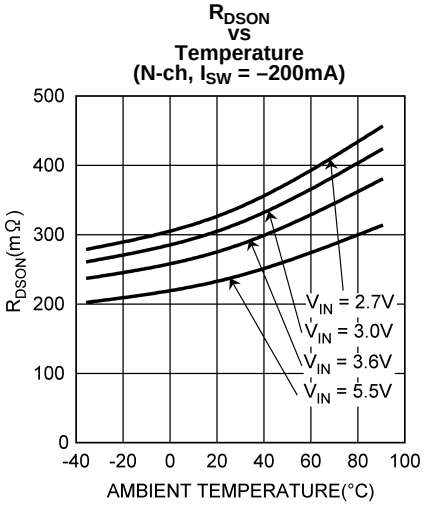


Figure 21.

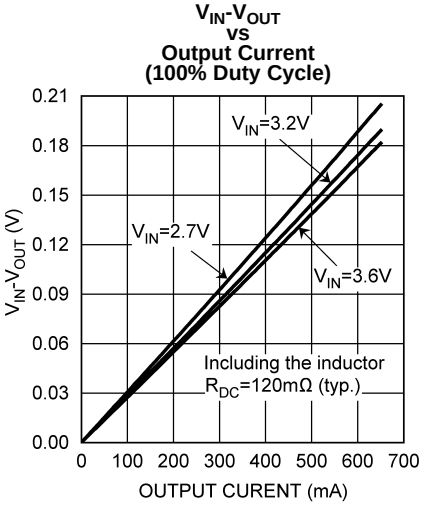


Figure 22.

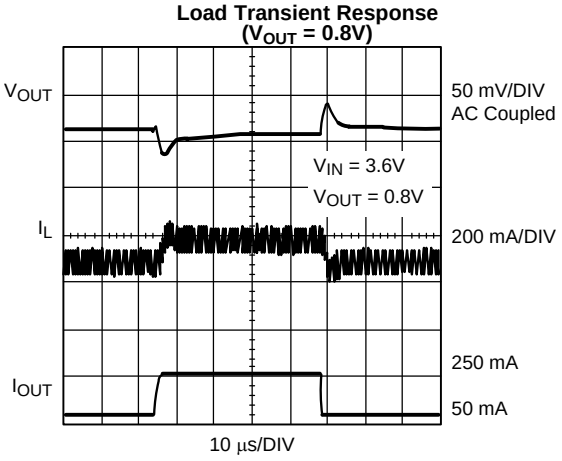


Figure 23.

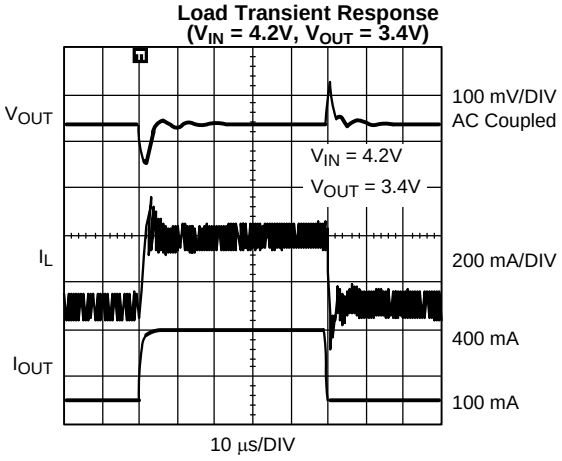


Figure 24.

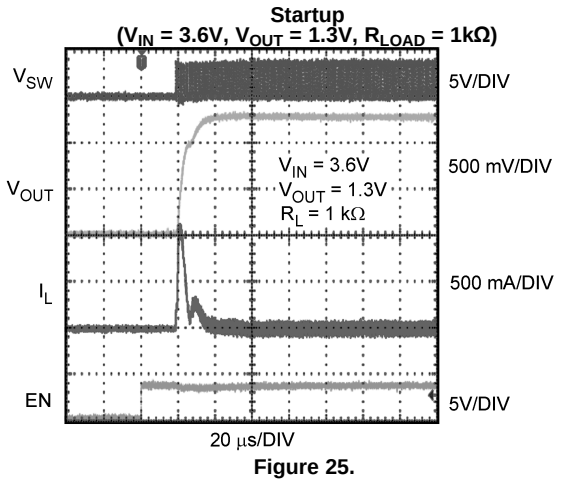


Figure 25.

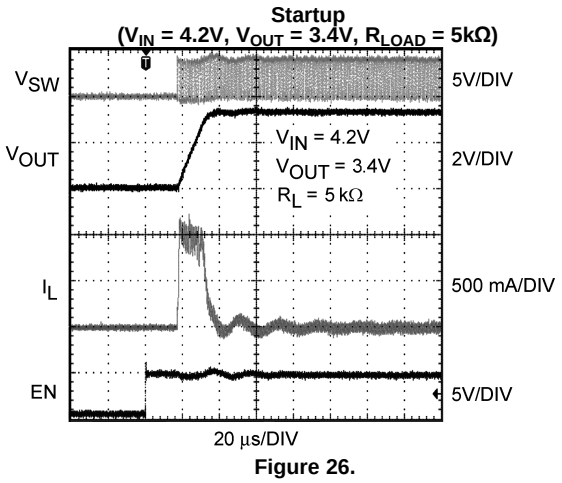


Figure 26.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

(Circuit in Figure 35, $PV_{IN} = V_{DD} = EN = 3.6V$ and $T_A = 25°C$ unless otherwise specified.).

Shutdown Response
(V_{IN} = 4.2V, V_{OUT} = 3.4V, R_{LOAD} = 10Ω)

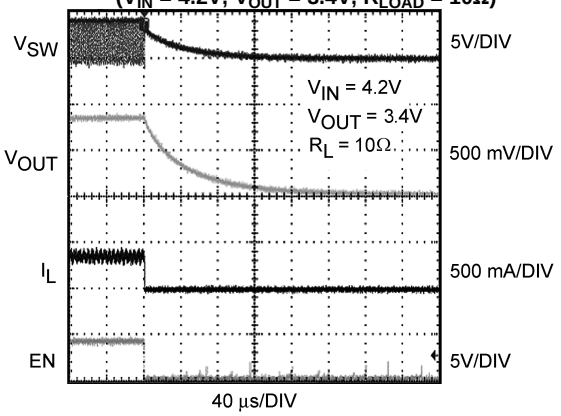


Figure 27.

Line Transient Reponse
(V_{IN} = 3.0V to 3.6V, I_{OUT} = 100mA)

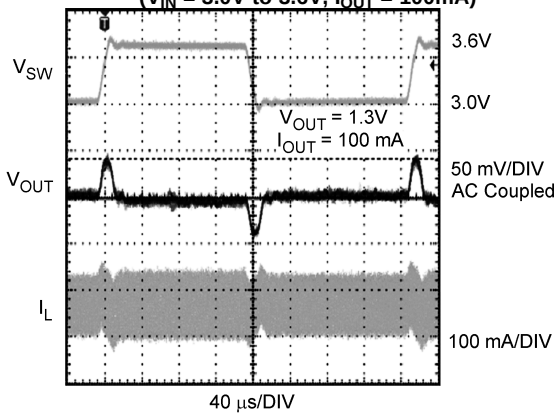


Figure 28.

V_{CON} Transient Response
(V_{IN} = 4.2V, V_{CON} = 0.32V/1.44V, R_{LOAD} = 10Ω)

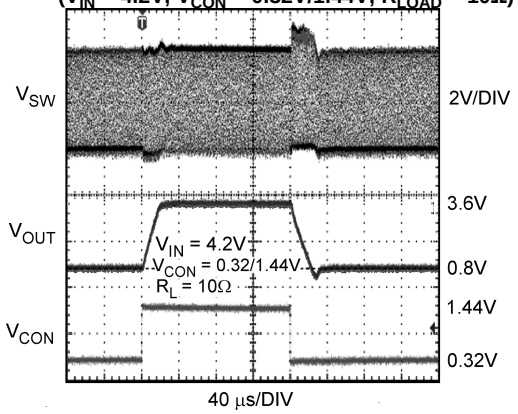


Figure 29.

Timed Current Limit Response
(V_{IN} = 3.6V)

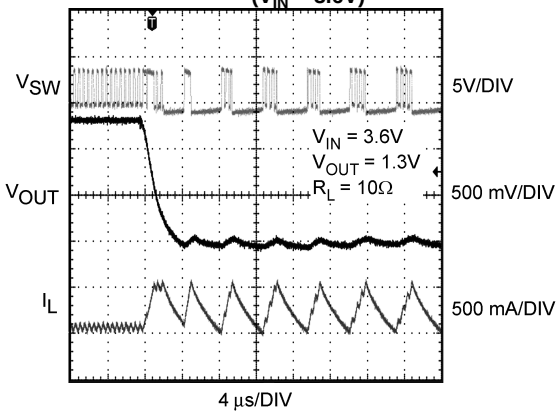


Figure 30.

Output Voltage Ripple
(V_{OUT} = 1.3V)

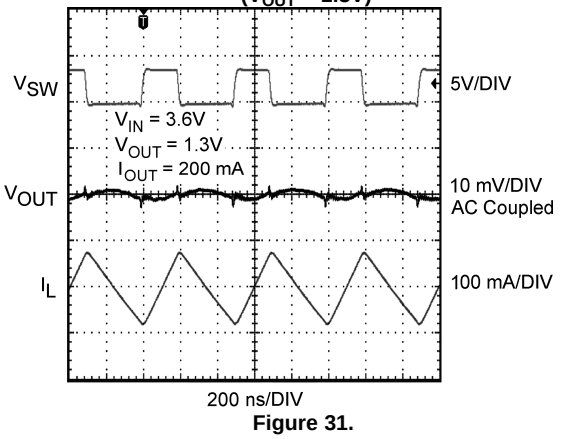


Figure 31.

Output Voltage Ripple
(V_{OUT} = 3.4V)

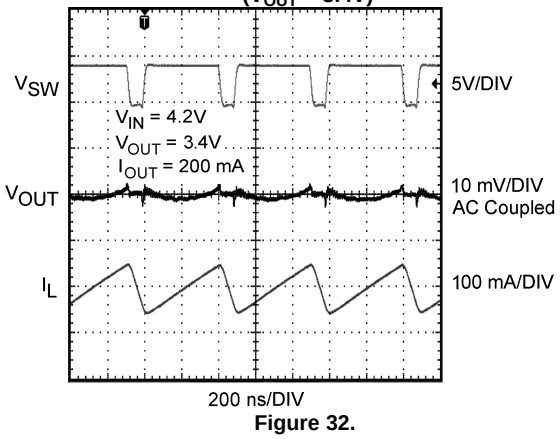


Figure 32.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

(Circuit in Figure 35, $PV_{IN} = V_{DD} = EN = 3.6V$ and $T_A = 25°C$ unless otherwise specified.).

Output Voltage Ripple in Pulse Skip
(V_{IN} = 3.96V, V_{OUT} = 3.4V, R_{LOAD} = 5Ω)

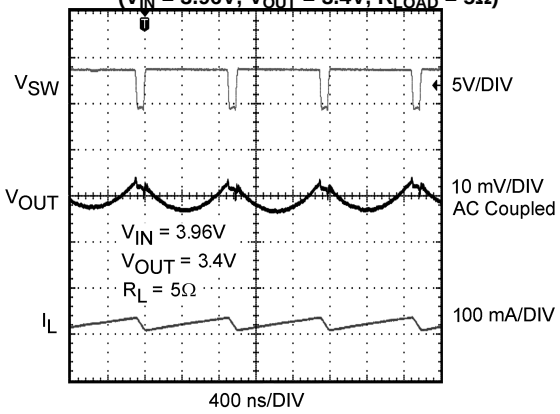


Figure 33.

BLOCK DIAGRAM

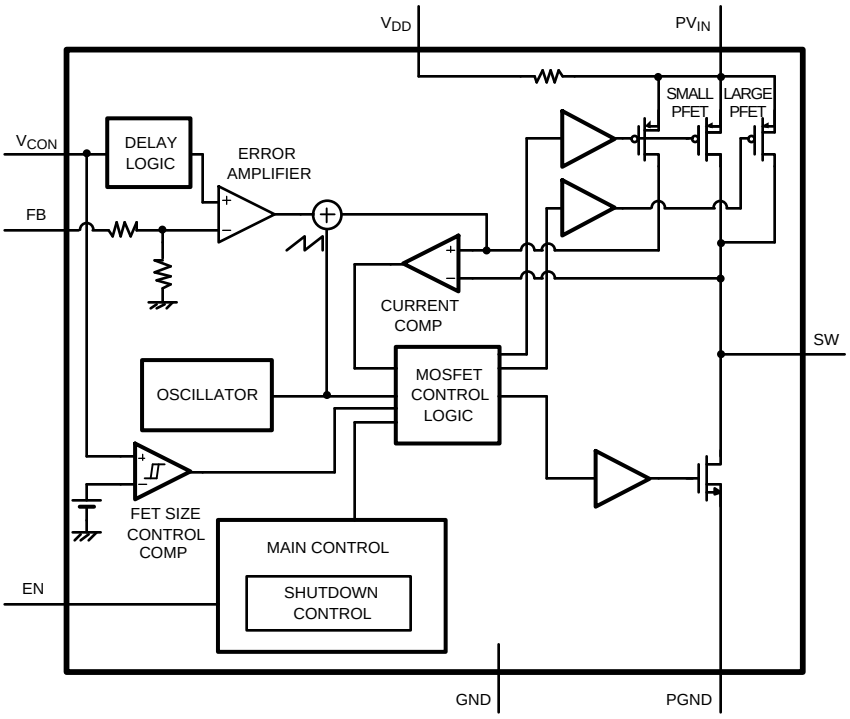


Figure 34. Functional Block Diagram

OPERATION DESCRIPTION

The LM3208 is a simple, step-down DC-DC converter optimized for powering RF power amplifiers (PAs) in mobile phones, portable communicators, and similar battery powered RF devices. It is designed to allow the RF PA to operate at maximum efficiency over a wide range of power levels from a single Li-Ion battery cell. It is based on a current-mode buck architecture, with synchronous rectification for high efficiency. It is designed for a maximum load capability of 650mA when V_{OUT} > 1.05V (typ.) and 400mA when V_{OUT} < 1.00V (typ.) in PWM mode.

Maximum load range may vary from this depending on input voltage, output voltage and the inductor chosen.

Efficiency is typically around 95% for a 400mA load with 3.4V output, 3.9V input. The LM3208 has an R_{DSON} management scheme to increase efficiency when V_{OUT} ≤ 1V. The output voltage is dynamically programmable from 0.8V to 3.6V by adjusting the voltage on the control pin without the need for external feedback resistors. This prolongs battery life by changing the PA supply voltage dynamically depending on its transmitting power.

Additional features include current overload protection and thermal overload shutdown.

The LM3208 is constructed using a chip-scale 8-pin DSBGA package. This package offers the smallest possible size, for space-critical applications such as cell phones, where board area is an important design consideration. Use of a high switching frequency (2MHz, typ.) reduces the size of external components. As shown in Figure 1, only three external power components are required for implementation. Use of a DSBGA package requires special design considerations for implementation. (See DSBGA Package Assembly and Use in the Application Information section.) Its fine bump-pitch requires careful board design and precision assembly equipment. Use of this package is best suited for opaque-case applications, where its edges are not subject to high-intensity ambient red or infrared light. In addition, the system controller should set EN low during power-up and other low supply voltage conditions. (See Shutdown Mode in the Device Information section.)

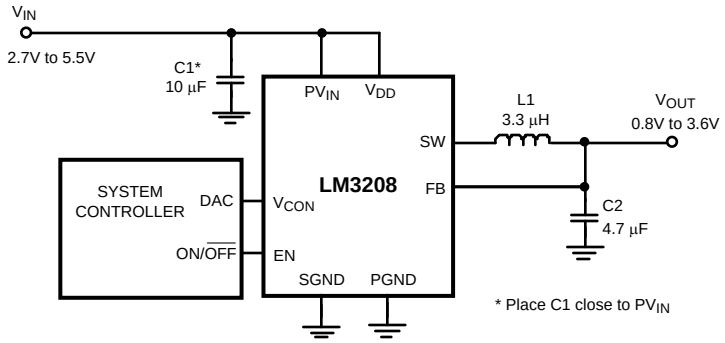


Figure 35. Typical Operating System Circuit

Circuit Operation

Referring to Figure 1 and Figure 34, the LM3208 operates as follows. During the first part of each switching cycle, the control block in the LM3208 turns on the internal PFET (P-channel MOSFET) switch. This allows current to flow from the input through the inductor to the output filter capacitor and load. The inductor limits the current to a ramp with a slope of around (V_{IN} – V_{OUT}) / L, by storing energy in a magnetic field. During the second part of each cycle, the controller turns the PFET switch off, blocking current flow from the input, and then turns the NFET (N-channel MOSFET) synchronous rectifier on. In response, the inductor's magnetic field collapses, generating a voltage that forces current from ground through the synchronous rectifier to the output filter capacitor and load. As the stored energy is transferred back into the circuit and depleted, the inductor current ramps down with a slope around V_{OUT} / L. The output filter capacitor stores charge when the inductor current is high, and releases it when low, smoothing the voltage across the load.

The output voltage is regulated by modulating the PFET switch on time to control the average current sent to the load. The effect is identical to sending a duty-cycle modulated rectangular wave formed by the switch and synchronous rectifier at SW to a low-pass filter formed by the inductor and output filter capacitor. The output voltage is equal to the average voltage at the SW pin.

While in operation, the output voltage is regulated by switching at a constant frequency and then modulating the energy per cycle to control power to the load. Energy per cycle is set by modulating the PFET switch on-time pulse width to control the peak inductor current. This is done by comparing the signal from the current-sense amplifier with a slope compensated error signal from the voltage-feedback error amplifier. At the beginning of each cycle, the clock turns on the PFET switch, causing the inductor current to ramp up. When the current sense signal ramps past the error amplifier signal, the PWM comparator turns off the PFET switch and turns on the NFET synchronous rectifier, ending the first part of the cycle. If an increase in load pulls the output down, the error amplifier output increases, which allows the inductor current to ramp higher before the comparator turns off the PFET. This increases the average current sent to the output and adjusts for the increase in the load.

Before appearing at the PWM comparator, a slope compensation ramp from the oscillator is subtracted from the error signal for stability of the current feedback loop. The minimum on time of PFET is 55ns (typ.)

Shutdown Mode

Setting the EN digital pin low (<0.5V) places the LM3208 in shutdown mode (0.01µA typ.). During shutdown, the PFET switch, NFET synchronous rectifier, reference voltage source, control and bias circuitry of the LM3208 are turned off. Setting EN high (>1.2V) enables normal operation.

EN should be set low to turn off the LM3208 during power-up and under voltage conditions when the power supply is less than the 2.7V minimum operating voltage. The LM3208 is designed for compact portable applications, such as mobile phones. In such applications, the system controller determines power supply sequencing and requirements for small package size outweigh the additional size required for inclusion of UVLO (Under Voltage Lock-Out) circuitry.

Internal Synchronous Rectification

While in PWM mode, the LM3208 uses an internal NFET as a synchronous rectifier to reduce rectifier forward voltage drop and associated power loss. Synchronous rectification provides a significant improvement in efficiency whenever the output voltage is relatively low compared to the voltage drop across an ordinary rectifier diode.

The internal NFET synchronous rectifier is turned on during the inductor current down slope in the second part of each cycle. The synchronous rectifier is turned off prior to the next cycle. The NFET is designed to conduct through its intrinsic body diode during transient intervals before it turns on, eliminating the need for an external diode.

$R_{DSON(P)}$ Management

The LM3208 has a unique $R_{DSON(P)}$ management function to improve efficiency in the low output current region up to 100mA. When the V_{CON} voltage is less than 0.40V (typ.), the device uses only a small part of the PFET to minimize drive loss of the PFET. When V_{CON} is greater than 0.42V (typ.), the entire PFET is used to minimize $R_{DSON(P)}$ loss. This threshold has about 20mV (typ.) of hysteresis.

$V_{CON,ON}$

The output is disabled when V_{CON} is below 125mV (typ.). It is enabled when V_{CON} is above 150mV (typ.). The threshold has about 25mV (typ.) of hysteresis.

Current Limiting

A current limit feature allows the LM3208 to protect itself and external components during overload conditions. In PWM mode, an 1100mA (typ.) cycle-by-cycle current limit is normally used when V_{CON} is above 0.42V (typ.), and an 800mA (typ.) is used when V_{CON} is below 0.40V (typ.). If an excessive load pulls the output voltage down to approximately 0.375V, then the device switches to a timed current limit mode when V_{CON} is above 0.42V (typ.). In timed current limit mode the internal PFET switch is turned off after the current comparator trips and the beginning of the next cycle is inhibited for 3.5µs to force the instantaneous inductor current to ramp down to a safe value. The synchronous rectifier is off in timed current limit mode. Timed current limit prevents the loss of current control seen in some products when the output voltage is pulled low in serious overload conditions.

Dynamically Adjustable Output Voltage

The LM3208 features dynamically adjustable output voltage to eliminate the need for external feedback resistors. The output can be set from 0.8V to 3.6V by changing the voltage on the analog V_{CON} pin. This feature is useful in PA applications where peak power is needed only when the handset is far away from the base station or when data is being transmitted. In other instances, the transmitting power can be reduced. Hence the supply voltage to the PA can be reduced, promoting longer battery life. See Setting The Output Voltage in the Application Information section for further details. The LM3208 moves into Pulse Skipping mode when duty cycle is over 92% and the output voltage ripple increases slightly.

Thermal Overload Protection

The LM3208 has a thermal overload protection function that operates to protect itself from short-term misuse and overload conditions. When the junction temperature exceeds around 150°C, the device inhibits operation. Both the PFET and the NFET are turned off in PWM mode. When the temperature drops below 125°C, normal operation resumes. Prolonged operation in thermal overload conditions may damage the device and is considered bad practice.

APPLICATION INFORMATION

Setting The Output Voltage

The LM3208 features a pin-controlled variable output voltage to eliminate the need for external feedback resistors. It can be programmed for an output voltage from 0.8V to 3.6V by setting the voltage on the V_{CON} pin, as in the following formula:

$$V_{OUT} = 2.5 \times V_{CON} \quad (1)$$

When V_{CON} is between 0.32V and 1.44V, the output voltage will follow proportionally by 2.5 times of V_{CON}.

If V_{CON} is over 1.44V (V_{OUT} = 3.6V), sub-harmonic oscillation may occur because of insufficient slope compensation. If V_{CON} voltage is less than 0.32V (V_{OUT} = 0.8V), the output voltage may not be regulated due to the required on-time being less than the minimum on-time (55ns). The output voltage can go lower than 0.8V providing a limited V_{IN} range is used. Refer to datasheet curve (V_{CON} Voltage vs Output Voltage) for details. This curve is for a typical part and there could be part-to-part variation for output voltages less than 0.8V over the limited V_{IN} range. When the control pin voltage is more than 0.15V (typ.), the switches are turned on. When it is less than 0.125V (typ.), the switches are turned off. This on/off function has 25mV (typ.) hysteresis. The quiescent current when (V_{CON} = 0V and V_{EN} = Hi) is around 600µA.

Estimation of Maximum Output Current Capability

Referring to Figure 35, the Inductor peak to peak ripple current can be estimated by:

$$I_{IND\_PP} = (V_{IN} - V_{OUT}) \times V_{OUT} / (L1 \times F_{SW} \times V_{IN}) \quad (2)$$

Where, Fsw is switching frequency.

Therefore, maximum output current can be calculated by:

$$I_{OUT\_MAX} = I_{LIM} - 0.5 \times I_{IND\_PP} \quad (3)$$

For the worst case calculation, the following parameters should be used:

F_{SW} (Lowest switching frequency): 1.8MHz

I_{LIM} (Lowest current limit value): 985mA

L1 (Lowest inductor value): refer to inductor data-sheet. Note that inductance will drop with DC bias current and temperature. The worst case is typically at 85°C.

For example, V_{IN} = 4.2V, V_{OUT} = 3.2V, L1 = 2.0µH (Inductance value at 985mA DC bias current and 85°C), F_{SW} = 1.8MHz , I_{LIM} = 985mA.

$$I_{IND\_PP} = 212mA \quad (4)$$

$$I_{OUT\_MAX} = 985 - 106 = 876mA \quad (5)$$

The effects of switch, inductor resistance and dead time are ignored. In real application, the ripple current would be 10% to 15% higher than ideal case. This should be taken into account when calculating maximum output current. Special attention needs to be paid that a delta between maximum output current capability and the current limit is necessary to satisfy transient response requirements. In practice, transient response requirements may not be met for output current greater than 650mA.

Inductor Selection

A 3.3µH inductor with saturation current rating over 1200mA and low inductance drop at the full DC bias condition is recommended for almost all applications. The inductor's DC resistance should be less than 0.2Ω for good efficiency. For low dropout voltage, lower DCR inductors are recommended. The lower limit of acceptable inductance is 1.7µH at 1200mA over the operating temperature range. Full attention should be paid to this limit, because some small inductors show large inductance drops at high DC bias. These cannot be used with the LM3208. FDK MIPW3226D3R0M is an example of an inductor with the lowest acceptable limit (as of Oct./05). Table 1 suggests some inductors and suppliers.

Table 1. Suggested Inductors And Their Suppliers

Model	Size (WxLxH) [mm]	Vendor
MIPW3226D3R0M	3.2 x 2.6 x 1.0	FDK
1098AS-3R3M	3.0 x 2.8 x 1.2	TOKO
NR3015T3R3M	3.0 x 3.0 x 1.5	Taiyo-Yuden
1098AS-2R7M	3.0 x 2.8 x 1.2	TOKO

If a smaller inductance inductor is used in the application, the LM3208 may become unstable during line and load transients, and V_{CON} transient response times may be affected.

For low-cost applications, an unshielded bobbin inductor is suggested. For noise-critical applications, a toroidal or shielded-bobbin inductor should be used. A good practice is to lay out the board with footprints accommodating both types for design flexibility. This allows substitution of a low-noise toroidal inductor, in the event that noise from low-cost bobbin models is unacceptable. Saturation occurs when the magnetic flux density from current through the windings of the inductor exceeds what the inductor's core material can support with a corresponding magnetic field. This can cause poor efficiency, regulation errors or stress to a DC-DC converter like the LM3208.

Capacitor Selection

The LM3208 is designed for use with ceramic capacitors for its input and output filters. Use a 10µF ceramic capacitor for input and a 4.7µF ceramic capacitor for output. They should maintain at least 50% capacitance at DC bias and temperature conditions. Ceramic capacitor types such as X5R, X7R and B are recommended for both filters. Table 2 lists some suggested part numbers and suppliers. DC bias characteristics of the capacitors must be considered when selecting the voltage rating and case size of the capacitor. If it is necessary to choose a 0603-size capacitor for C_{IN} and C_{OUT}, the operation of the LM3208 should be carefully evaluated on the system board. Use of multiple 2.2µF or 1µF capacitors in parallel may also be considered.

Table 2. Suggested Capacitors And Their Suppliers

Model	Vendor
C2012X5R0J106M,10µF, 6.3V	TDK
C1608X5R0J475M, 4.7µF, 6.3V	TDK
0805ZD475KA 4.7µF, 10V	AVX

The input filter capacitor supplies AC current drawn by the PFET switch of the LM3208 in the first part of each cycle and reduces the voltage ripple imposed on the input power source. The output filter capacitor absorbs the AC inductor current, helps maintain a steady output voltage during transient load changes and reduces output voltage ripple. These capacitors must be selected with sufficient capacitance and sufficiently low ESR (Equivalent Series Resistance) to perform these functions. The ESR of the filter capacitors is generally a major factor in voltage ripple.

EN Pin Control

Drive the EN pin using the system controller to turn the LM3208 ON and OFF. Use a comparator, Schmidt trigger or logic gate to drive the EN pin. Set EN high (>1.2V) for normal operation and low (<0.5V) for a 0.01µA (typ.) shutdown mode.

Set EN low to turn off the LM3208 during power-up and under voltage conditions when the power supply is less than the 2.7V minimum operating voltage. The part is out of regulation when the input voltage is less than 2.7V. The LM3208 is designed for mobile phones where the system controller controls operation mode for maximizing battery life and requirements for small package size outweigh the additional size required for inclusion of UVLO (Under Voltage Lock-Out) circuitry.

DSBGA Package Assembly and Use

Use of the DSBGA package requires specialized board layout, precision mounting and careful re-flow techniques, as detailed in TI Application Note 1112 (SNVA009). Refer to the section *Surface Mount Technology (SMD) Assembly Considerations.* For best results in assembly, alignment ordinals on the PC board should be used to facilitate placement of the device. The pad style used with DSBGA package must be the NSMD (non-solder mask defined) type. This means that the solder-mask opening is larger than the pad size. This prevents a lip that otherwise forms if the solder-mask and pad overlap, from holding the device off the surface of the board and interfering with mounting. See Application Note 1112 (SNVA009) for specific instructions how to do this.

The 8-Bump package used for LM3208 has 300micron solder balls and requires 10.82mil pads for mounting on the circuit board. The trace to each pad should enter the pad with a 90°entry angle to prevent debris from being caught in deep corners. Initially, the trace to each pad should be 7mil wide, for a section approximately 7mil long, as a thermal relief. Then each trace should neck up or down to its optimal width. The important criterion is symmetry. This ensures the solder bumps on the LM3208 re-flow evenly and that the device solders level to the board. In particular, special attention must be paid to the pads for bumps A1 and A3. Because PGND and PV_{IN} are typically connected to large copper planes, inadequate thermal relief's can result in late or inadequate re-flow of these bumps.

The DSBGA package is optimized for the smallest possible size in applications with red or infrared opaque cases. Because the DSBGA package lacks the plastic encapsulation characteristic of larger devices, it is vulnerable to light. Backside metallization and/or epoxy coating, along with front-side shading by the printed circuit board, reduce this sensitivity. However, the package has exposed die edges. In particular, DSBGA devices are sensitive to light (in the red and infrared range) shining on the package's exposed die edges.

Board Layout Considerations

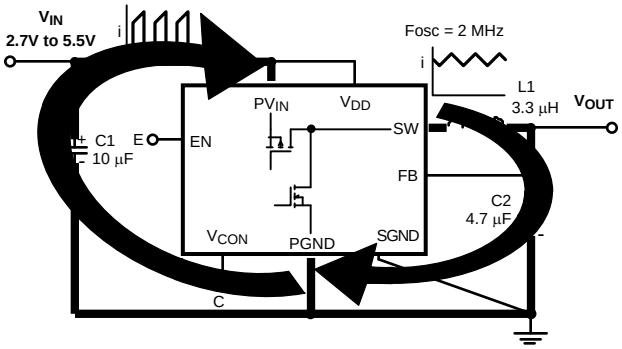


Figure 36. Current Loop

The LM3208 converts higher input voltage to lower output voltage with high efficiency. This is achieved with an inductor-based switching topology. During the first half of the switching cycle, the internal PMOS switch turns on, the input voltage is applied to the inductor, and the current flows from PV_{IN} line into the output capacitor and the load through the inductor. During the second half cycle, the PMOS turns off and the internal NMOS turns on. The inductor current continues to flow via the inductor from the device PGND line into the output capacitor and the load.

Referring to Figure 36, a pulse current flows in the left hand side loop, and a ripple current flows in the right hand side loop. Board layout and circuit pattern design of these two loops are the key factors for reducing noise radiation and stable operation. In other lines, such as from battery to C1 and C2 to the load, the current is mostly DC current. Therefore, it is not necessary to take so much care. Only pattern width (current capability) and DCR drop considerations are needed.

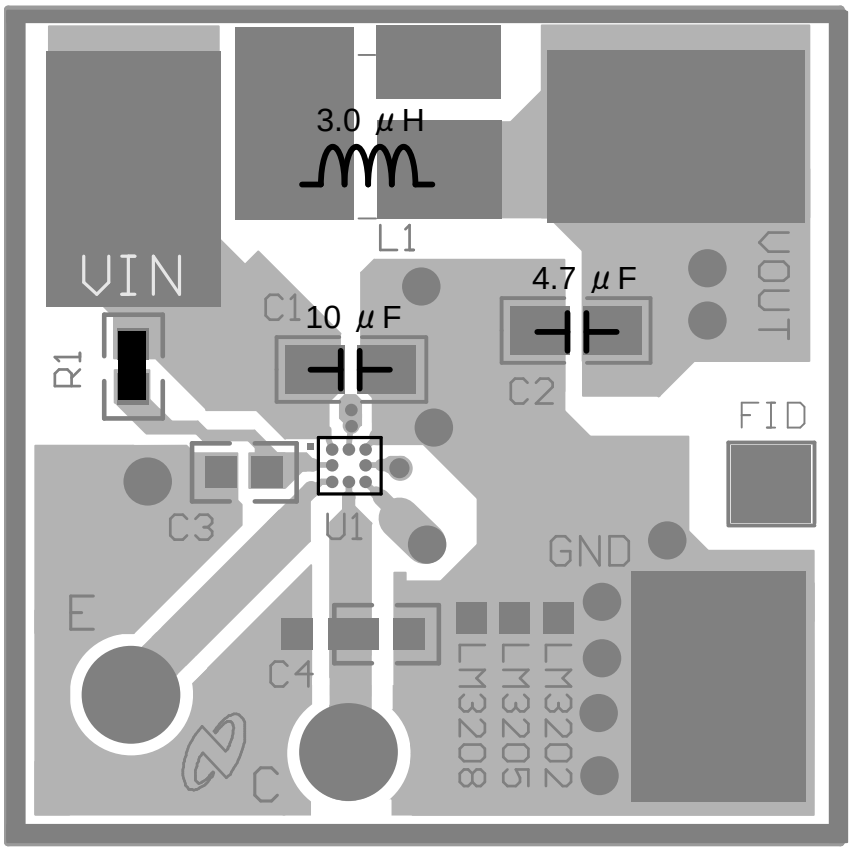


Figure 37. Evaluation Board Layout

Board Layout Flow

1. Minimize C1, PV_{IN}, and PGND loop. These traces should be as wide and short as possible. This is the highest priority.
2. Minimize L1, C2, SW and PGND loop. These traces also should be wide and short. This is the second priority.
3. The above layout patterns should be placed on the component side of the PCB to minimize parasitic inductance and resistance due to via-holes. It may be a good idea that the SW to L1 path is routed between C1(+) and C1(–) land patterns. If vias are used in these large current paths, multiple via-holes should be used if possible.
4. Connect C1(–), C2(–) and PGND with wide GND pattern. This pattern should be short, so C1(–), C2(–), and PGND should be as close as possible. Then connect to a PCB common GND pattern with as many via-holes as possible.
5. SGND should not connect directly to PGND. Connecting these pins under the device should be avoided. (If possible, connect SGND to the common port of C1(–), C2(–) and PGND.)
6. V_{DD} should not be connected directly to PV_{IN}. Connecting these pins under the device should be avoided. It is good idea to connect V_{DD} to C1(+) to avoid switching noise injection to the V_{DD} line.
7. The FB line should be protected from noise. It is a good idea to use an inner GND layer (if available) as a shield.

NOTE

The evaluation board shown in Figure 37 for the LM3208 was designed with these considerations, and it shows good performance. However some aspects have not been optimized because of limitations due to evaluation-specific requirements. The board can be used as a reference. Please refer questions to a TI representative.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
LM3208TL/NOPB	ACTIVE	DSBGA	YZR	8	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-30 to 85	S 33	Samples
LM3208TLX/NOPB	ACTIVE	DSBGA	YZR	8	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-30 to 85	S 33	Samples

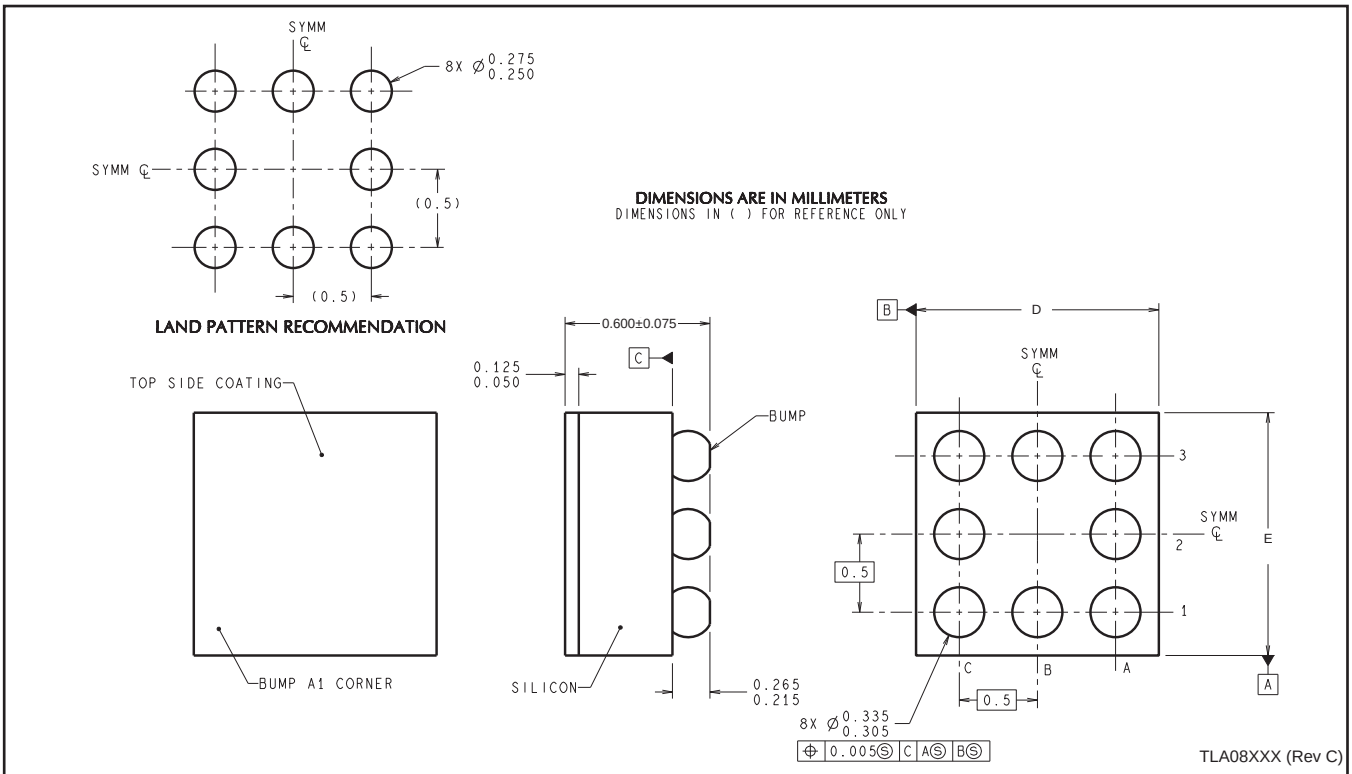
(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Only one of markings shown within the brackets will appear on the physical device.

YZR0008



D: Max = 1.882 mm, Min =1.782 mm

E: Max = 1.732 mm, Min =1.632 mm

4215045/A 12/12

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.

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