LM4050QML Precision Micropower Shunt Voltage Reference

Check for Samples: LM4050QML

FEATURES

- **Low Dose Rate Qualified 100 krad(Si)**
- **SEFI Immune**
- **SET Immune with 60µF C_{LOAD}**
- **C_{LOAD} 0µF to 100µF**
- **Fixed Reverse Breakdown Voltage of 2.500V, 5.000V**

KEY SPECIFICATIONS

- **LM4050-2.5QML**
  - **Output Voltage Tolerance IR = 100µA ±0.1% @ 25°C**
  - **Low Temperature Coefficient 15 ppm/°C**
  - **Low Output Noise 50 µVrms(typ)**
  - **Wide Operating Current Range 60 µA to 15 mA**
- **LM4050-5.0QML**
  - **Output Voltage Tolerance IR = 100µA ±0.1% @ 25°C**
  - **Low Temperature Coefficient 23 ppm/°C**
  - **Low Output Noise 100 µVrms(typ)**
  - **Wide Operating Current Range 74 µA to 15 mA**

APPLICATIONS

- **Control Systems**
- **Data Acquisition Systems**
- **Instrumentation**
- **Process Control**
- **Energy Management**

DESCRIPTION

The LM4050QML precision voltage reference is available in a 10-Lead Ceramic CLGA package. The LM4050QML's design eliminates the need for an external stabilizing capacitor while ensuring stability with a capacitive load, thus making the LM4050QML easy to use. The LM4050-2.5QML has a 60 µA minimum and 15 mA maximum operating current. The LM4050-5.0QML has a 74 µA minimum and 15 mA maximum operating current.

The LM4050QML utilizes fuse and zener-zap reverse breakdown voltage trim during wafer sort to ensure that the prime parts have an accuracy of better than ±0.1% at 25°C. Bandgap reference temperature drift curvature correction and low dynamic impedance ensure stable reverse breakdown voltage accuracy over a wide range of operating temperatures and currents.

The LM4050QML operates over the temperature range of -55°C to +125°C.

Connection Diagram

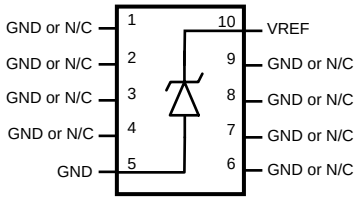


Figure 1. 10-Lead Ceramic CLGA, Top View
See NAC0010A Package

PIN DESCRIPTIONS

Pin Number	Pin Name	Function
1	GND/NC	Ground or No Connect
2	GND/NC	Ground or No Connect
3	GND/NC	Ground or No Connect
4	GND/NC	Ground or No Connect
5	GND	Ground
6	GND/NC	Ground or No Connect
7	GND/NC	Ground or No Connect
8	GND/NC	Ground or No Connect
9	GND/NC	Ground or No Connect
10	VREF	Reference Voltage

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings(1)

Reverse Current		20 mA
Forward Current		10 mA
Power Dissipation (T_A = 25°C)(2)	CLGA Package	467 mW
Lead Temperature (Soldering, 10 seconds)	CLGA Package	260°C
Storage Temperature		-65°C to +150°C
Package Weight (typical)	CLGA Package	241mg
ESD Tolerance (3)		Class 2 (2000V)

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

(2) The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{Jmax} (maximum junction temperature), θ_{JA} (junction to ambient thermal resistance), and T_A (ambient temperature). The maximum allowable power dissipation at any temperature is $PD_{max} = (T_{Jmax} - T_A)/\theta_{JA}$ or the number given in the Absolute Maximum Ratings, whichever is lower. For the LM4050QML, T_{Jmax} = 125°C, and the typical thermal resistance (θ_{JA}), when board mounted, is 214°C/W for the 10-Lead Ceramic CLGA package.

(3) The human body model is a 100 pF capacitor discharged through a 1.5 kΩ resistor into each pin.

Operating Ratings (1)

Temperature Range		-55°C ≤ T_A ≤ +125°C
Reverse Current	LM4050-2.5QML	60 µA to 15 mA
	LM4050-5.0QML	74 µA to 15 mA

(1) The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{Jmax} (maximum junction temperature), θ_{JA} (junction to ambient thermal resistance), and T_A (ambient temperature). The maximum allowable power dissipation at any temperature is $PD_{max} = (T_{Jmax} - T_A)/\theta_{JA}$ or the number given in the Absolute Maximum Ratings, whichever is lower. For the LM4050QML, T_{Jmax} = 125°C, and the typical thermal resistance (θ_{JA}), when board mounted, is 214°C/W for the 10-Lead Ceramic CLGA package.

Package Thermal Resistance

Package	θ_{JA} (Still Air)	θ_{JA} (500LF/Min Air flow)	θ_{JC}
CLGA Package on 2 layer, 1oz PCB	214°C/ W	147°C/ W	20.87°C/ W

Quality Conformance Inspection

MIL-STD-883, Method 5005 - Group A

Subgroup	Description	Temp (C)
1	Static tests at	+25
2	Static tests at	+125
3	Static tests at	-55
4	Dynamic tests at	+25
5	Dynamic tests at	+125
6	Dynamic tests at	-55
7	Functional tests at	+25
8A	Functional tests at	+125
8B	Functional tests at	-55
9	Switching tests at	+25
10	Switching tests at	+125
11	Switching tests at	-55
12	Setting time at	+25
13	Setting time at	+125
14	Setting time at	-55

LM4050-2.5QML Electrical Characteristics SMD: 5962R0923561

The initial Reverse Breakdown Voltage tolerance is ±0.1% @ 100µA.

Symbol	Parameter	Conditions	Notes	Typical (1)	Min	Max	Units	Sub-groups
V_R	Reverse Breakdown Voltage	I_R = 100 µA		2.500			V	
	Reverse Breakdown Voltage Tolerance	I_R = 60µA				±2.5	mV	1
		I_R = 100µA				±2.5		
		I_R = 1mA				±3.75		
		I_R = 10mA				±10		
		I_R = 15mA				±13		
		I_R = 60µA				**±5**	mV	2
		I_R = 100µA				**±5**		
		I_R = 1mA				**±6.25**		
		I_R = 10mA				**±12.5**		
		I_R = 15mA				**±14**		
		I_R = 60µA				**±4.5**	mV	3
		I_R = 100µA				**±4.5**		
		I_R = 1mA				**±5.75**		
		I_R = 10mA				**±13**		
		I_R = 15mA				**±17.5**		
I_{RMIN}	Minimum Operating Current			40.5		60	µA	1
						65	µA	2, 3

(1) Typicals are at T_A = 25°C and represent most likely parametric norm.

LM4050-2.5QML Electrical Characteristics SMD: 5962R0923561 (continued)

The initial Reverse Breakdown Voltage tolerance is ±0.1% @ 100µA.

Symbol	Parameter	Conditions	Notes	Typical (1)	Min	Max	Units	Sub-groups
$\Delta V_R/\Delta T$	Average Reverse Breakdown Voltage Temperature Coefficient @ 25°C ≤ T_A ≤ 125°C	I_R = 60µA	See (2)	±3		**±15**	ppm/°C	2
		I_R = 100µA		±3		**±16**		
		I_R = 1mA		±3		**±18**		
		I_R = 10mA		±4		**±20**		
		I_R = 15mA		±6		**±22**		
	Average Reverse Breakdown Voltage Temperature Coefficient @ −55°C ≤ T_A ≤ 25°C	I_R = 60µA	See (2)	±3		**±18**		3
		I_R = 100µA		±3		**±19**		
		I_R = 1mA		±3.5		**±22**		
		I_R = 10mA		±10		**±32**		
		I_R = 15mA		±15		**±45**		
Z_R	Reverse Dynamic Impedance	I_R = 1 mA, f = 120 Hz, I_{AC} = 0.1 I_R		0.3			Ω	
V_N	Output Noise Voltage	0.1 Hz ≤ f ≤ 10 Hz		9			µVpp	
		10 Hz ≤ f ≤ 10KHz		50			µVrms	
C_{LOAD}	Load Capacitor	Stable Over Temperature	See (3)	60	0	100	µF	
V_{HYST}	Thermal Hysteresis	ΔT = −55°C to 125°C	See (4)	1			ppm	

(2) Not tested post irradiation. Typical post irradiation values listed in the post radiation Tempco table.

(3) Capacitive load not required but improves SET stability. This parameter is guaranteed by design and/or characterization and is not tested in production.

(4) Thermal hysteresis is defined as the change in voltage measured at +25°C after cycling to temperature -55°C and the 25°C measurement after cycling to temperature +125°C.

$$V_{HYST} = \frac{|V_{R1} - V_{R2}|}{V_R} \times 10^6 \text{ ppm}$$

Where: V_{HYST} = Thermal hysteresis expressed in ppm
V_R = Nominal preset output voltage
V_{R1} = V_R before temperature fluctuation
V_{R2} = V_R after temperature fluctuation.

Post Radiation @ 25°C (1)

The initial Reverse Breakdown Voltage tolerance is ±0.1% @ 100µA.

Symbol	Parameter	Conditions		30 krad	50 krad	100 krad	Sub-groups
V_R	Reverse Breakdown Voltage Tolerance	I_R = 60µA	Max	+0.42%	+0.67%	+1.5%	1
		I_R= 100µA					
		I_R = 1mA					
		I_R = 10mA					
		I_R = 15mA					

(1) Pre and post irradiation limits are identical to those listed under electrical characteristics except as listed in the post radiation table.

Post Radiation Tempco (1)

Symbol	Parameter	Conditions	TYPICALS			
			30 krad	50 krad	100 krad	Units
$\Delta V_R/\Delta T$	Average Reverse Breakdown Voltage Temperature Coefficient Drift @ 25°C ≤ T_A ≤ 125°C	60µA ≤ I_R ≤ 15mA	+41	+83	+144	ppm/°C
	Average Reverse Breakdown Voltage Temperature Coefficient Drift @ −55°C ≤ T_A ≤ 25°C	60µA ≤ I_R ≤ 15mA	+46	+87	+166	ppm/°C

(1) Not tested post irradiation. Typical post irradiation values listed in the post radiation Tempco table.

Operational Life Test Delta Parameters

This table represents the drift seen from initial measurements post 1000hr Operational Life Burn-In. All units will remain within the electrical characteristics limits post 1000hr Operational Life Burn-In. Deltas required for QMLV product at Group B, Sub-Group 5.

Symbol	Parameter	Conditions	Note	Min	Max	Units	Temp
V_R	Reverse Breakdonwn Voltage Tolerance	I_R = 60µA		-0.873	0.873	mV	1
		I_R = 100µA		-0.873	0.873		
		I_R = 1mA		-0.998	0.998		
		I_R = 10mA		-3.93	3.93		
		I_R = 15mA		-5	5		
I_{RMIN}	Minimum Operating Current			-0.623	0.623	µA	1

LM4050-5.0QML Electrical Characteristics SMD: 5962R0923562

The initial Reverse Breakdown Voltage tolerance is ±0.1% @ 100µA.

Symbol	Parameter	Conditions	Notes	Typical (1)	Min	Max	Units	Sub-groups
V_R	Reverse Breakdown Voltage	I_R = 100 µA		5.000			V	
	Reverse Breakdown Voltage Tolerance	I_R = 74µA				±5.0	mV	1
		I_R = 100µA				±5.0		
		I_R = 1mA				±8		
		I_R = 10mA				±18		
		I_R = 15mA				±20		
		I_R = 74µA				**±10**	mV	2
		I_R = 100µA				**±10**		
		I_R = 1mA				**±12**		
		I_R = 10mA				**±22.5**		
		I_R = 15mA				**±28**		
		I_R = 74µA				**±9**	mV	3
		I_R = 100µA				**±9**		
		I_R = 1mA				**±11.5**		
		I_R = 10mA				**±29**		
		I_R = 15mA				**±37**		
I_{RMIN}	Minimum Operating Current			53		70	µA	1
						74	µA	2, 3
$\Delta V_R/\Delta T$	Average Reverse Breakdown Voltage Temperature Coefficient @ 25°C ≤ T_A ≤ 125°C	I_R = 74µA	See (2)	±9		**±23**	ppm/°C	2
		I_R = 100µA		±9		**±25**		
		I_R = 1mA		±10		**±28**		
		I_R = 10mA		±11		**±35**		
		I_R = 15mA		±11		**±40**		
	Average Reverse Breakdown Voltage Temperature Coefficient @ −55°C ≤ T_A ≤ 25°C	I_R = 74µA	See (2)	±10		**±25**		3
		I_R = 100µA		±10		**±29**		
		I_R = 1mA		±10		**±34**		
		I_R = 10mA		±15		**±45**		
		I_R = 15mA		±20		**±60**		
Z_R	Reverse Dynamic Impedance	I_R = 1 mA, f = 120 Hz, I_{AC} = 0.1 I_R		0.5			Ω	
V_N	Output Noise Voltage	10 Hz ≤ f ≤ 10KHz		100			µVrms	

(1) Typicals are at T_A = 25°C and represent most likely parametric norm.
(2) Not tested post irradiation. Typical post irradiation values listed in the post radiation Tempco table.

LM4050-5.0QML Electrical Characteristics SMD: 5962R0923562 (continued)

The initial Reverse Breakdown Voltage tolerance is ±0.1% @ 100µA.

Symbol	Parameter	Conditions	Notes	Typical (1)	Min	Max	Units	Sub-groups
C_{LOAD}	Load Capacitor	Stable Over Temperature	See (3)	60	0	100	µF	
V_{HYST}	Thermal Hysteresis	ΔT = -55°C to 125°C	See (4)	20			ppm	

(3) Capacitive load not required but improves SET stability. This parameter is guaranteed by design and/or characterization and is not tested in production.

(4) Thermal hysteresis is defined as the change in voltage measured at +25°C after cycling to temperature -55°C and the 25°C measurement after cycling to temperature +125°C.

$$V_{HYST} = \frac{|V_{R1} - V_{R2}|}{V_R} \times 10^6 \text{ ppm}$$

Where: V_{HYST} = Thermal hysteresis expressed in ppm
V_R = Nominal preset output voltage
V_{R1} = V_R before temperature fluctuation
V_{R2} = V_R after temperature fluctuation.

Post Radiation @ 25°C (1)

The initial Reverse Breakdown Voltage tolerance is ±0.1% @ 100µA.

Symbol	Parameter	Conditions		30 krad	50 krad	100 krad	Sub-groups
V_R	Reverse Breakdown Voltage Tolerance	I_R = 74µA	Max	+0.37%	+0.61%	+1.75%	1
		I_R= 100µA					
		I_R = 1mA					
		I_R = 10mA					
		I_R = 15mA					

(1) Pre and post irradiation limits are identical to those listed under electrical characteristics except as listed in the post radiation table.

Post Radiation Tempco (1)

Symbol	Parameter	Conditions	TYPICALS			
			30 krad	50 krad	100 krad	Units
$\Delta V_R/\Delta T$	Average Reverse Breakdown Voltage Temperature Coefficient Drift @ 25°C ≤ T_A ≤ 125°C	74µA ≤ I_R ≤ 15mA	+87	+166	+387	ppm/°C
	Average Reverse Breakdown Voltage Temperature Coefficient Drift @ −55°C ≤ T_A ≤ 25°C	74µA ≤ I_R ≤ 15mA	+96	+162	+343	ppm/°C

(1) Not tested post irradiation. Typical post irradiation values listed in the post radiation Tempco table.

Operational Life Test Delta Parameters

This table represents the drift seen from initial measurements post 1000hr Operational Life Burn-In. All units will remain within the electrical characteristics limits post 1000hr Operational Life Burn-In. Deltas required for QMLV product at Group B, Sub-Group 5.

Symbol	Parameter	Conditions	Note	Min	Max	Units	Temp
V_R	Reverse Breakdonwn Voltage Tolerance	I_R = 74µA		−0.8	0.8	mV	1
		I_R = 100µA		−0.8	0.8		
		I_R = 1mA		−0.84	0.84		
		I_R = 10mA		−1.6	1.6		
		I_R = 15mA		−2.6	2.6		
I_{RMIN}	Minimum Operating Current			−0.623	0.623	µA	1

Typical Performance Characteristics

Output Impedance vs Frequency

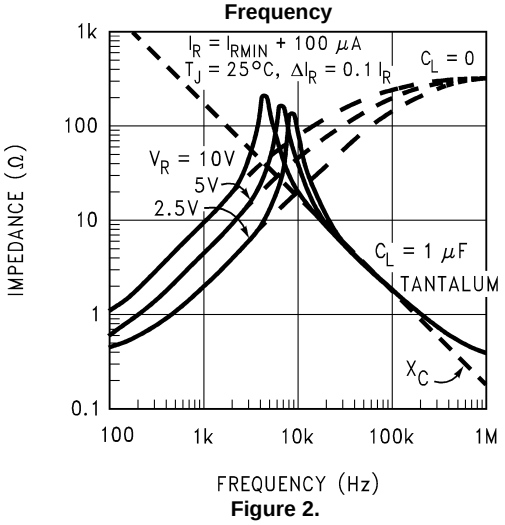


Figure 2.

Output Impedance vs Frequency

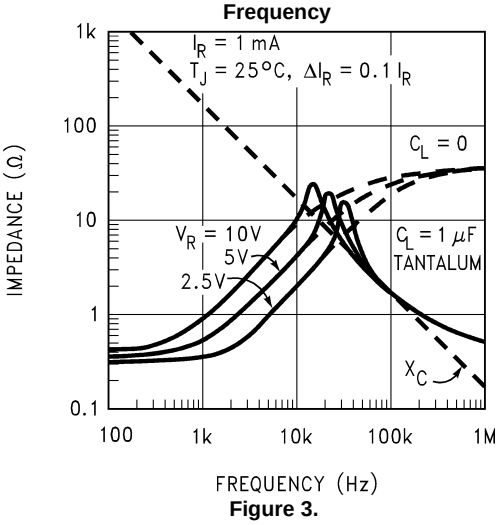


Figure 3.

Reverse Characteristics and Minimum Operating Current

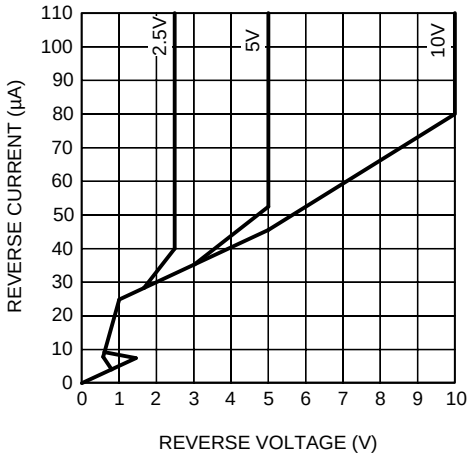


Figure 4.

2.5V Thermal Hysteresis

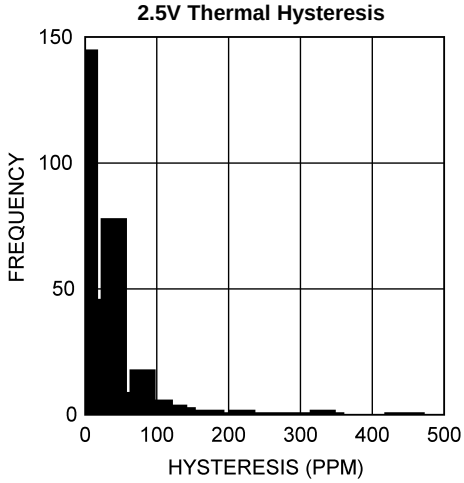


Figure 5.

5.0V Thermal Hysteresis

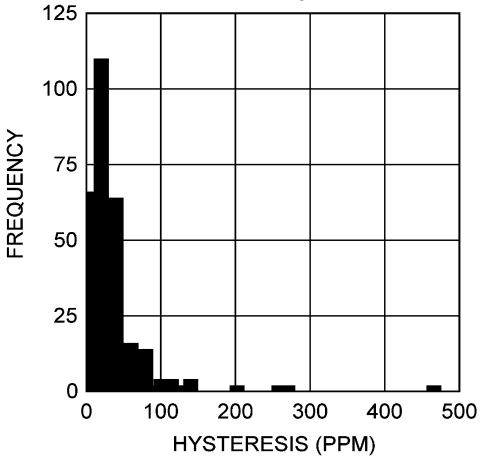


Figure 6.

Typical Radiation Characteristics

2.5V Low Dose Rate Drift at 10 mrad(Si)/s

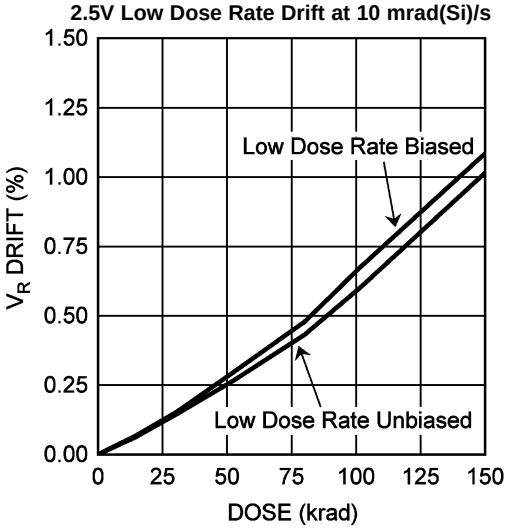


Figure 7.

5V Low Dose Rate Drift at 10 mrad(Si)/s

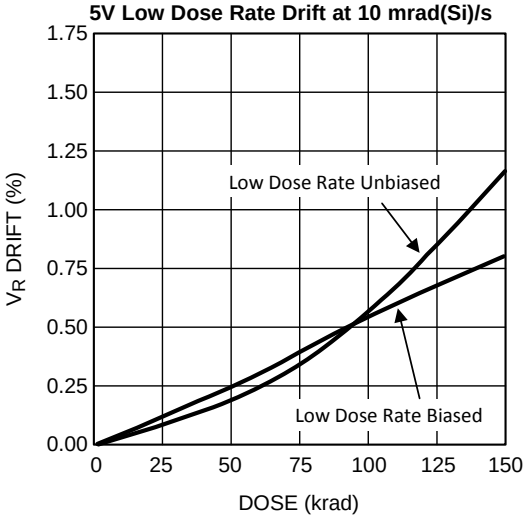


Figure 8.

Start-Up Characteristics

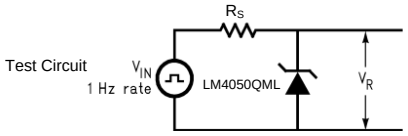


Figure 9.

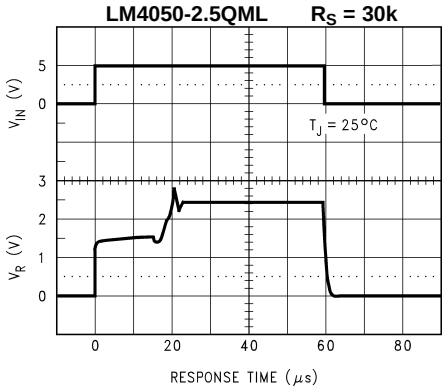


Figure 10.

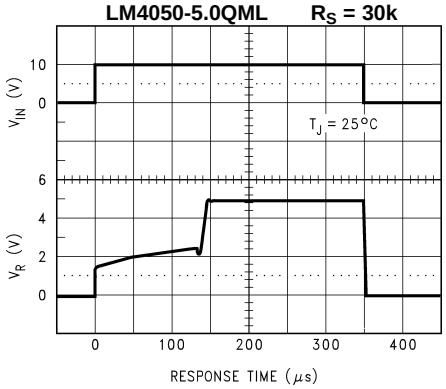
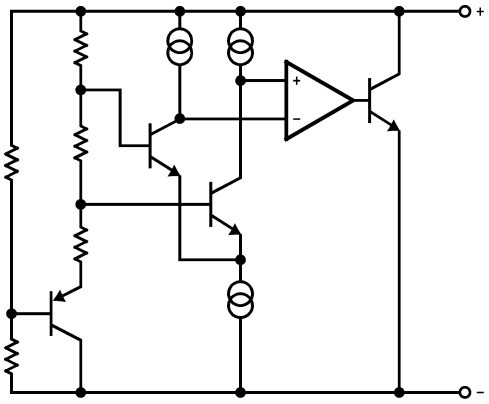


Figure 11.

Functional Block Diagram



APPLICATIONS INFORMATION

The LM4050QML is a precision micro-power curvature-corrected bandgap shunt voltage reference. The LM4050QML is available in the 10-Lead Ceramic CLGA package. The LM4050QML has been designed for stable operation without the need of an external capacitor connected between the "+" pin and the "−" pin. If, however, a bypass capacitor is used, the LM4050QML remains stable. The LM4050-2.5QML has a 60 µA minimum and 15 mA maximum operating current. The LM4050-5.0QML has a 74 µA minimum and 15 mA maximum operating current.

The typical thermal hysteresis specification is defined as the change in +25°C voltage measured after thermal cycling. The device is thermal cycled to temperature -55°C and then measured at 25°C. Next the device is thermal cycled to temperature +125°C and again measured at 25°C. The resulting V_{OUT} delta shift between the 25°C measurements is thermal hysteresis. Thermal hysteresis is common in precision references and is induced by thermal-mechanical package stress. Changes in environmental storage temperature, operating temperature and board mounting temperature are all factors that can contribute to thermal hysteresis.

In a conventional shunt regulator application (Figure 12) , an external series resistor (R_S) is connected between the supply voltage and the LM4050QML. R_S determines the current that flows through the load (I_L) and the LM4050QML (I_Q). Since load current and supply voltage may vary, R_S should be small enough to supply at least the maximum guaranteed I_{RMIN} (spec. table) to the LM4050QML even when the supply voltage is at its minimum and the load current is at its maximum value. When the supply voltage is at its maximum and I_L is at its minimum, R_S should be large enough so that the current flowing through the LM4050QML is less than 15 mA.

R_S is determined by the supply voltage, (V_S), the load and operating current, (I_L and I_Q), and the LM4050QML's reverse breakdown voltage, V_R.

$$R_S = \frac{V_S - V_R}{I_L + I_Q} \quad (1)$$

Radiation Environments

Careful consideration should be given to environmental conditions when using a product in a radiation environment.

TOTAL IONIZING DOSE

Radiation hardness assured (RHA) products are those part numbers with a total ionizing dose (TID) level specified in the Ordering Information table on the front page. Testing and qualification of these products is done on a wafer level according to MIL-STD-883, Test Method 1019. Wafer level TID data is available with lot shipments.

Testing and qualification is performed at the 30, 50 and 100 krad TID levels at a dose rate of 10 mrad/s, using a 1.5X overtest at each TID level. For the 30 krad level units are tested to 50 krad, for 50 krad units are tested to 80 krad and for 100 krad units are tested to 150 krad, with all parameters remaining inside the post irradiation test limits.

SINGLE EVENT EFFECTS (SEE)

One time single event effects characterization was performed according to EIA/JEDEC Standard, EIA/JEDEC57.

A test report is available upon request.

SINGLE EVENT TRANSIENTS (SET)

With a 60 µF capacitor on the output, no single event transients were seen at the highest linear energy transfer (LET) tested: 59 MeV-cm^2/mg.

SET characterization with other capacitor values is in the SEE report, available upon request.

SINGLE EVENT FUNCTIONAL INTERRUPT (SEFI)

No single event functional interrupts were detected to the highest linear energy transfer (LET) tested: 100 MeV-cm^2/mg.

Typical Applications

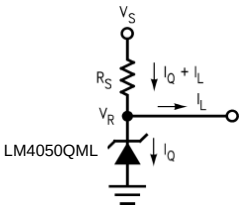


Figure 12. Shunt Regulator

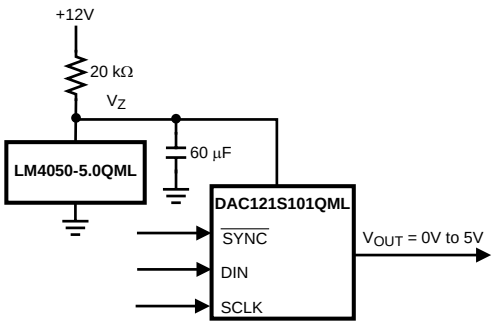


Figure 13. The LM4050QML as a power supply and reference

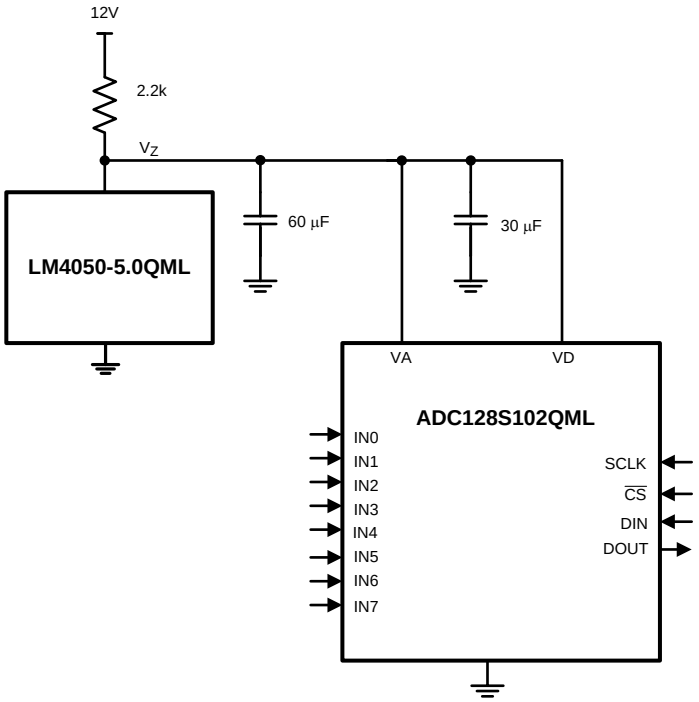


Figure 14. The LM4050QML as a power supply and reference

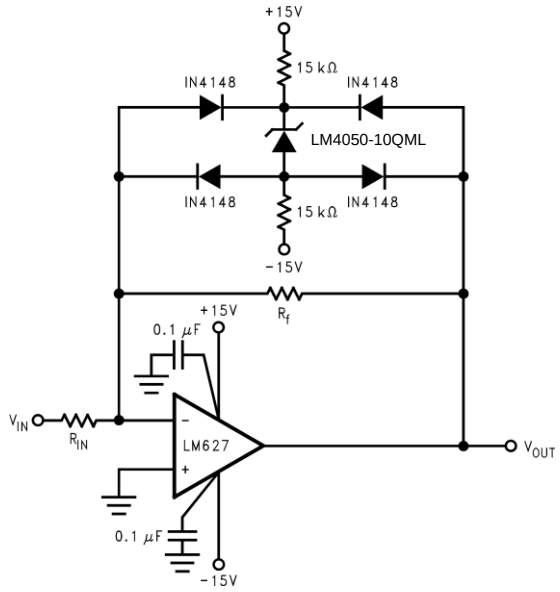
The LM4050QML is a good choice as a power regulator for the DAC121S101QML or ADC128S102QML. The minimum resistor value in the circuit of Figure 13 or Figure 14 should be chosen such that the maximum current through the LM4050QML does not exceed its 15 mA rating. The conditions for maximum current include the input voltage at its maximum, the LM4050QML voltage at its minimum, the resistor value at its minimum due to tolerance, and the DAC121S101QML or ADC128S102QML draws zero current. The maximum resistor value must allow the LM4050QML to draw more than its minimum current for regulation plus the maximum DAC121S101QML or ADC128S102QML current in full operation. The conditions for minimum current include the input voltage at its minimum, the LM4050QML voltage at its maximum, the resistor value at its maximum due to tolerance, and the DAC121S101QML or ADC128S102QML draws its maximum current. These conditions can be summarized as

$$R(min) = (V_{IN}(max) - V_Z(min) / (I_A(min) + I_Z(max) \quad (2)$$

and

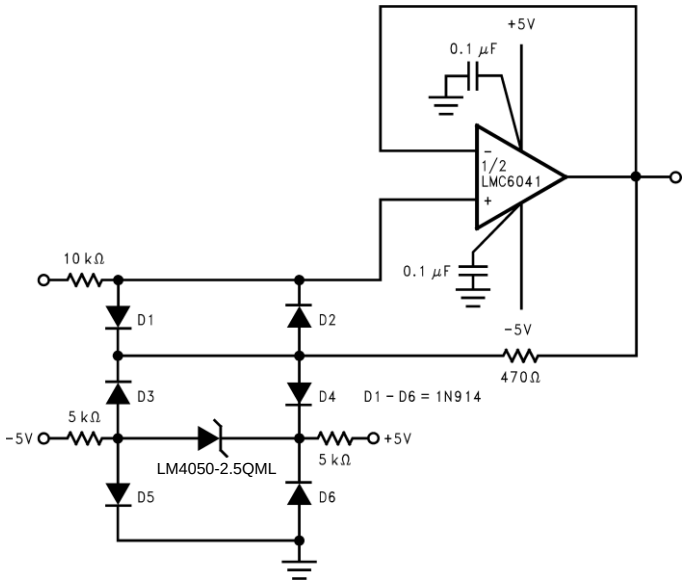
$$R(max) = (V_{IN}(min) - V_Z(max) / (I_A(max) + I_Z(min) \quad (3)$$

where $V_Z(min)$ and $V_Z(max)$ are the nominal LM4050QML output voltages ± the LM4050QML output tolerance over temperature, $I_Z(max)$ is the maximum allowable current through the LM4050QML, $I_Z(min)$ is the minimum current required by the LM4050QML for proper regulation, $I_A(max)$ is the maximum DAC121S101QML or ADC128S102QML supply current, and $I_A(min)$ is the minimum DAC121S101QML or ADC128S102QML supply current.



Nominal clamping voltage is ±11.5V (LM4050QML's reverse breakdown voltage +2 diode V_F).
Bounded amplifier reduces saturation-induced delays and can prevent succeeding stage damage.

Figure 15. Bounded amplifier



The bounding voltage is ±4V with the LM4050-2.5QML
(LM4050QML's reverse breakdown voltage + 3 diode V_F).

Figure 16. Protecting Op Amp input

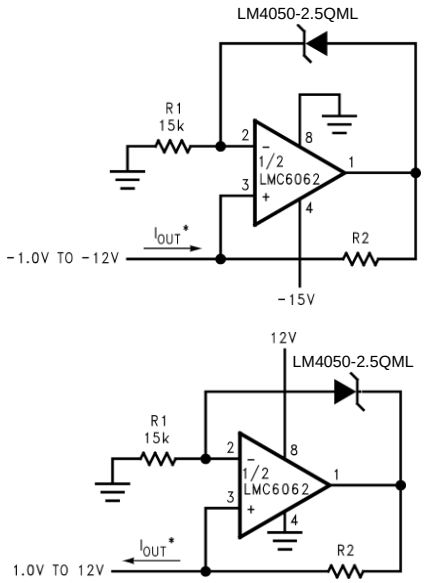


Figure 17. Precision 1 µA to 1 mA Current Sources

$$*I_{OUT} = \frac{2.5V}{R2} \quad (4)$$

Revision History

Date Released	Revision	Section	Changes
08/20/2010	A	Initial Release	New Product Low Dose Qualified LM4050WG2.5RLQV Initial Release
01/20/2012	B	General Description, Features, Key Specifications, Ordering Table, Operating Ratings, Package Thermal Table, Electrical Section	General Description, Features, Key Specifications, Ordering Table, Operating Ratings, Package Thermal Table, Electrical Section — Added the 5.0 V option information for all sections. Added new NSIDS LM4050WG5.0RLQV and LM4050WG5.0–MPR Voltage option to data sheet. Revision A will be Archived.
05/23/2012	C	Electrical Section	Electrical Section — Updated Delta Vr/Delta T for typical limits for both the 2.5 and 5.0 versions. Revision B will be Archived.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
5962R0923561VZA	ACTIVE	CLGA	NAC	10	54	TBD	A42 SNPB	Level-1-NA-UNLIM	-55 to 125	LM4050WG 2.5RLQV Q 5962R09235 61VZA ACO 61VZA >T	Samples
LM4050WG2.5RLQV	ACTIVE	CLGA	NAC	10	54	TBD	A42 SNPB	Level-1-NA-UNLIM	-55 to 125	LM4050WG 2.5RLQV Q 5962R09235 61VZA ACO 61VZA >T	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Only one of markings shown within the brackets will appear on the physical device.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

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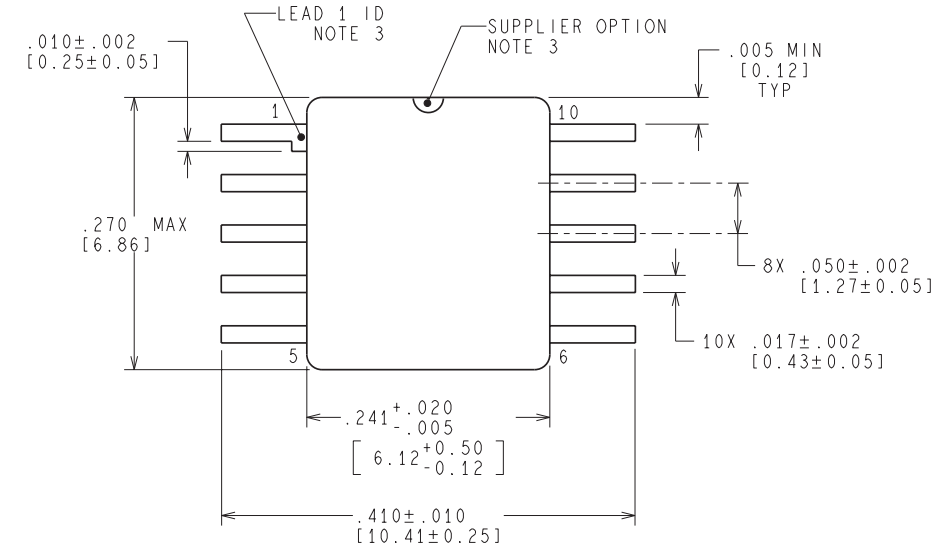

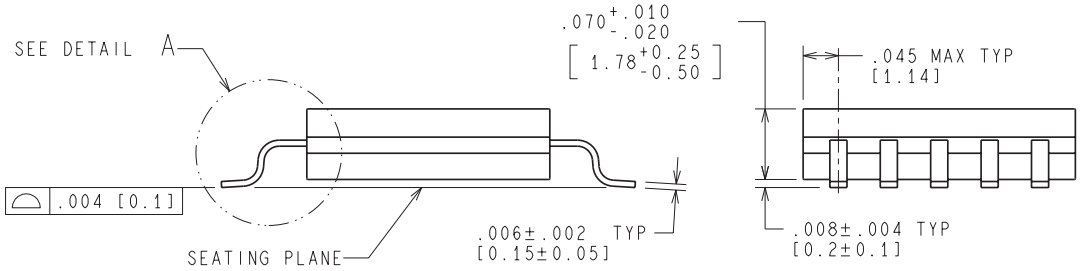

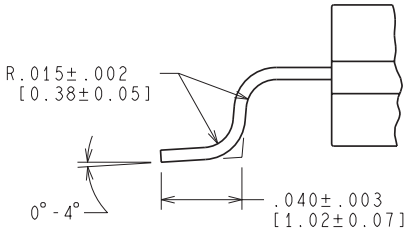

DETAIL A
TYPICAL

MIL-PRF-38535
CONFIGURATION CONTROL

WG10A (Rev H)

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