LM4846 Boomer™ Audio Power Amplifier Series Output Capacitor-less Audio Subsystem with Programmable Texas Instruments 3D

Check for Samples: LM4846

FEATURES

- **I²C/SPI Control Interface**
- **I²C/SPI Programmable Texas Instruments 3D Audio**
- **I²C/SPI Controlled 32 Step Digital Volume Control (-54dB to +18dB)**
- **Three Independent Volume Channels (Left, Right, Mono)**
- **Eight Distinct Output Modes**
- **DSBGA Surface Mount Packaging**
- **"Click and Pop" Suppression Circuitry**
- **Thermal Shutdown Protection**
- **Low Shutdown Current (0.1µA, Typ)**

APPLICATIONS

- **Mobile Phones**
- **PDAs**

KEY SPECIFICATIONS

- **THD+N at 1kHz, 500mW into 8Ω BTL (3.3V), 1.0% (Typ)**
- **THD+N at 1kHz, 30mW into 32Ω SE (3.3V), 1.0% (Typ)**
- **Single Supply Operation (V_{DD}), 2.7 to 5.5V**
- **I²C/SPI Single Supply Operation, 2.2 to 5.5V**

DESCRIPTION

The LM4846 is an audio power amplifier capable of delivering 500mW of continuous average power into a mono 8Ω bridged-tied load (BTL) with 1% THD+N, 25mW per channel of continuous average power into stereo 32Ω single-ended (SE) loads with 1% THD+N, or an output capacitor-less (OCL) configuration with identical specification as the SE configuration, from a 3.3V power supply.

The LM4846 features a 32-step digital volume control and eight distinct output modes. The digital volume control, 3D enhancement, and output modes (mono/SE/OCL) are programmed through a two-wire I²C or a three-wire SPI compatible interface that allows flexibility in routing and mixing audio channels. The LM4846 has three input channels: one pair for a two-channel stereo signal and the third for a single-channel mono input.

The LM4846 is designed for cellular phone, PDA, and other portable handheld applications. It delivers high quality output power from a surface-mount package and requires only seven external components in the OCL mode (two additional components in SE mode).

Typical Application

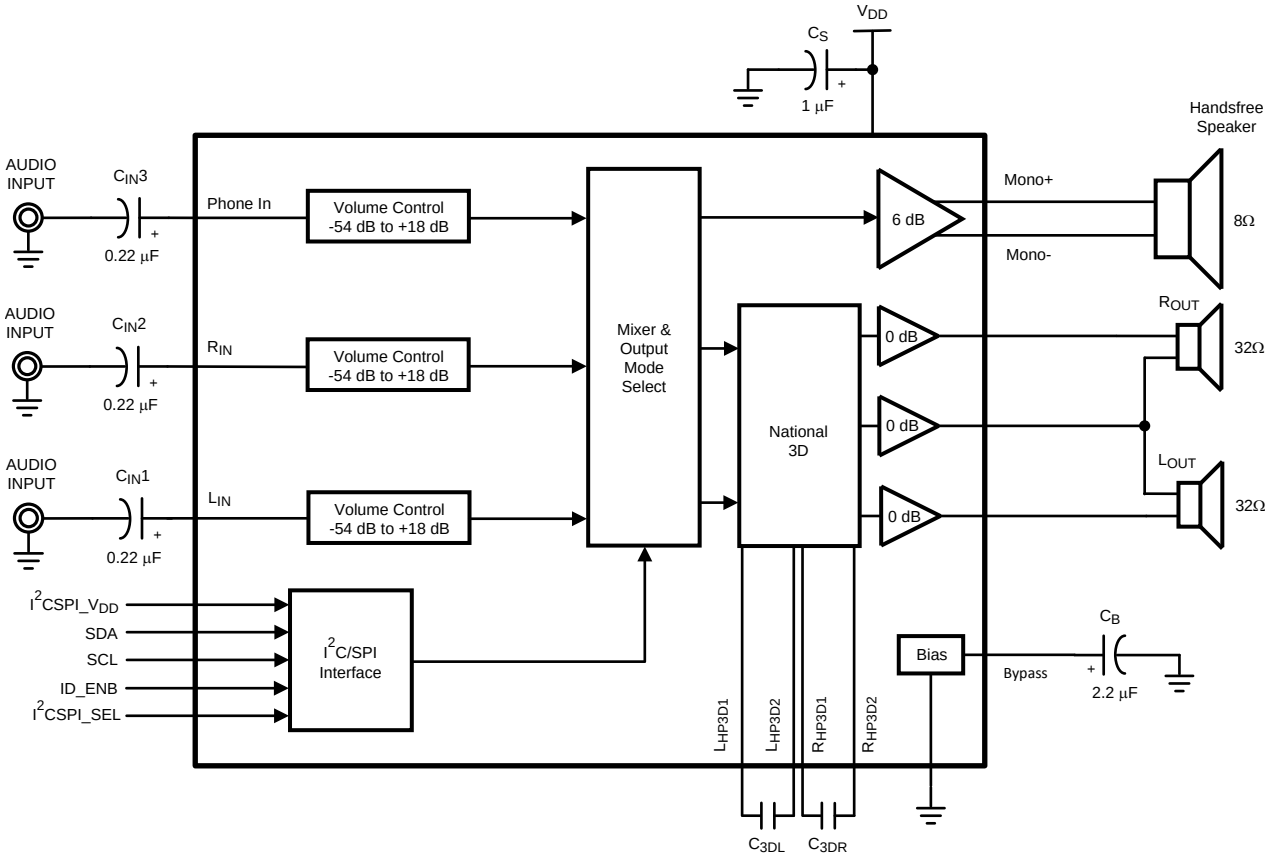


Figure 1. Typical Audio Amplifier Application Circuit-Output Capacitor-less

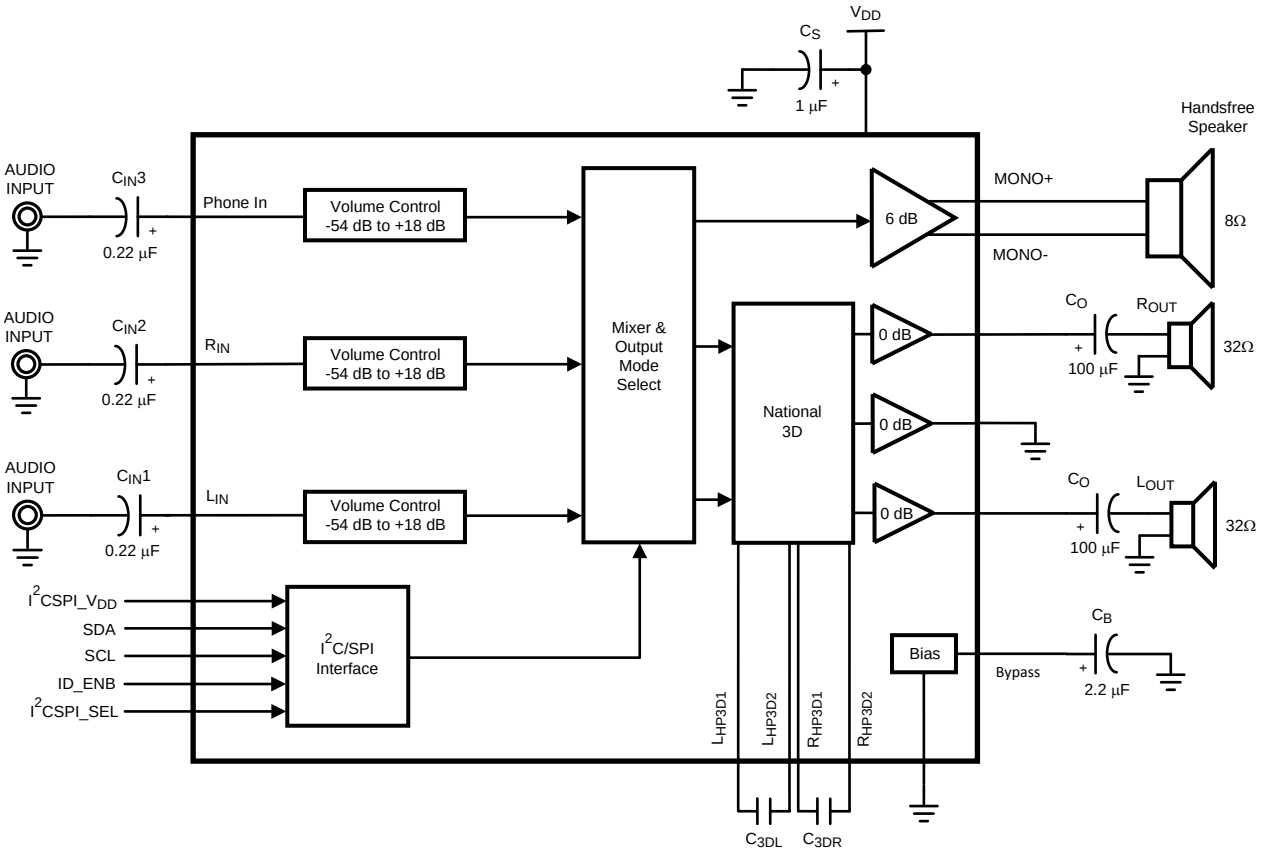


Figure 2. Typical Audio Amplifier Application Circuit-Single Ended

Connection Diagram

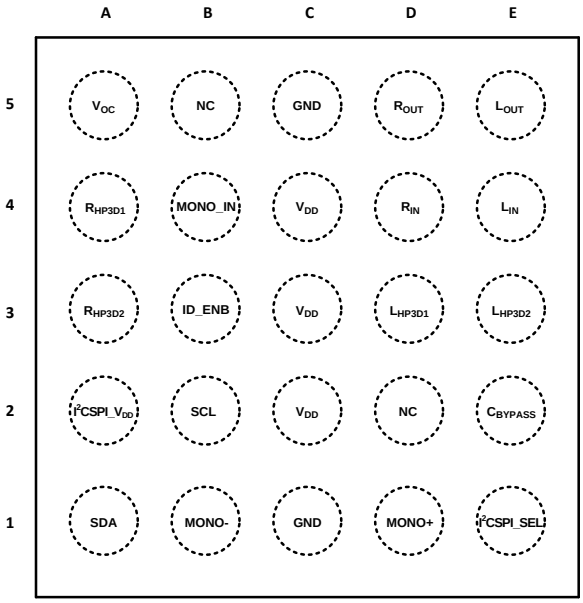


Figure 3. 25-Bump DSBGA - Top View

PIN DESCRIPTIONS

	Bump	Name	Description
1	A1	SDA	I^2C or SPI Data
2	A2	$I^2CSPI\_V_{DD}$	I^2C or SPI Interface Power Supply
3	A3	R_{HP3D2}	Right Headphone 3D Input 2
4	A4	R_{HP3D1}	Right Headphone 3D Input 1
5	A5	VOC	Center Amplifier Output
6	B1	MONO-	Loudspeaker Negative Output
7	B2	SCL	I^2C or SPI Clock
8	B3	ID_ENB	Address Identification/Enable Bar
9	B4	Phone_In	Mono Input
10	B5	NC	No Connect
11	C1	GND	Ground
12	C2	V_{DD}	Power Supply
13	C3	V_{DD}	Power Supply
14	C4	V_{DD}	Power Supply
15	C5	GND	GND
16	D1	MONO+	Loudspeaker Positive Output
17	D2	NC	No Connect
18	D3	L_{HP3D1}	Left Headphone 3D Input 1
19	D4	R_{IN}	Right Input Channel
20	D5	R_{OUT}	Right Headphone Output
21	E1	I^2C SPI_SEL	I^2C or SPI Select
22	E2	C_{BYPASS}	Half-Supply Bypass
23	E3	L_{HP3D2}	Left Headphone 3D Input 2
24	E4	L_{IN}	Left Input Channel
25	E5	L_{OUT}	Left Headphone Output

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings(1)(2)

Supply Voltage		6.0V
Storage Temperature		−65°C to +150°C
Input Voltage		−0.3 to V_{DD} +0.3
ESD Susceptibility(3)		2.0kV
ESD Machine model(4)		200V
Junction Temperature (T_J)		150°C
Solder Information	Vapor Phase (60 sec.)	215°C
	Infrared (15 sec.)	220°C
Thermal Resistance	θ_{JA} (typ) - YZR0025	65°C/W(5)

(1) Operating Ratings indicate conditions for which the device is functional, but do not ensure specific performance limits. For ensured specifications and test conditions, see the Electrical Characteristics. The ensured specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.
(3) Human body model, 100pF discharged through a 1.5kΩ resistor.
(4) Machine Model ESD test is covered by specification EIAJ IC-121-1981. A 200pF cap is charged to the specified voltage, then discharged directly into the IC with no external series resistor (resistance of discharge path must be under 50Ω).
(5) The given θ_{JA} for an LM4846ITL mounted on a demonstration board with a $9in^2$ area of 1oz printed circuit board copper ground plane.

Operating Ratings(1)

Temperature Range	−40°C to 85°C
Supply Voltage (V_{DD})	2.7V ≤ V_{DD} ≤ 5.5V
Supply Voltage (I^2C/SPI)	2.2V ≤ V_{DD} ≤ 5.5V

(1) Operating Ratings indicate conditions for which the device is functional, but do not ensure specific performance limits. For ensured specifications and test conditions, see the Electrical Characteristics. The ensured specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Electrical Characteristics 3.3V[1][2]

The following specifications apply for V_{DD} = 3.3V, T_A = 25°C unless otherwise specified. [A_V = 2 (BTL), A_V = 1 (SE)]

Symbol	Parameter	Conditions	LM4846		Units (Limits)
			Typical [3]	Limits [4]	
I_{DD}	Supply Current	Output Modes 2, 4, 6 V_{IN} = 0V; No load, OCL = 0 (Table 2)	3.3	6.5	mA (max)
		Output Modes 1, 3, 5, 7 V_{IN} = 0V; No load, BTL, OCL = 0 (Table 2)	6	11	mA (max)
I_{SD}	Shutdown Current	Output Mode 0	0.1	1	µA (max)
V_{OS}	Output Offset Voltage	V_{IN} = 0V, Mode 5[5]	10	50	mV (max)
P_O	Output Power	$MONO_{OUT}$; R_L = 8Ω THD+N = 1%; f = 1kHz, BTL, Mode 1	500	400	mW (min)
		R_{OUT} and L_{OUT}; R_L = 32Ω THD+N = 1%; f = 1kHz, SE, Mode 4	42	20	mW (min)
THD+N	Total Harmonic Distortion Plus Noise	$MONO_{OUT}$ f = 20Hz to 20kHz P_{OUT} = 250mW; R_L = 8Ω, BTL, Mode 1	0.5		%
		R_{OUT} and L_{OUT} f = 20Hz to 20kHz P_{OUT} = 12mW; R_L = 32Ω, SE, Mode 4	0.5		%
N_{OUT}	Output Noise	A-weighted[6], Mode 5, BTL input referred	26		µV
PSRR	Power Supply Rejection Ratio $MONO_{OUT}$	V_{RIPPLE} = 200mV_{PP}; f = 217Hz, C_B = 2.2µF, BTL All audio inputs terminated into 50Ω; output referred gain = 6dB (BTL)			
		Output Mode 1,7	71		dB
		Output Mode 3	68		dB
		Output Mode 5	63		dB
	Power Supply Rejection Ratio R_{OUT} and L_{OUT}	V_{RIPPLE} = 200mV_{PP}; f = 217Hz C_B = 2.2µF, SE, C_O = 100µF All audio inputs terminated into 50Ω; output referred gain, OCL = 0 (Table 2)			
		Output Mode 2	88		dB
		Output Mode 4	76		dB
		Output Mode 6, 7	76		dB
	Digital Volume Range (R_{IN} and L_{IN})	Input referred maximum attenuation	-54	–53.25 –54.75	dB (min) dB (max)
		Input referred maximum gain	18	17.25 18.75	dB (min) dB (max)
	Mute Attenuation	Output Mode 1, 3, 5	80		dB
	MONO_IN Input Impedance R_{IN} and L_{IN} Input Impedance	Maximum gain setting	11	8 14	kΩ (min) kΩ (max)
		Maximum attenuation setting	100	75 125	kΩ (min) kΩ (max)
T_{WU}	Wake-Up Time from Shutdown	C_B = 2.2µF, OCL C_B = 2.2µF, SE	90 138		ms

(1) Operating Ratings indicate conditions for which the device is functional, but do not ensure specific performance limits. For ensured specifications and test conditions, see the Electrical Characteristics. The ensured specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.
(2) All voltages are measured with respect to the ground pin, unless otherwise specified.
(3) Typical specifications are specified at +25°C and represent the most likely parametric norm.
(4) Tested limits are specified to Texas Instruments' AOQL (Average Outgoing Quality Level).
(5) Potentially worse case: All three input stages are DC coupled to the BTL output stage.
(6) Datasheet min/max specifications are ensured by design, test, or statistical analysis.

Electrical Characteristics 5.0V(1) (2)

The following specifications apply for V_{DD} = 5.0V, T_A = 25°C unless otherwise specified. [A_V = 2 (BTL), A_V = 1 (SE)].

Symbol	Parameter	Conditions	LM4846		Units (Limits)
			Typical(3)	Limits(4)(5)	
I_{DD}	Supply Current	Output Modes 2, 4, 6 V_{IN} = 0V; No load, OCL = 0 (Table 2)	3.6		mA
		Output Modes 1, 3, 5, 7 V_{IN} = 0V; No Load, OCL = 0 (Table 2)	6.8		mA
I_{SD}	Shutdown Current	Output Mode 0	0.1	.5	µA
V_{OS}	Output Offset Voltage	V_{IN} = 0V, Mode 5(5)	10		mV
P_O	Output Power	$MONO_{OUT}$; R_L = 8Ω THD+N = 1%; f = 1kHz, BTL, Mode 1	1.15		W
		R_{OUT} and L_{OUT}; R_L = 32Ω THD+N = 1%; f = 1kHz, SE, Mode 4	75		mW
THD+N	Total Harmonic Distortion Plus Noise	$MONO_{OUT}$ f = 20Hz to 20kHz P_{OUT} = 500mW; R_L = 8Ω, BTL, Mode 1	0.5		%
		R_{OUT} and L_{OUT} f = 20Hz to 20kHz P_{OUT} = 30mW; R_L = 32Ω,SE, Mode 4	0.5		%
N_{OUT}	Output Noise	A-weighted (6), Mode 5, BTL input referred	26		µV
PSRR	Power Supply Rejection Ratio $MONO_{OUT}$	V_{RIPPLE} = 200mV_{PP}; f = 217Hz, C_B = 2.2µF, BTL All audio inputs terminated into 50Ω; output referred gain = 6dB (BTL)			
		Output Mode 1, 7	71		dB
		Output Mode 3	68		dB
		Output Mode 5	63		dB
	Power Supply Rejection Ratio R_{OUT} and L_{OUT}	V_{RIPPLE} = 200mV_{PP}; f = 217Hz, C_B = 2.2µF, SE, C_O = 100µF All audio inputs terminated into 50Ω; output referred gain, OCL = 0 (Table 2)			
		Output Mode 2	88		dB
		Output Mode 4	76		dB
		Output Mode 6, 7	76		dB
	Digital Volume Range (R_{IN} and L_{IN})	Input referred maximum attenuation	-54	–53.25 –54.75	dB dB
		Input referred maximum gain	18	17.25 18.75	dB dB
	Mute Attenuation	Output Mode 1, 3, 5	80		dB
	MONO_IN Input Impedance R_{IN} and L_{IN} Input Impedance	Maximum gain setting	11		kΩ kΩ
		Minimum gain setting	100		kΩ kΩ
T_{WU}	Wake-Up Time from Shutdown	C_B = 2.2µF, OCL C_B = 2.2µF, SE	122 184		ms

(1) Human body model, 100pF discharged through a 1.5kΩ resistor.
(2) All voltages are measured with respect to the ground pin, unless otherwise specified.
(3) Typical specifications are specified at +25°C and represent the most likely parametric norm.
(4) Tested limits are specified to Texas Instruments' AOQL (Average Outgoing Quality Level).
(5) Potentially worse case: All three input stages are DC coupled to the BTL output stage.
(6) Datasheet min/max specifications are ensured by design, test, or statistical analysis.

I^2C/SPI (1) (2)

The following specifications apply for V_{DD} = 5.0V and 3.3V, T_A = 25°C unless otherwise specified.

Symbol	Parameter	Conditions	LM4846		Units (Limits)
			Typical (3)	Limits (4) (5)	
t_1	I^2C Clock Period			2.5	µs (max)
t_2	I^2C Clock Setup Time			100	ns (min)
t_3	I^2C Data Hold Time			100	ns (min)
t_4	Start Condition Time			100	ns (min)
t_5	Stop Condition Time			100	ns (min)
f_{SPI}	Maximum SPI Frequency			1000	kHz (max)
t_{EL}	SPI ENB Low Time			100	ns (min)
t_{DS}	SPI Data Setup Time			100	µs (max)
t_{ES}	SPI ENB Setup Time			100	ns (min)
t_{DH}	SPI Data Hold Time			100	ns (min)
t_{EH}	SPI Enable Hold Time			100	ns (min)
t_{CL}	SPI Clock Low Time			500	ns (min)
t_{CH}	SPI Clock High Time			500	ns (min)
t_{CS}	SPI Clock Transition Time			100	ns (min)
V_{IH}	I^2C/SPI Input Voltage High			0.7xI^2CSPI V_{DD}	V (min)
V_{IL}	I^2C/SPI Input Voltage Low			0.3xI^2CSPI V_{DD}	V (max)

(1) Operating Ratings indicate conditions for which the device is functional, but do not ensure specific performance limits. For ensured specifications and test conditions, see the Electrical Characteristics. The ensured specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.
(2) All voltages are measured with respect to the ground pin, unless otherwise specified.
(3) Typical specifications are specified at +25°C and represent the most likely parametric norm.
(4) Tested limits are specified to Texas Instruments' AOQL (Average Outgoing Quality Level).
(5) Potentially worse case: All three input stages are DC coupled to the BTL output stage.

Typical Performance Characteristics

THD+N vs Frequency
V_{DD} = 3.3V, R_L = 8Ω, P_O = 250mW
Mode 1, BTL

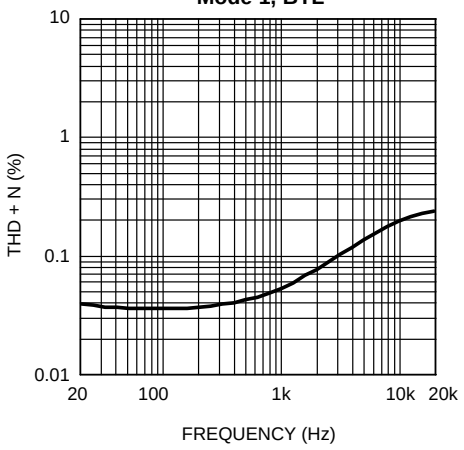


Figure 4.

THD+N vs Frequency
V_{DD} = 3.3V, R_L = 32Ω, P_O = 12mW
Mode 4, OCL

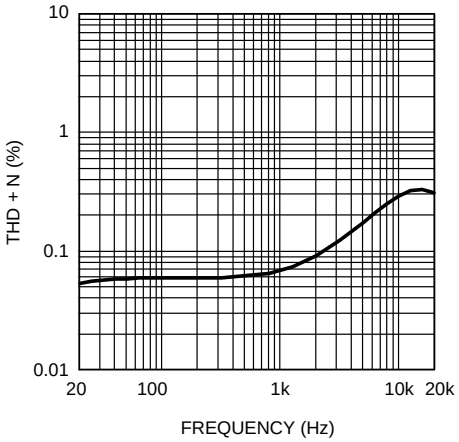


Figure 5.

THD+N vs Frequency
V_{DD} = 3.3V, R_L = 32Ω, P_O = 12mW
Mode 6, OCL

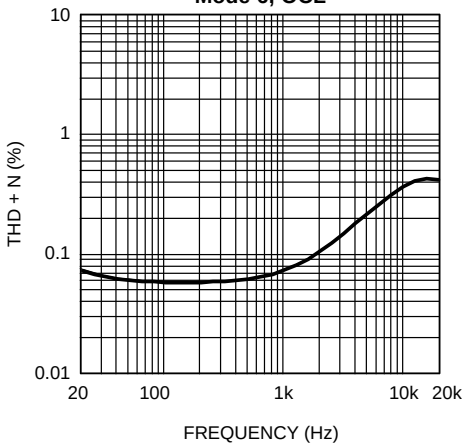


Figure 6.

THD+N vs Frequency
V_{DD} = 3.3V, R_L = 32Ω, P_O = 12mW
Mode 4, SE

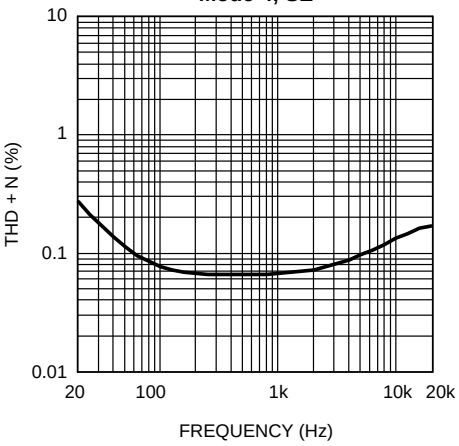


Figure 7.

THD+N vs Frequency
V_{DD} = 3.3V, R_L = 32Ω, P_O = 12mW
Mode 6, SE

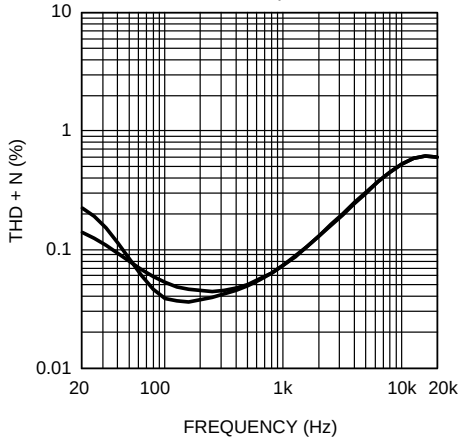


Figure 8.

THD+N vs Frequency
V_{DD} = 3.3V, R_L = 8Ω, P_O = 250mW
Mode 5

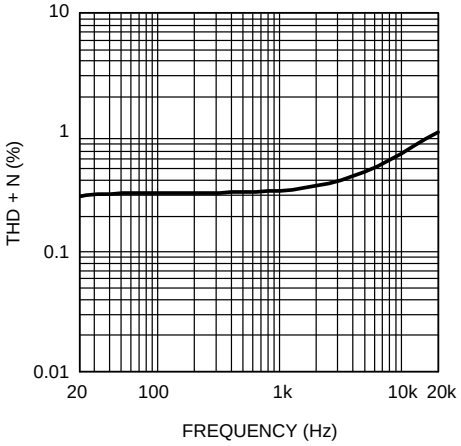


Figure 9.

Typical Performance Characteristics (continued)

THD+N vs Frequency
V_{DD} = 5V, R_L = 8Ω, P_O = 500mW
Mode 1, BTL

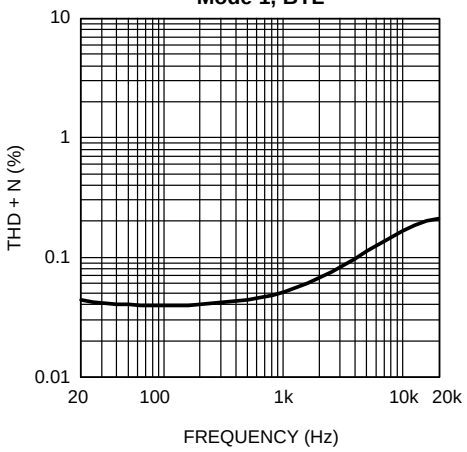


Figure 10.

THD+N vs Frequency
V_{DD} = 5V, R_L = 32Ω, P_O = 30mW
Mode 4, OCL

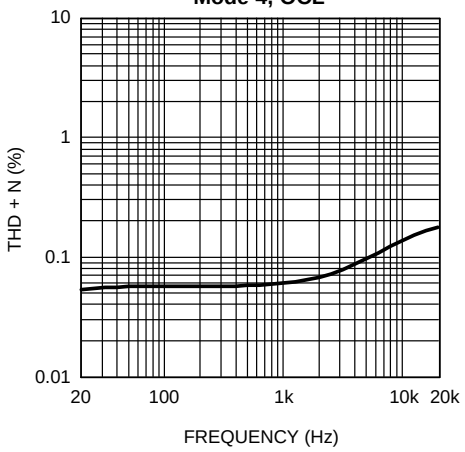


Figure 11.

THD+N vs Frequency
V_{DD} = 5V, R_L = 32Ω, P_O = 30mW
Mode 4, SE

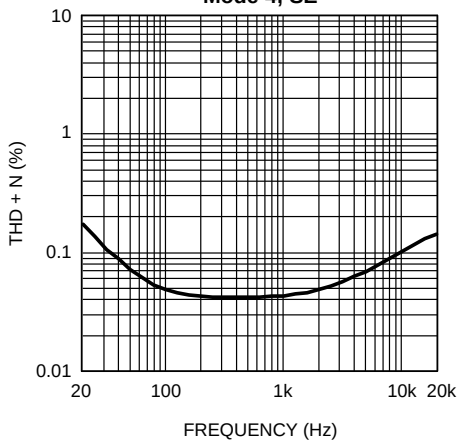


Figure 12.

THD+N vs Frequency
V_{DD} = 5V, R_L = 32Ω, P_O = 30mW
Mode 6, OCL

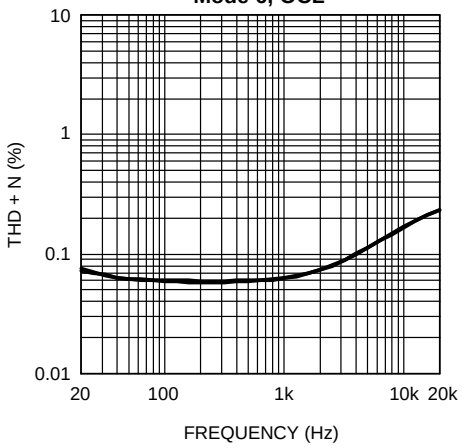


Figure 13.

THD+N vs Frequency
V_{DD} = 5V, R_L = 32Ω, P_O = 30mW
Mode 6, SE

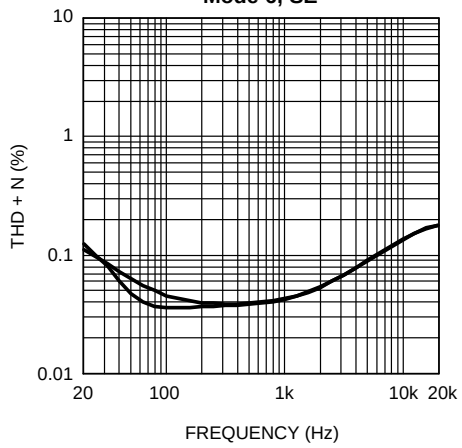


Figure 14.

THD+N vs Frequency
V_{DD} = 5V, R_L = 8Ω, P_O = 500mW
Mode 5

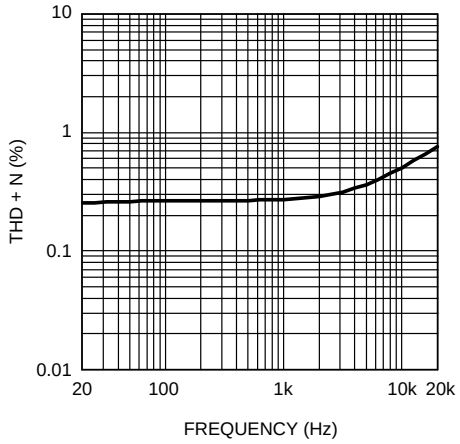


Figure 15.

Typical Performance Characteristics (continued)

THD+N vs Output Power
V_{DD} = 3.3V, R_L = 8Ω, f = 1kHz
Mode 1, BTL

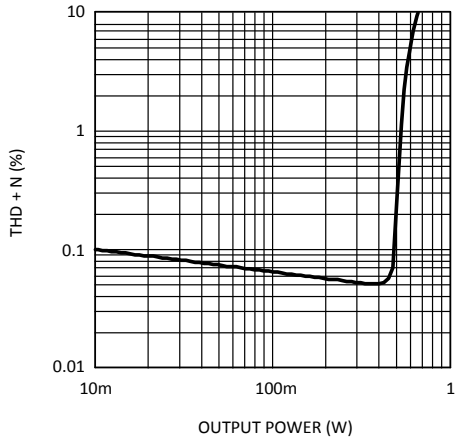


Figure 16.

THD+N vs Output Power
V_{DD} = 3.3V, R_L = 8Ω, f = 1kHz
Mode 5, BTL

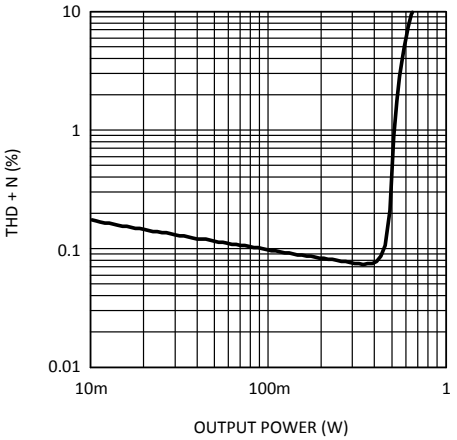


Figure 17.

THD+N vs Output Power
V_{DD} = 3.3V, R_L = 32Ω, f = 1kHz
Mode 4, OCL

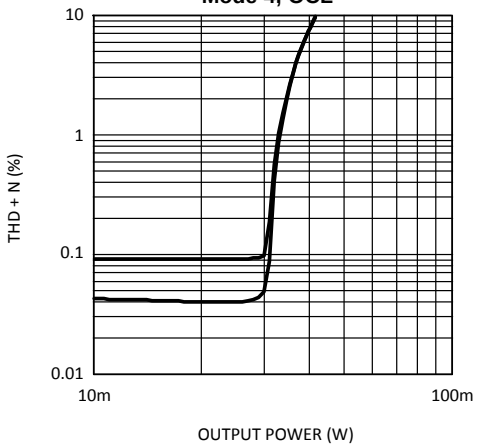


Figure 18.

THD+N vs Output Power
V_{DD} = 3.3V, R_L = 32Ω, f = 1kHz
Mode 4, SE

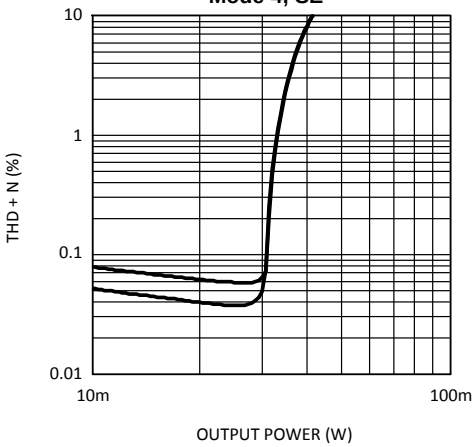


Figure 19.

THD+N vs Output Power
V_{DD} = 3.3V, R_L = 32Ω, f = 1kHz
Mode 6, OCL

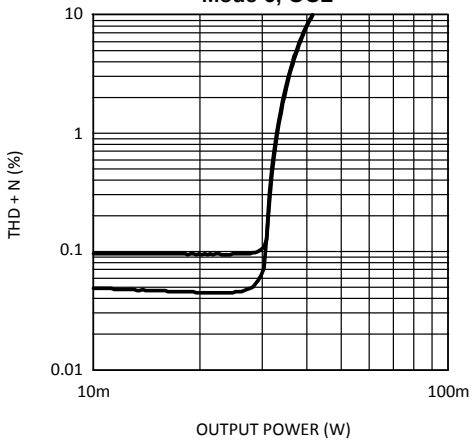


Figure 20.

THD+N vs Output Power
V_{DD} = 3.3V, R_L = 32Ω, f = 1kHz
Mode 6, SE

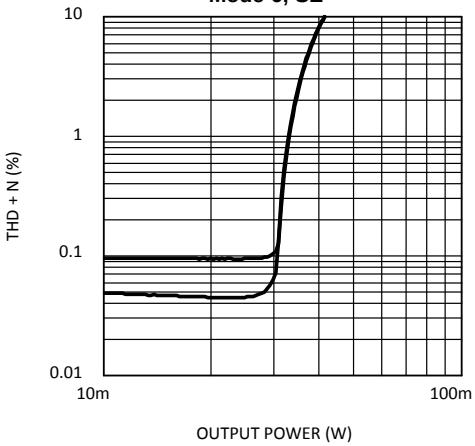


Figure 21.

Typical Performance Characteristics (continued)

THD+N vs Output Power
V_{DD} = 5V, R_L = 8Ω, f = 1kHz
Mode 1, BTL

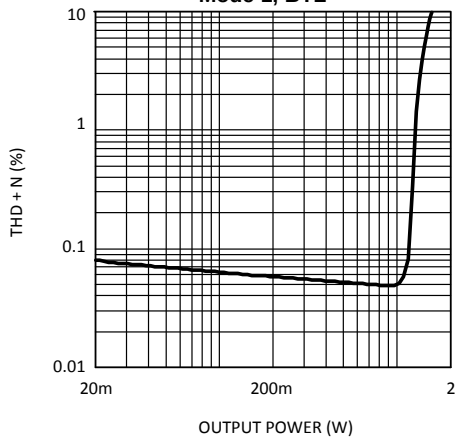


Figure 22.

THD+N vs Output Power
V_{DD} = 5V, R_L = 8Ω, f = 1kHz
Mode 5, BTL

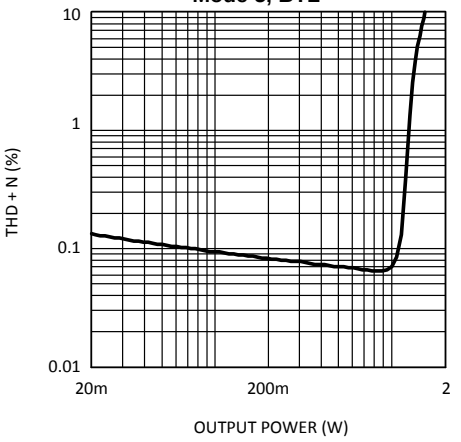


Figure 23.

THD+N vs Output Power
V_{DD} = 5V, R_L = 32Ω, f = 1kHz
Mode 4, OCL

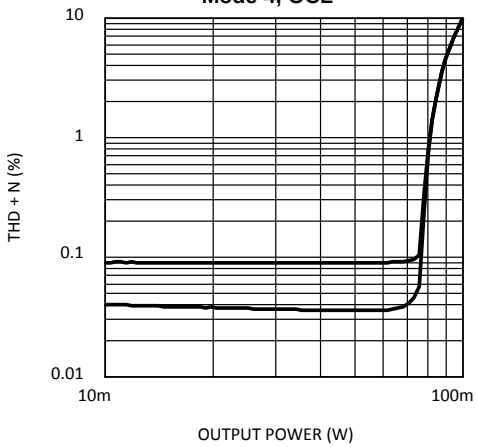


Figure 24.

THD+N vs Output Power
V_{DD} = 5V, R_L = 32Ω, f = 1kHz
Mode 4, SE

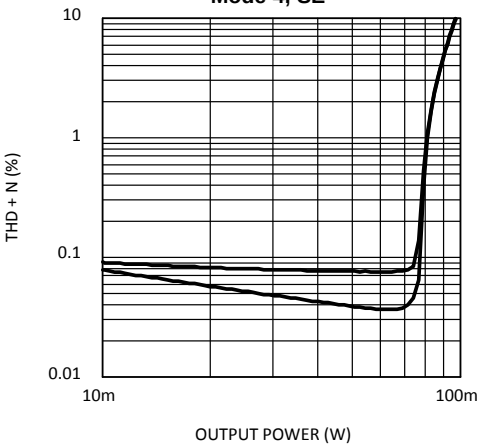


Figure 25.

THD+N vs Output Power
V_{DD} = 5V, R_L = 32Ω, f = 1kHz
Mode 6, OCL

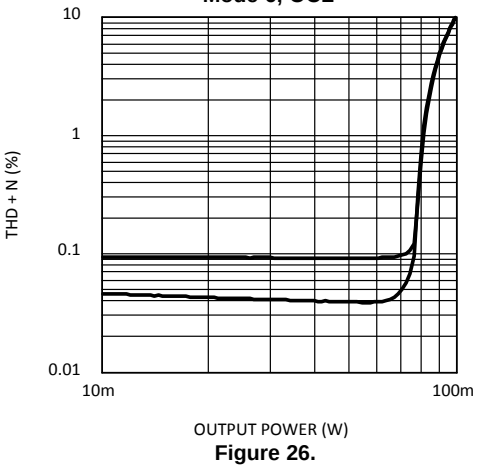


Figure 26.

THD+N vs Output Power
V_{DD} = 5V, R_L = 32Ω, f = 1kHz
Mode 6, SE

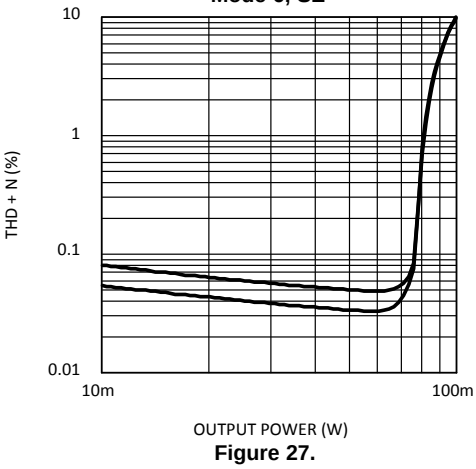


Figure 27.

Typical Performance Characteristics (continued)

PSRR vs Frequency
V_{DD} = 3.3V, 0dB
Mode 4, OCL

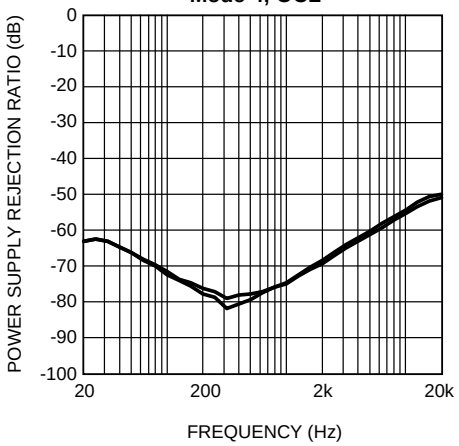


Figure 28.

PSRR vs Frequency
V_{DD} = 3.3V, 0dB
Mode 4, SE

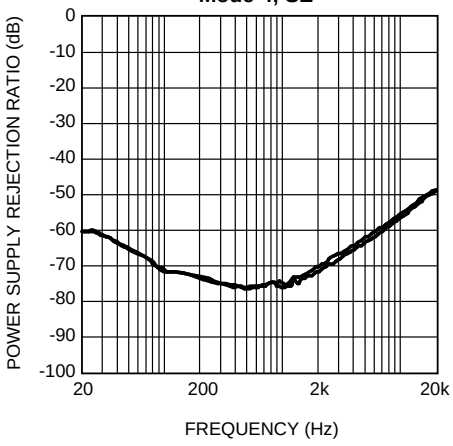


Figure 29.

PSRR vs Frequency
V_{DD} = 3.3V, 0dB
Mode 6, OCL

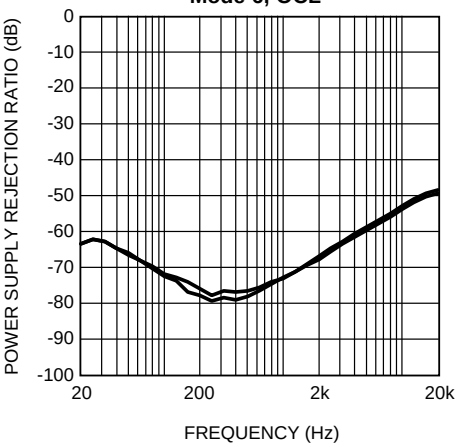


Figure 30.

PSRR vs Frequency
V_{DD} = 3.3V, 0dB
Mode 6, SE

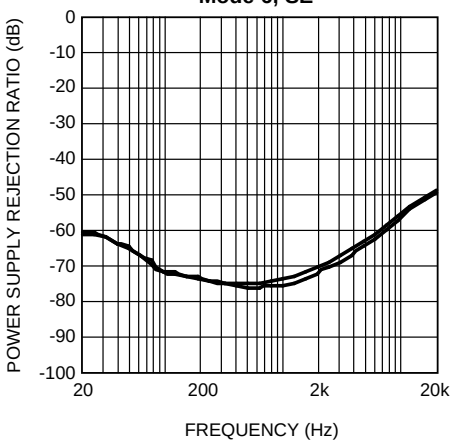


Figure 31.

PSRR vs Frequency
V_{DD} = 3.3V, 6dB
Mode 1, BTL

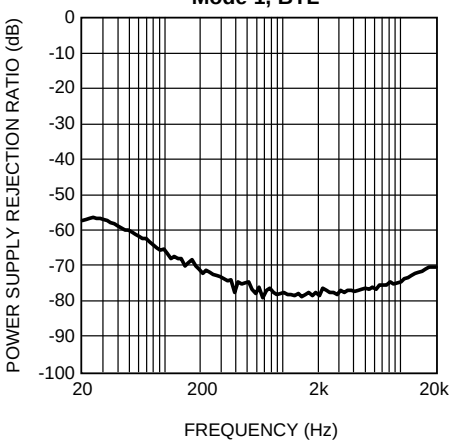


Figure 32.

PSRR vs Frequency
V_{DD} = 3.3V, 6dB
Mode 5, BTL

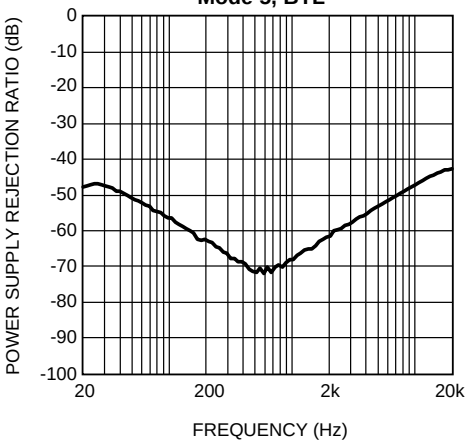


Figure 33.

Typical Performance Characteristics (continued)

Noise
V_{DD} = 3.3V, Mode 4, OCL

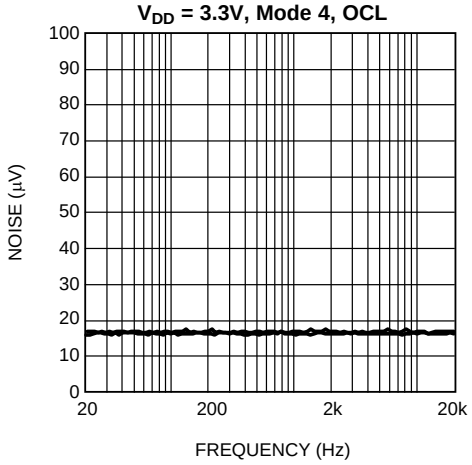


Figure 34.

Noise
V_{DD} = 3.3V, Mode 4, SE

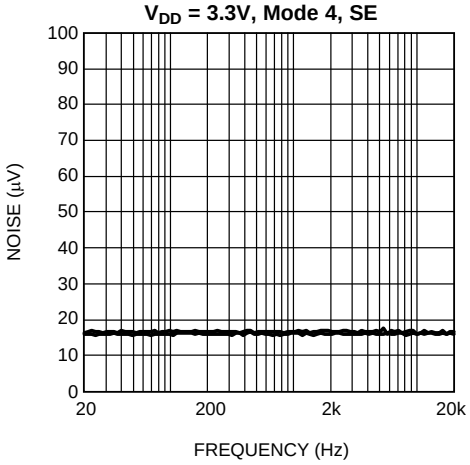


Figure 35.

Noise
V_{DD} = 3.3V, Mode 6, SE

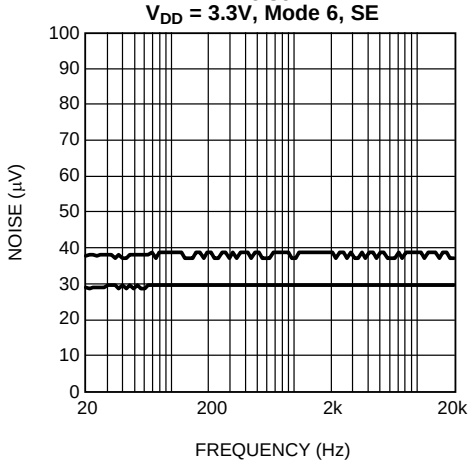


Figure 36.

Noise
V_{DD} = 3.3V, Mode 5, BTL

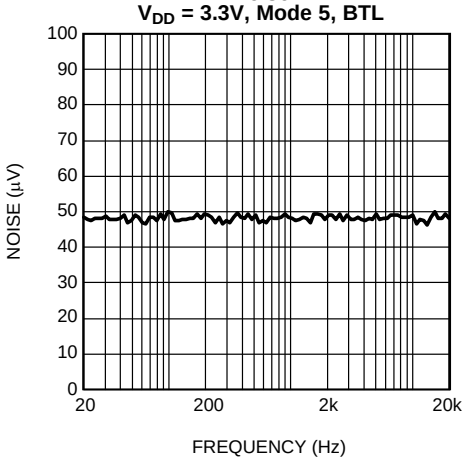


Figure 37.

Noise
V_{DD} = 3.3V, Mode 1, BTL

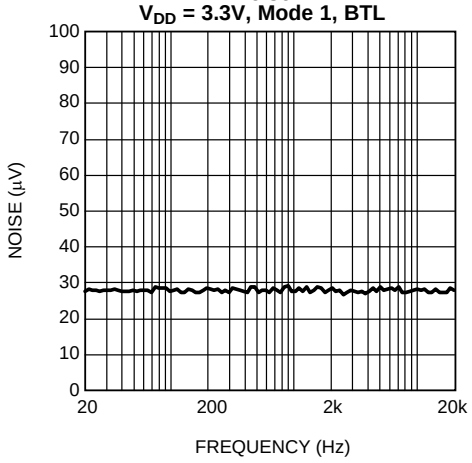


Figure 38.

Power Dissipation vs Output Power
V_{DD} = 3.3V, R_L = 8Ω
f = 1kHz, Mode 1, BTL

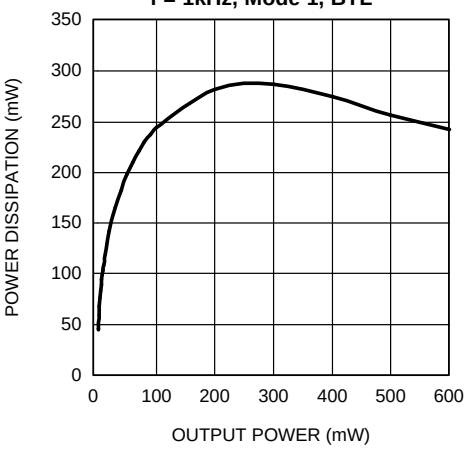


Figure 39.

Typical Performance Characteristics (continued)

Power Dissipation vs Output Power
V_{DD} = 3.3V, R_L = 8Ω
f = 1kHz, BTL, Mode 5

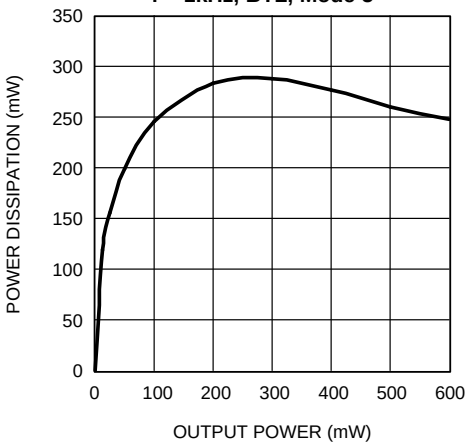


Figure 40.

Power Dissipation vs Output Power
V_{DD} = 3.3V, R_L = 32Ω
f = 1kHz, OCL, Mode 4

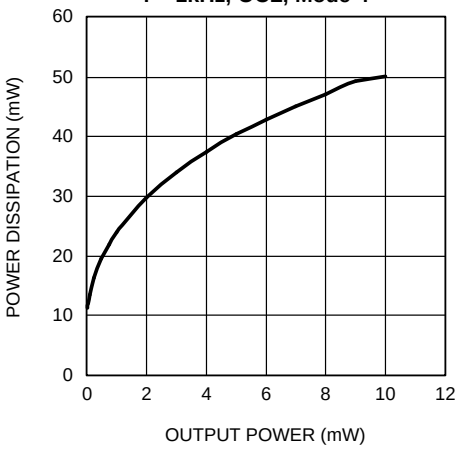


Figure 41.

Power Dissipation vs Output Power
V_{DD} = 3.3V, R_L = 32Ω
f = 1kHz, OCL, Mode 6

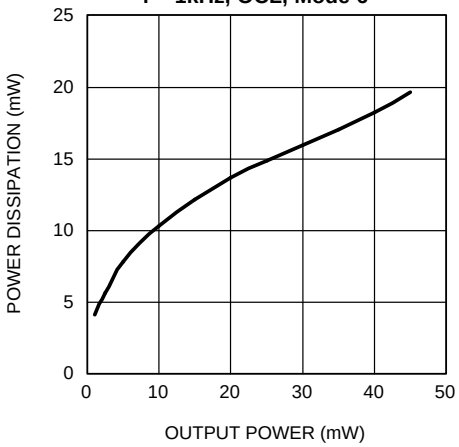


Figure 42.

Power Dissipation vs Output Power
V_{DD} = 3.3V, R_L = 32Ω
f = 1kHz, SE, Mode 4

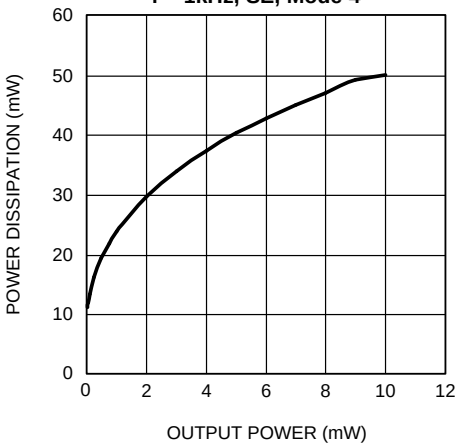


Figure 43.

Power Dissipation vs Output Power
V_{DD} = 3.3V, R_L = 32Ω
f = 1kHz, SE, Mode 6

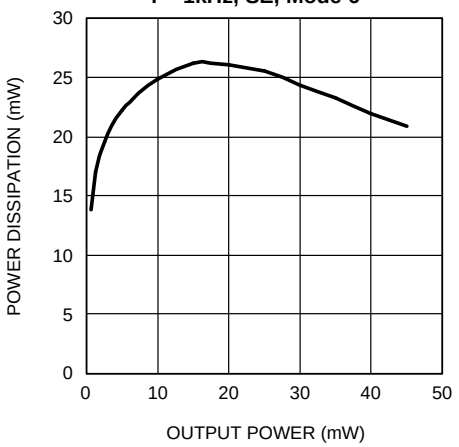


Figure 44.

Power Dissipation vs Output Power
V_{DD} = 5V, R_L = 8Ω
f = 1kHz, BTL, Mode 1

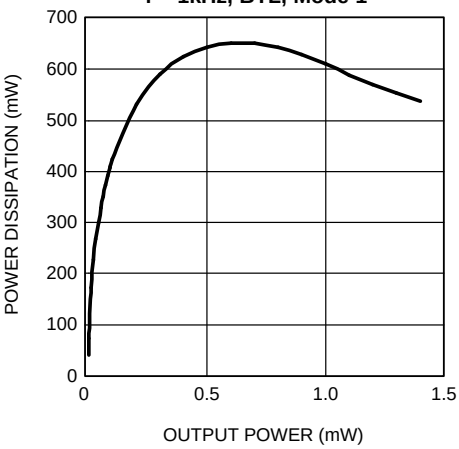


Figure 45.

Typical Performance Characteristics (continued)

Power Dissipation vs Output Power
V_{DD} = 5V, R_L = 8Ω
f = 1kHz, BTL, Mode 5

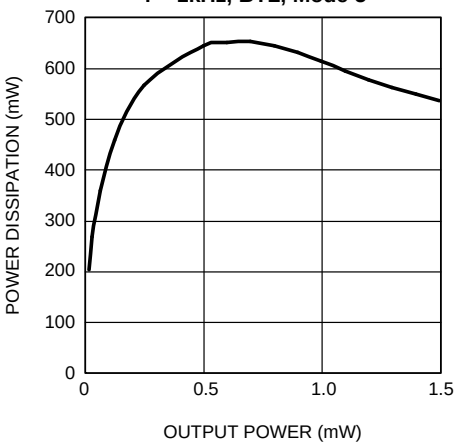


Figure 46.

Power Dissipation vs Output Power
V_{DD} = 5V, R_L = 32Ω
f = 1kHz, OCL, Mode 4

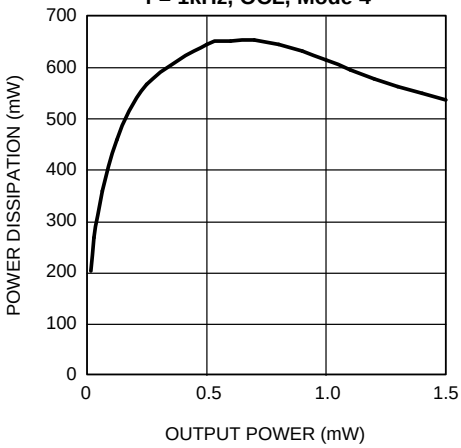


Figure 47.

Power Dissipation vs Output Power
V_{DD} = 5V, R_L = 32Ω
f = 1kHz, OCL, Mode 6

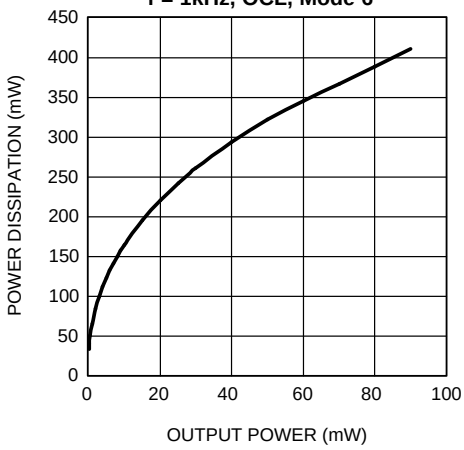


Figure 48.

Power Dissipation vs Output Power
V_{DD} = 5V, R_L = 32Ω
f = 1kHz, SE, Mode 4

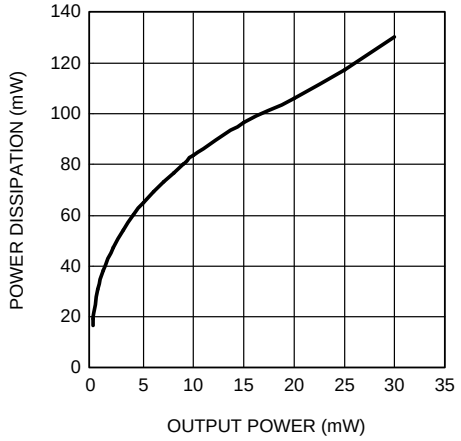


Figure 49.

Power Dissipation vs Output Power
V_{DD} = 5V, R_L = 32Ω
f = 1kHz, SE, Mode 6

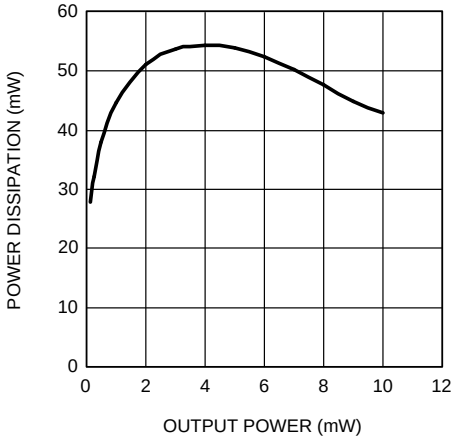


Figure 50.

Crosstalk vs Frequency
V_{DD} = 3.3V, R_L = 32Ω, P_O = 12mW
Right-Left, OCL, Mode 4

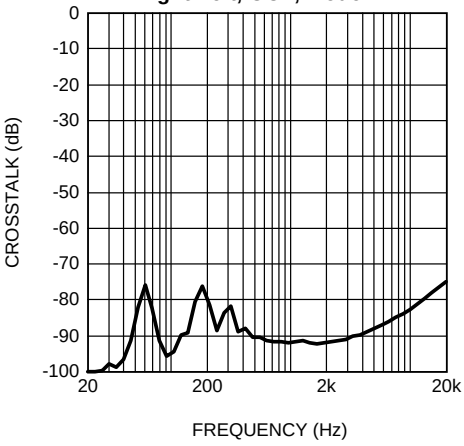


Figure 51.

Typical Performance Characteristics (continued)

Crosstalk vs Frequency
V_{DD} = 3.3V, R_L = 32Ω, P_O = 12mW
Right-Left, OCL, Mode 6

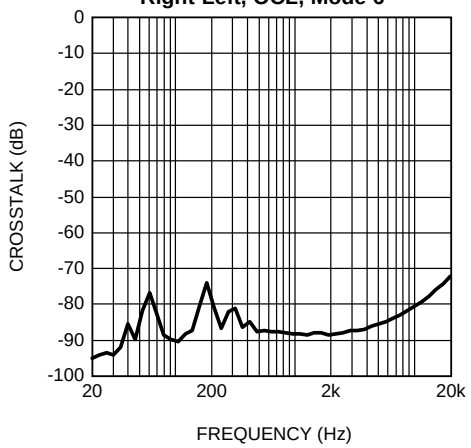


Figure 52.

Crosstalk vs Frequency
V_{DD} = 3.3V, R_L = 32Ω, P_O = 12mW
Right-Left, SE, Mode 4

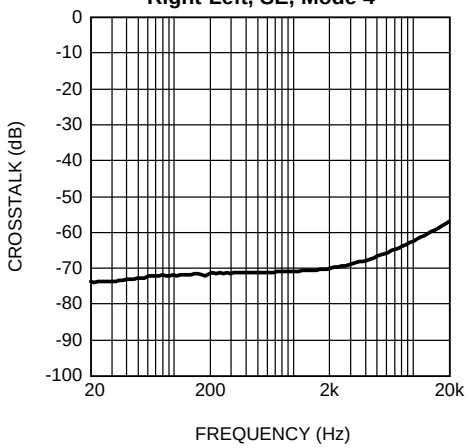


Figure 53.

Crosstalk vs Frequency
V_{DD} = 3.3V, R_L = 32Ω, P_O = 12mW
Right-Left, SE, Mode 6

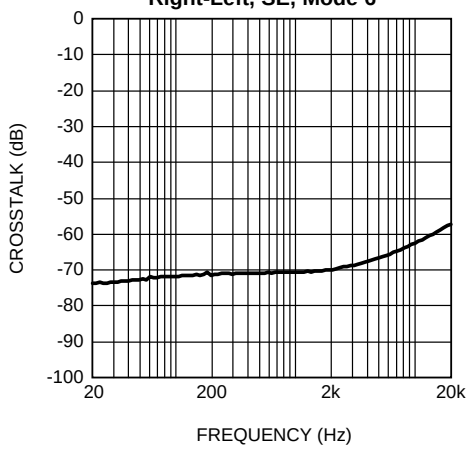


Figure 54.

Supply Current vs Supply Voltage
R_L = 8Ω, Mode 1

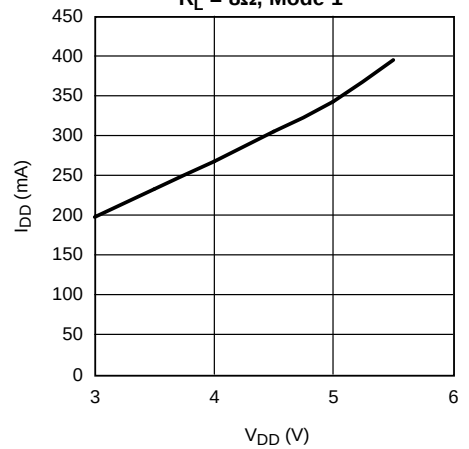


Figure 55.

Supply Current vs Supply Voltage
R_L = 8Ω, Mode 5

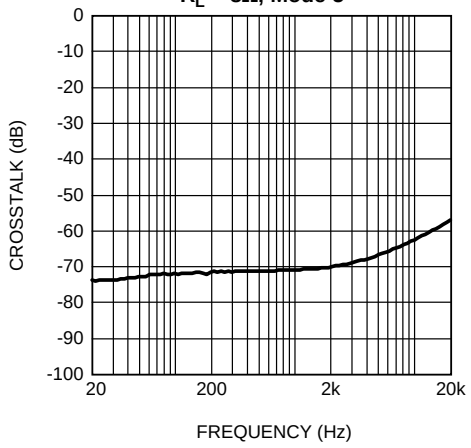


Figure 56.

Supply Current vs Supply Voltage
R_L = 32Ω, OCL, Mode 4

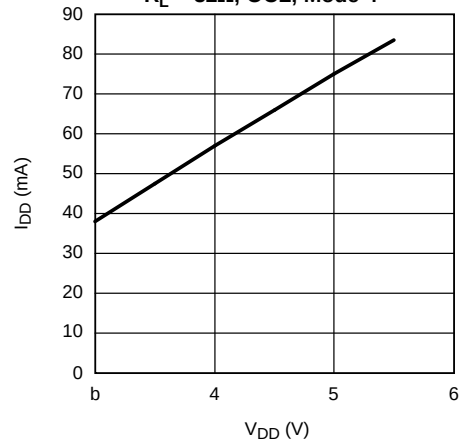


Figure 57.

Typical Performance Characteristics (continued)

Supply Current vs Supply Voltage
R_L = 32Ω, OCL, Mode 6

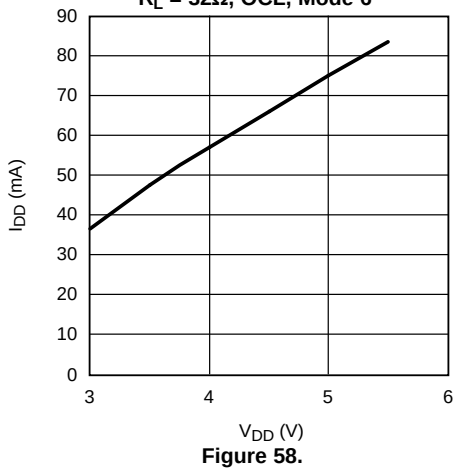


Figure 58.

Supply Current vs Supply Voltage
R_L = 32Ω, SE, Mode 4

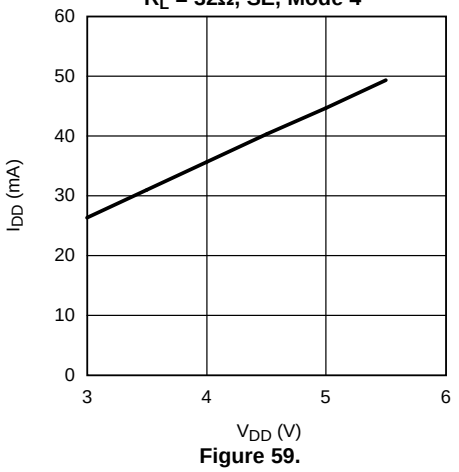


Figure 59.

Supply Current vs Supply Voltage
R_L = 32Ω, SE, Mode 6

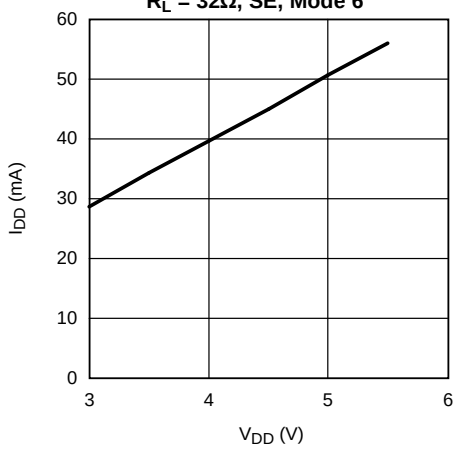


Figure 60.

Output Power vs Supply Voltage
R_L = 8Ω, Mode 1

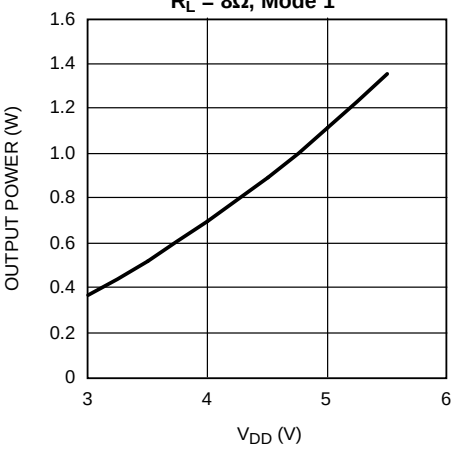


Figure 61.

Output Power vs Supply Voltage
R_L = 8Ω, Mode 5

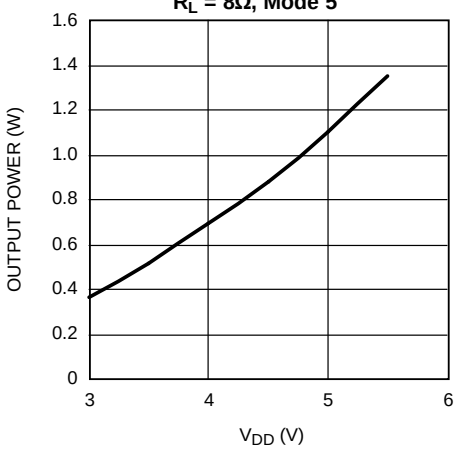


Figure 62.

Output Power vs Supply Voltage
R_L = 32Ω, Mode 4

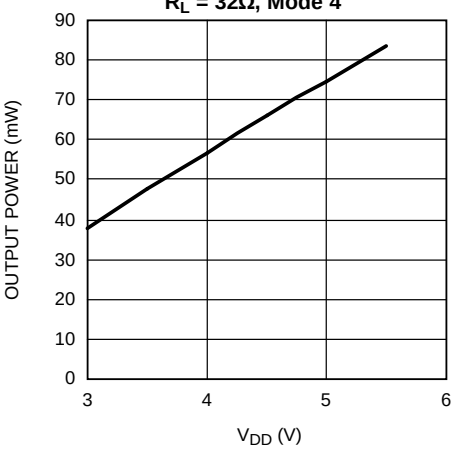


Figure 63.

Typical Performance Characteristics (continued)

Output Power vs Supply Voltage
R_L = 32Ω, OCL, Mode 6

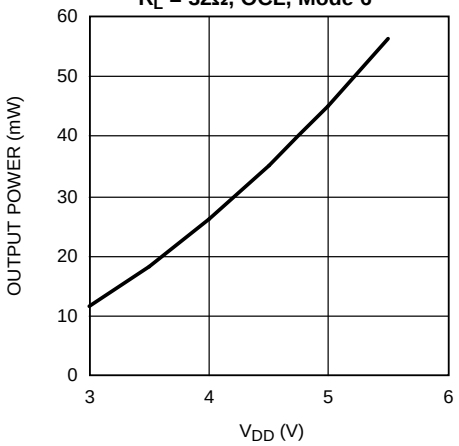


Figure 64.

Output Power vs Supply Voltage
R_L = 32Ω, SE, Mode 4

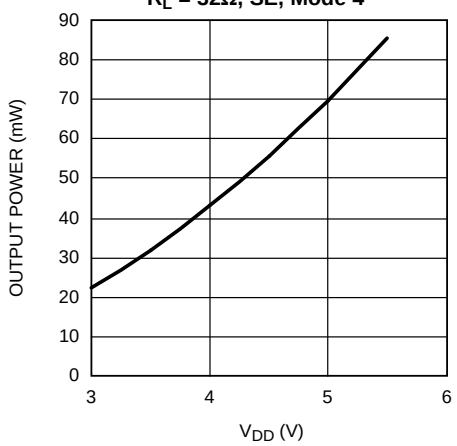


Figure 65.

Output Power vs Supply Voltage
R_L = 32Ω, SE, Mode 6

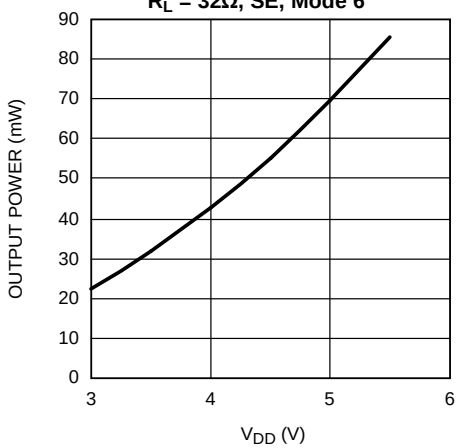


Figure 66.

APPLICATION INFORMATION

I^2C PIN DESCRIPTION

SDA: This is the serial data input pin.

SCL: This is the clock input pin.

ID_ENB: This is the address select input pin.

I^2CSPI_SEL: This is tied LOW for I^2C mode.

I^2C COMPATIBLE INTERFACE

The LM4846 uses a serial bus which conforms to the I^2C protocol to control the chip's functions with two wires: clock (SCL) and data (SDA). The clock line is uni-directional. The data line is bi-directional (open-collector). The maximum clock frequency specified by the I^2C standard is 400kHz. In this discussion, the master is the controlling microcontroller and the slave is the LM4846.

The I^2C address for the LM4846 is determined using the ID_ENB pin. The LM4846's two possible I^2C chip addresses are of the form $111110X_10$ (binary), where X_1 = 0, if ID_ENB is logic LOW; and X_1 = 1, if ID_ENB is logic HIGH. If the I^2C interface is used to address a number of chips in a system, the LM4846's chip address can be changed to avoid any possible address conflicts.

The bus format for the I^2C interface is shown in Figure 67. The bus format diagram is broken up into six major sections:

The "start" signal is generated by lowering the data signal while the clock signal is HIGH. The start signal will alert all devices attached to the I^2C bus to check the incoming address against their own address.

The 8-bit chip address is sent next, most significant bit first. The data is latched in on the rising edge of the clock. Each address bit must be stable while the clock level is HIGH.

For I^2C interface operation, the I^2CSPI_SEL pin needs to be tied LOW (and tied high for SPI operation).

After the last bit of the address bit is sent, the master releases the data line HIGH (through a pull-up resistor). Then the master sends an acknowledge clock pulse. If the LM4846 has received the address correctly, then it holds the data line LOW during the clock pulse. If the data line is not held LOW during the acknowledge clock pulse, then the master should abort the rest of the data transfer to the LM4846.

The 8 bits of data are sent next, most significant bit first. Each data bit should be valid while the clock level is stable HIGH.

After the data byte is sent, the master must check for another acknowledge to see if the LM4846 received the data.

If the master has more data bytes to send to the LM4846, then the master can repeat the previous two steps until all data bytes have been sent.

The "stop" signal ends the transfer. To signal "stop", the data signal goes HIGH while the clock signal is HIGH. The data line should be held HIGH when not in use.

I^2C INTERFACE POWER SUPPLY PIN (I^2CV_{DD})

The LM4846's I^2C interface is powered up through the I^2CV_{DD} pin. The LM4846's I^2C interface operates at a voltage level set by the I^2CV_{DD} pin which can be set independent to that of the main power supply pin V_{DD}. This is ideal whenever logic levels for the I^2C interface are dictated by a microcontroller or microprocessor that is operating at a lower supply voltage than the main battery of a portable system.

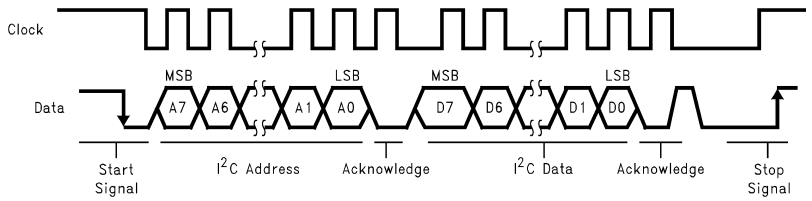


Figure 67. I²C Bus Format

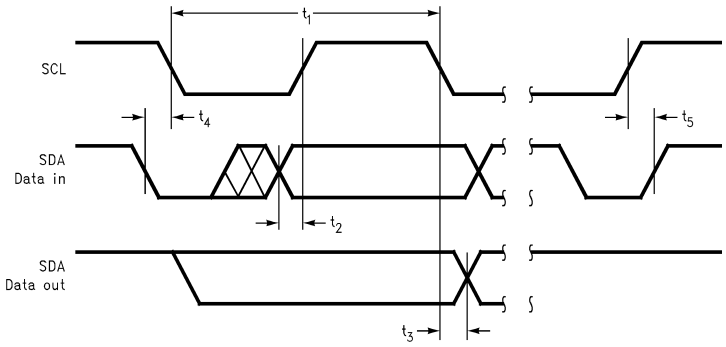


Figure 68. I²C Timing Diagram

SPI DESCRIPTION

0. I²CSPI_SEL: This pin is tied HIGH for SPI mode.

1. The data bits are transmitted with the MSB first.

2. The maximum clock rate is 1MHz for the CLK pin.

3. CLK must remain HIGH for at least 500ns (t_{CH}) after the rising edge of CLK, and CLK must remain LOW for at least 500ns (t_{CL}) after the falling edge of CLK.

4. The serial data bits are sampled at the rising edge of CLK. Any transition on DATA must occur at least 100ns (t_{DS}) before the rising edge of CLK. Also, any transition on DATA must occur at least 100ns (t_{DH}) after the rising edge of CLK and stabilize before the next rising edge of CLK.

5.ID_ENB should be LOW only during serial data transmission.

6. ID_ENB must be LOW at least 100ns (t_{ES}) before the first rising edge of CLK, and ID_ENB has to remain LOW at least 100ns (t_{EH}) after the eighth rising edge of CLK.

7. If ID_ENB remains HIGH for more than 100ns before all 8 bits are transmitted then the data latch will be aborted.

8. If ID_ENB is LOW for more than 8 CLK pulses then only the first 8 data bits will be latched and activated when ID_ENB transitions to logic-high.

9. ID_ENB must remain HIGH for at least 100ns (t_{EL}) to latch in the data.

10. Coincidental rising or falling edges of CLK and ID_ENB are not allowed. If CLK is to be held HIGH after the data transmission, the falling edge of CLK must occur at least 100ns (t_{CS}) before ID_ENB transitions to LOW for the next set of data.

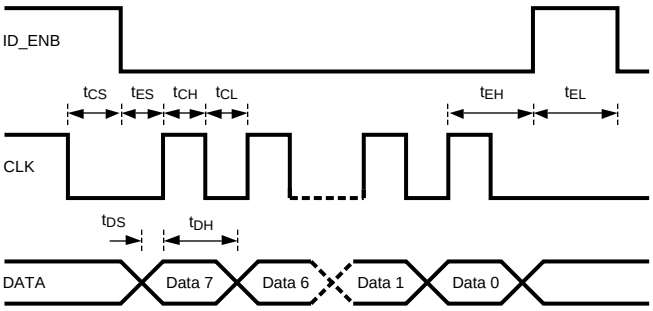


Figure 69. SPI Timing Diagram

Table 1. Chip Address

	A7	A6	A5	A4	A3	A2	A1	A0
Chip Address	1	1	1	1	1	0	EC	0
ID_ENB = 0	1	1	1	1	1	0	0	0
ID_ENB = 1	1	1	1	1	1	0	1	0

Table 2. Control Registers(1)

	D7	D6	D5	D4	D3	D2	D1	D0
Mode Control	0	0	0	0	OCL	MC2	MC1	MC0
Programmable 3D	0	1	0	0	N3D3	N3D2	N3D1	N3D0
Mono Volume Control	1	0	0	MVC4	MVC3	MVC2	MVC1	MVC0
Left Volume Control	1	1	0	LVC4	LVC3	LVC2	LVC1	LVC0
Right Volume Control	1	1	1	RVC4	RVC3	RVC2	RVC1	RVC0

(1) 1. Bits MVC0 — MVC4 control 32 step volume control for MONO input
2. Bits LVC0 — LVC4 control 32 step volume control for LEFT input
3. Bits RVC0 — RVC4 control 32 step volume control for RIGHT input
4. Bits MC0 — MC2 control 8 distinct modes
5. Bits N3D3, N3D2, N3D1, N3D0 control programmable 3D function
6. N3D0 turns the 3D function ON (N3D0 = 1) or OFF (N3D0 = 0), and N3D1 = 0 provides a “wider” aural effect or N3D1 = 1 a “narrower” aural effect
7. Bit OCL selects between SE with output capacitor (OCL = 0) or SE without output capacitors (OCL = 1). **Default is OCL = 0**
8. N3D1 selects between two different 3D configurations

Table 3. Programmable Texas Instruments 3D Audio

	N3D3	N3D2
Low	0	0
Medium	0	1
High	1	0
Maximum	1	1

Table 4. Output Mode Selection(1)

Output Mode Number	MC2	MC1	MC0	Handsfree Speaker Output	Right HP Output	Left HP Output
0	0	0	0	SD	SD	SD
1	0	0	1	2 x G_P x P	MUTE	MUTE
2	0	1	0	SD	G_P x P	G_P x P
3	0	1	1	2 x (G_L x L + G_R x R)	MUTE	MUTE
4	1	0	0	SD	G_R x R	G_L x L
5	1	0	1	2 x (G_L x L + G_R x R + G_P x P)	MUTE	MUTE
6	1	1	0	SD	G_R x R + G_P x P	G_L x L + G_P x P
7	1	1	1	2 x (G_R x R + G_L x L)	G_R x R	G_L x L

(1) On initial POWER ON, the default mode is 000
P = Phone in
R = R_{IN}
L = L_{IN}
SD = Shutdown
MUTE = Mute Mode
G_P = Phone In (Mono) volume control gain
G_R = Right stereo volume control gain
G_L = Left stereo volume control gain

Table 5. Volume Control Table(1)

Volume Step	xVC4	xVC3	xVC2	xVC1	xVC0	Headphone Gain, dB	Speaker Gain, dB (BTL)
1	0	0	0	0	0	–54.00	–48.00
2	0	0	0	0	1	–46.50	–40.50
3	0	0	0	1	0	–40.50	–34.50
4	0	0	0	1	1	–34.50	–28.50
5	0	0	1	0	0	–30.00	–24.00
6	0	0	1	0	1	–27.00	–21.00
7	0	0	1	1	0	–24.00	–18.00
8	0	0	1	1	1	–21.00	–15.00
9	0	1	0	0	0	–18.00	–12.00
10	0	1	0	0	1	–15.00	–9.00
11	0	1	0	1	0	–13.50	–7.50
12	0	1	0	1	1	–12.00	–6.00
13	0	1	1	0	0	–10.50	–4.50
14	0	1	1	0	1	–9.00	–3.00
15	0	1	1	1	0	–7.50	–1.50
16	0	1	1	1	1	–6.00	0.00
17	1	0	0	0	0	–4.50	1.50
18	1	0	0	0	1	–3.00	3.00
19	1	0	0	1	0	–1.50	4.50
20	1	0	0	1	1	0.00	6.00
21	1	0	1	0	0	1.50	7.50
22	1	0	1	0	1	3.00	9.00
23	1	0	1	1	0	4.50	10.50
24	1	0	1	1	1	6.00	12.00

(1) 1. x = M, L, or R
2. Gain / Attenuation is from input to output

Table 5. Volume Control Table(1) (continued)

Volume Step	xVC4	xVC3	xVC2	xVC1	xVC0	Headphone Gain, dB	Speaker Gain, dB (BTL)
25	1	1	0	0	0	7.50	13.50
26	1	1	0	0	1	9.00	15.00
27	1	1	0	1	0	10.50	16.50
28	1	1	0	1	1	12.00	18.00
29	1	1	1	0	0	13.50	19.50
30	1	1	1	0	1	15.00	21.00
31	1	1	1	1	0	16.50	22.50
32	1	1	1	1	1	18.00	24.00

TEXAS INSTRUMENTS 3D ENHANCEMENT

The LM4846 features a stereo headphone, 3D audio enhancement effect that widens the perceived soundstage from a stereo audio signal. The 3D audio enhancement creates a perceived spatial effect optimized for stereo headphone listening. The LM4846 can be programmed for a “narrow” or “wide” soundstage perception. The narrow soundstage has a more focused approaching sound direction, while the wide soundstage has a spatial, theater-like effect. Within each of these two modes, four discrete levels of 3D effect that can be programmed: low, medium, high, and maximum (Table 2), each level with an ever increasing aural effect, respectively. The difference between each level is 3dB.

The external capacitors, shown in Figure 70, are required to enable the 3D effect. The value of the capacitors set the cutoff frequency of the 3D effect, as shown by Equation 1 and Equation 2. Note that the internal 20kΩ resistor is nominal (±25%).

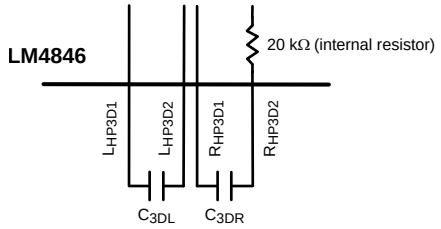


Figure 70. External 3D Effect Capacitors

$$f_{3DL(-3dB)} = 1 / 2\pi * 20k\Omega * C_{3DL} \quad (1)$$

$$f_{3DR(-3dB)} = 1 / 2\pi * 20k\Omega * C_{3DR} \quad (2)$$

Optional resistors R_{3DL} and R_{3DR} can also be added (Figure 71) to affect the -3dB frequency and 3D magnitude.

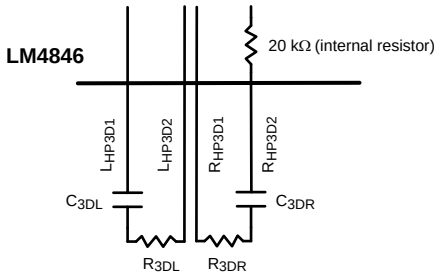


Figure 71. External RC Network with Optional R_{3DL} and R_{3DR} Resistors

$$f_{3DL(-3dB)} = 1 / 2\pi * (20k\Omega + R_{3DL}) * C_{3DL} \quad (3)$$

$$f_{3DR(-3dB)} = 1 / 2\pi * 20k\Omega + R_{3DR}) * C_{3DR} \quad (4)$$

ΔAV (change in AC gain) = 1 / 1 + M, where M represents some ratio of the nominal internal resistor, 20kΩ (see example below).

$$f_{3dB}\ (3D) = 1 / 2\pi\ (1 + M)(20k\Omega * C_{3D}) \quad (5)$$

$$C_{Equivalent}\ (new) = C_{3D} / 1 + M \quad (6)$$

Table 6. Pole Locations

R_{3D} (kΩ) (optional)	C_{3D} (nF)	M	ΔAV (dB)	f-3dB (3D) (Hz)	Value of C_{3D} to keep same pole location (nF)	new Pole Location (Hz)
0	68	0	0	117		
1	68	0.05	–0.4	111	64.8	117
5	68	0.25	–1.9	94	54.4	117
10	68	0.50	–3.5	78	45.3	117
20	68	1.00	–6.0	59	34.0	117

PCB LAYOUT AND SUPPLY REGULATION CONSIDERATIONS FOR DRIVING 8Ω LOAD

Power dissipated by a load is a function of the voltage swing across the load and the load's impedance. As load impedance decreases, load dissipation becomes increasingly dependent on the interconnect (PCB trace and wire) resistance between the amplifier output pins and the load's connections. Residual trace resistance causes a voltage drop, which results in power dissipated in the trace and not in the load as desired. For example, 0.1Ω trace resistance reduces the output power dissipated by an 8Ω load from 158.3mW to 156.4mW. The problem of decreased load dissipation is exacerbated as load impedance decreases. Therefore, to maintain the highest load dissipation and widest output voltage swing, PCB traces that connect the output pins to a load must be as wide as possible.

Poor power supply regulation adversely affects maximum output power. A poorly regulated supply's output voltage decreases with increasing load current. Reduced supply voltage causes decreased headroom, output signal clipping, and reduced output power. Even with tightly regulated supplies, trace resistance creates the same effects as poor supply regulation. Therefore, making the power supply traces as wide as possible helps maintain full output voltage swing.

BRIDGE CONFIGURATION EXPLANATION

The LM4846 drives a load, such as a speaker, connected between outputs, MONO+ and MONO-.

This results in both amplifiers producing signals identical in magnitude, but 180° out of phase. Taking advantage of this phase difference, a load is placed between MONO- and MONO+ and driven differentially (commonly referred to as ”bridge mode”). This results in a differential or BTL gain of:

$$A_{VD} = 2(R_f / R_i) = 2 \quad (7)$$

Bridge mode amplifiers are different from single-ended amplifiers that drive loads connected between a single amplifier's output and ground. For a given supply voltage, bridge mode has a distinct advantage over the single-ended configuration: its differential output doubles the voltage swing across the load. Theoretically, this produces four times the output power when compared to a single-ended amplifier under the same conditions. This increase in attainable output power assumes that the amplifier is not current limited and that the output signal is not clipped.

Another advantage of the differential bridge output is no net DC voltage across the load. This is accomplished by biasing MONO- and MONO+ outputs at half-supply. This eliminates the coupling capacitor that single supply, single-ended amplifiers require. Eliminating an output coupling capacitor in a typical single-ended configuration forces a single-supply amplifier's half-supply bias voltage across the load. This increases internal IC power dissipation and may permanently damage loads such as speakers.

POWER DISSIPATION

Power dissipation is a major concern when designing a successful single-ended or bridged amplifier.

A direct consequence of the increased power delivered to the load by a bridge amplifier is higher internal power dissipation. The LM4846 has a pair of bridged-tied amplifiers driving a handsfree speaker, MONO. The maximum internal power dissipation operating in the bridge mode is twice that of a single-ended amplifier. From Equation 8, assuming a 5V power supply and an 8Ω load, the maximum MONO power dissipation is 634mW.

$$P_{DMAX\text{-}SPKROUT} = 4(V_{DD})^2 / (2\pi^2 R_L)\text{: Bridge Mode} \quad (8)$$

The LM4846 also has a pair of single-ended amplifiers driving stereo headphones, R_{OUT} and L_{OUT}. The maximum internal power dissipation for R_{OUT} and L_{OUT} is given by Equation 9 and Equation 10. From Equation 9 and Equation 10, assuming a 5V power supply and a 32Ω load, the maximum power dissipation for L_{OUT} and R_{OUT} is 40mW, or 80mW total.

$$P_{DMAX-LOUT} = (V_{DD})^2 / (2\pi^2 R_L)\text{: Single-ended Mode} \quad (9)$$

$$P_{DMAX-ROUT} = (V_{DD})^2 / (2\pi^2 R_L)\text{: Single-ended Mode} \quad (10)$$

The maximum internal power dissipation of the LM4846 occurs when all 3 amplifiers pairs are simultaneously on; and is given by Equation 11.

$$P_{DMAX-TOTAL} = P_{DMAX-SPKROUT} + P_{DMAX-LOUT} + P_{DMAX-ROUT} \quad (11)$$

The maximum power dissipation point given by Equation 11 must not exceed the power dissipation given by Equation 12:

$$P_{DMAX} = (T_{JMAX} - T_A) / \theta_{JA} \quad (12)$$

The LM4846's T_{JMAX} = 150°C. In the YZR package, the LM4846's θ_{JA} is 65°C/W. At any given ambient temperature T_A, use Equation 12 to find the maximum internal power dissipation supported by the IC packaging. Rearranging Equation 12 and substituting $P_{DMAX-TOTAL}$ for P_{DMAX}' results in Equation 13. This equation gives the maximum ambient temperature that still allows maximum stereo power dissipation without violating the LM4846's maximum junction temperature.

$$T_A = T_{JMAX} - P_{DMAX-TOTAL}\,\theta_{JA} \quad (13)$$

For a typical application with a 5V power supply and an 8Ω load, the maximum ambient temperature that allows maximum stereo power dissipation without exceeding the maximum junction temperature is approximately 104°C for the YZR package.

$$T_{JMAX} = P_{DMAX-TOTAL}\,\theta_{JA} + T_A \quad (14)$$

Equation 14 gives the maximum junction temperature T_{JMAX}. If the result violates the LM4846's 150°C, reduce the maximum junction temperature by reducing the power supply voltage or increasing the load resistance. Further allowance should be made for increased ambient temperatures.

The above examples assume that a device is a surface mount part operating around the maximum power dissipation point. Since internal power dissipation is a function of output power, higher ambient temperatures are allowed as output power or duty cycle decreases. If the result of Equation 11 is greater than that of Equation 12, then decrease the supply voltage, increase the load impedance, or reduce the ambient temperature. If these measures are insufficient, a heat sink can be added to reduce θ_{JA}. The heat sink can be created using additional copper area around the package, with connections to the ground pin(s), supply pin and amplifier output pins. External, solder attached SMT heatsinks such as the Thermalloy 7106D can also improve power dissipation. When adding a heat sink, the θ_{JA} is the sum of θ_{JC}, θ_{CS}, and θ_{SA}. (θ_{JC} is the junction-to-case thermal impedance, θ_{CS} is the case-to-sink thermal impedance, and θ_{SA} is the sink-to-ambient thermal impedance). Refer to the Typical Performance Characteristics curves for power dissipation information at lower output power levels.

POWER SUPPLY BYPASSING

As with any power amplifier, proper supply bypassing is critical for low noise performance and high power supply rejection. Applications that employ a 5V regulator typically use a 1µF in parallel with a 0.1µF filter capacitors to stabilize the regulator's output, reduce noise on the supply line, and improve the supply's transient response. However, their presence does not eliminate the need for a local 1.1µF tantalum bypass capacitance connected between the LM4846's supply pins and ground. Keep the length of leads and traces that connect capacitors between the LM4846's power supply pin and ground as short as possible. Connecting a 2.2µF capacitor, C_B, between the BYPASS pin and ground improves the internal bias voltage's stability and improves the amplifier's PSRR. The PSRR improvements increase as the bypass pin capacitor value increases. Too large, however, increases turn-on time and can compromise the amplifier's click and pop performance. The selection of bypass capacitor values, especially C_B, depends on desired PSRR requirements, click and pop performance (as explained in the section, SELECTING EXTERNAL COMPONENTS), system cost, and size constraints.

SELECTING EXTERNAL COMPONENTS

Input Capacitor Value Selection

Amplifying the lowest audio frequencies requires high value input coupling capacitor (C_i in Figure 1 & Figure 2). A high value capacitor can be expensive and may compromise space efficiency in portable designs. In many cases, however, the speakers used in portable systems, whether internal or external, have little ability to reproduce signals below 150Hz. Applications using speakers with this limited frequency response reap little improvement by using large input capacitor.

The internal input resistor (R_i), nominal 20kΩ, and the input capacitor (C_i) produce a high pass filter cutoff frequency that is found using Equation 15.

$$f_c = 1 / (2\pi R_i C_i) \quad (15)$$

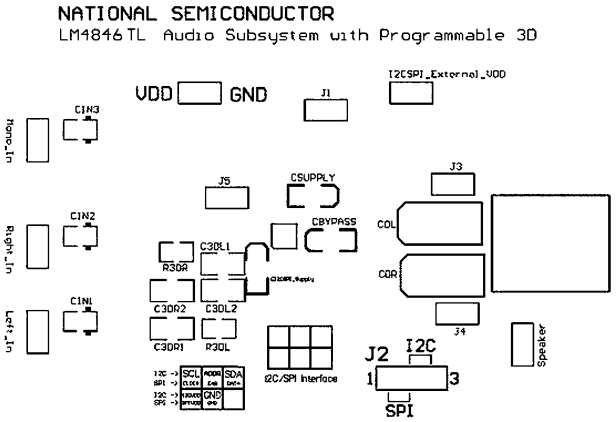
As an example when using a speaker with a low frequency limit of 150Hz, C_i, using Equation 15 is 0.053µF. The 0.22µF C_i shown in Figure 1 allows the LM4846 to drive high efficiency, full range speaker whose response extends below 40Hz.

Bypass Capacitor Value Selection

Besides minimizing the input capacitor size, careful consideration should be paid to value of C_B, the capacitor connected to the BYPASS bump. Since C_B determines how fast the LM4846 settles to quiescent operation, its value is critical when minimizing turn-on pops. The slower the LM4846's outputs ramp to their quiescent DC voltage (nominally $V_{DD}/2$), the smaller the turn-on pop. Choosing C_B equal to 1.0µF along with a small value of C_i (in the range of 0.1µF to 0.39µF), produces a click-less and pop-less shutdown function. As discussed above, choosing C_i no larger than necessary for the desired bandwidth helps minimize clicks and pops. C_B's value should be in the range of 5 times to 7 times the value of C_i. This ensures that output transients are eliminated when power is first applied or the LM4846 resumes operation after shutdown.

LM4846 TL DEMO BOARD ARTWORK

Figure 72. Top Overlay



	J5	J4	J3	J2	J1
SE	SHORT	OPEN	OPEN		
OCL	OPEN	SHORT	SHORT		
I2C				2-3	
SPI				1-2	
I2CSPI_VDD					SHORT
I2CSPI_External_VDD					OPEN

Figure 73. Top Layer

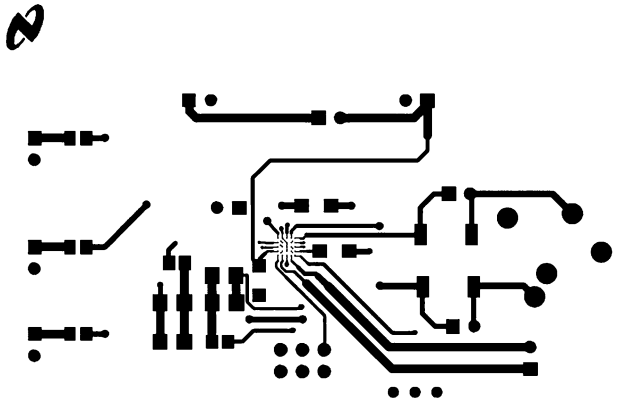
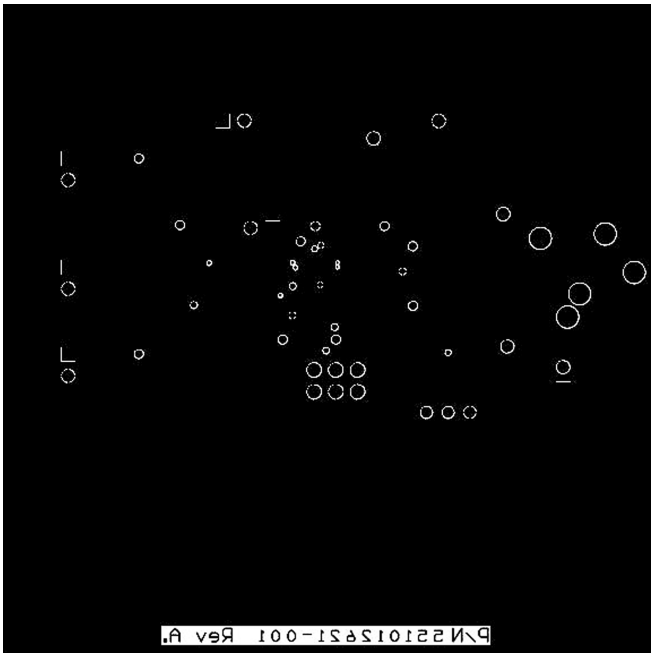


Figure 74. Bottom Layer



Revision History

Rev	Date	Description
1.0	11/10/05	1st WEB released.
1.1	12/21/05	Edited the X1, X2, and X3 in the mktg ouline, then re-released D/S to the WEB.
1.2	01/13/06	Added the Typ. Perf. curves, then released D/S to the WEB.
1.3	07/06/06	Added the Twu row on the 3.3V and 5.0V EC tables (per Allan S.), then re-released D/S to the WEB.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
LM4846TL/NOPB	ACTIVE	DSBGA	YZR	25	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	GG5	Samples
LM4846TLX/NOPB	ACTIVE	DSBGA	YZR	25	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	GG5	Samples

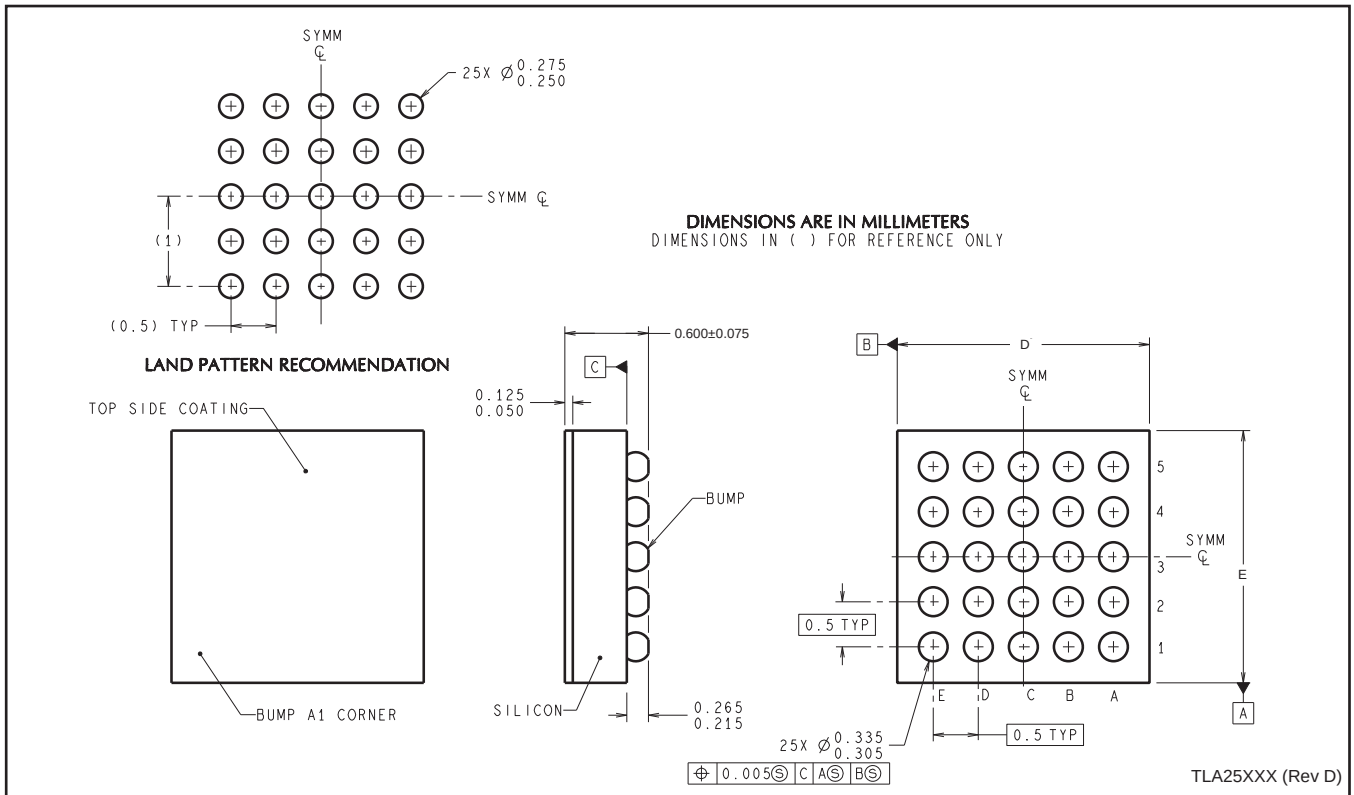
(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Only one of markings shown within the brackets will appear on the physical device.

YZR0025



D: Max = 2.601 mm, Min = 2.5 mm

E: Max = 2.581 mm, Min = 2.48 mm

4215055/A 12/12

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.

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