LM4859 Boomer® Audio Power Amplifier Series Stereo 1.2W Audio Sub-system with 3D Enhancement

Check for Samples: LM4859

FEATURES

- **Stereo Speaker Amplifier**
- **Stereo Headphone Amplifier**
- **Independent Left, Right, and Mono Volume Controls**
- **Texas Instruments 3D Enhancement**
- **I^2C Compatible Interface**
- **Ultra Low Shutdown Current**
- **Click and Pop Suppression Circuit**
- **10 Distinct Output Modes**
- **Thermal Shutdown Protection**
- **Available in DSBGA and UQFN packages**

APPLICATIONS

- **Cell Phones**
- **PDAs**
- **Portable Gaming Devices**
- **Internet Appliances**
- **Portable DVD/CD/AAC/MP3 Players**

APPLICATIONS

- **P_{OUT}, Stereo Loudspeakers, 4Ω, 5V, 1% THD+N (LM4859SP), 1.6W (Typ)**
- **P_{OUT}, Stereo Loudspeakers, 8Ω, 5V, 1% THD+N, 1.2W (Typ)**
- **P_{OUT}, Stereo Headphones, 32Ω, 5V, 1% THD+N, 75mW (typ)**
- **P_{OUT}, Stereo Loudspeakers, 8Ω, 3.3V, 1% THD+N, 495mW (typ)**
- **P_{OUT}, Stereo Headphones, 32Ω, 3.3V, 1% THD+N, 33mW (typ)**
- **Shutdown Current, 0.06µA (typ)**

DESCRIPTION

The LM4859 is an integrated audio sub-system designed for stereo cell phone applications. Operating on a 3.3V supply, it combines a stereo speaker amplifier delivering 495mW per channel into an 8Ω load and a stereo headphone amplifier delivering 33mW per channel into a 32Ω load. It integrates the audio amplifiers, volume control, mixer, power management control, and Texas Instruments 3D enhancement all into a single package. In addition, the LM4859 routes and mixes the stereo and mono inputs into 10 distinct output modes. The LM4859 is controlled through an I^2C compatible interface. Other features include an ultra-low current shutdown mode and thermal shutdown protection.

Boomer audio power amplifiers are designed specifically to provide high quality output power with a minimal amount of external components.

The LM4859 is available in a 30–bump TL package and a 28–lead UQFN package.

Typical Application

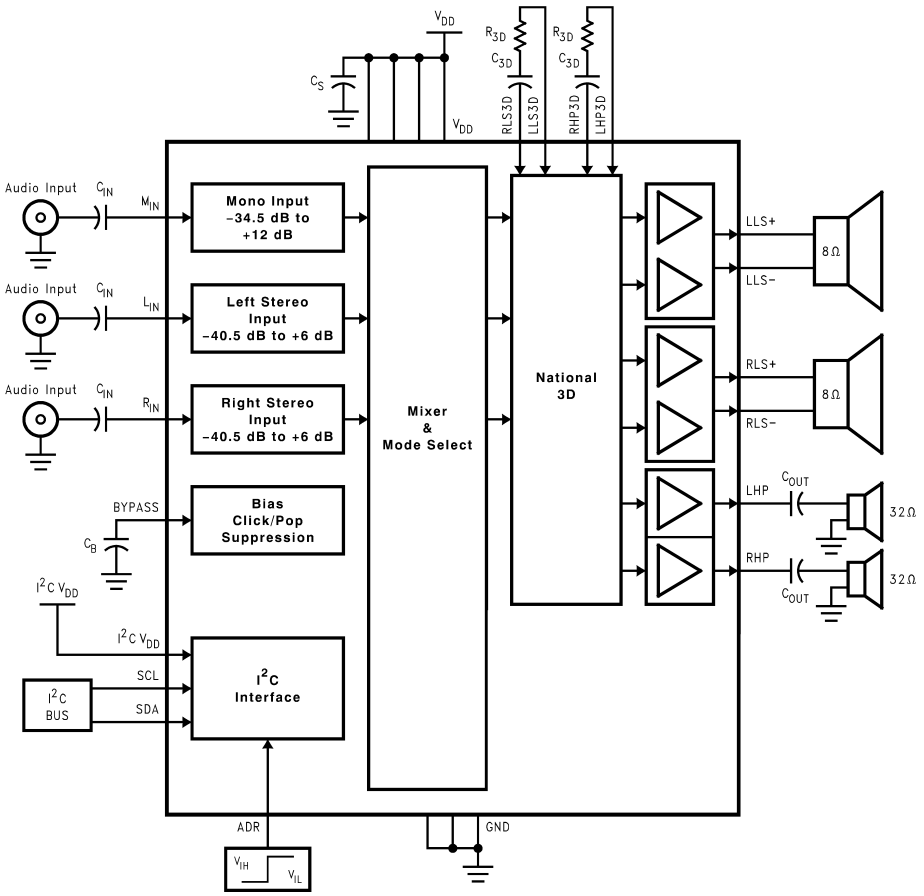


Figure 1. Typical Audio Amplifier Application Circuit

Connection Diagram

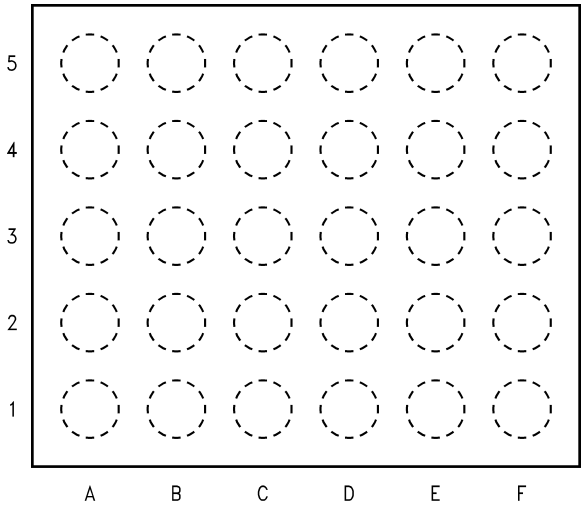


Figure 2. 30 Bump DSBGA Package
Top View
(Bump-side down)
See Package Number YZR0030

PIN CONNECTIONS (DSBGA)

Pin	Name	Pin Description
A1	RLS+	Right Loudspeaker Positive Output
A2	V_{DD}	Power Supply
A3	SDA	Data
A4	RHP3D	Right Headphone 3D
A5	RHP	Right Headphone Output
B1	GND	Ground
B2	I^2CV_{DD}	I^2C Interface Power Supply
B3	ADR	I^2C Address Select
B4	LHP3D	Left Headphone 3D
B5	V_{DD}	Power Supply
C1	RLS-	Right Loudspeaker Negative Output
C2	NC	No Connect
C3	SCL	Clock
C4	NC	No Connect
C5	GND	Ground
D1	LLS-	Left Loudspeaker Negative Output
D2	V_{DD}	Power Supply
D3	M_{IN}	Mono Input
D4	NC	No Connect
D5	NC	No Connect
E1	GND	Ground
E2	BYPASS	Half-supply bypass
E3	LLS3D	Left Loudspeaker 3D
E4	R_{IN}	Right Stereo Input
E5	NC	No Connect
F1	LLS+	Left Loudspeaker Positive Output
F2	V_{DD}	Power Supply
F3	RLS3D	Right Loudspeaker 3D
F4	L_{IN}	Left Stereo Input
F5	LHP	Left Headphone Output

Connection Diagram

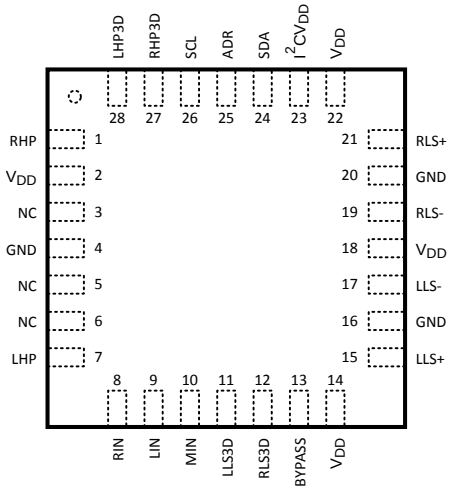


Figure 3. 28 – Lead UQFN Package, Top View
See Package Number NJD0028A

PIN CONNECTIONS (UQFN)

Pin	Name	Pin Description
1	RHP	Right Headphone Output
2	V_{DD}	Power Supply
3	NC	No Connect
4	GND	Ground
5	NC	No Connect
6	NC	No Connect
7	LHP	Left Headphone Output
8	RIN	Right Stereo Input
9	LIN	Left Stereo Input
10	MIN	Mono Input
11	LLS3D	Left Loudspeaker 3D
12	RLS3D	Right Loudspeaker 3D
13	BYPASS	Half-supply bypass
14	V_{DD}	Power Supply
15	LLS+	Left Loudspeaker Positive Output
16	GND	Ground
17	LLS-	Left Loudspeaker Negative Output
18	V_{DD}	Power Supply
19	RLS-	Right Loudspeaker Negative Output
20	GND	Ground
21	RLS+	Right Loudspeaker Positive Output
22	V_{DD}	Power Supply
23	I^2CV_{DD}	I^2C Interface Power Supply
24	SDA	Data
25	ADR	I^2C Address Select
26	SCL	Clock
27	RHP3D	Right Headphone 3D
28	LHP3D	Left Headphone 3D

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings(1)(2)

Supply Voltage		6.0V
Storage Temperature		−65°C to +150°C
Input Voltage		−0.3V to V_{DD} +0.3V
Power Dissipation(3)		Internally Limited
ESD Susceptibility(4)		2000V
ESD Susceptibility(5)		200V
Junction Temperature (T_J)		150°C
Thermal Resistance	θ_{JA} (NJD0028A)(6)	42°C/W
	θ_{JC} (NJD0028A)	3°C/W
	θ_{JA} (YZR0030)(7)	62°C/W

(1) All voltages are measured with respect to the GND pin unless otherwise specified.
(2) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional but do not guarantee specific performance limits. Electrical Characteristics state DC and AC electrical specifications under particular test conditions which guarantee specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not guaranteed for parameters where no limit is given, however, the typical value is a good indication of device performance.
(3) The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{JMAX}, θ_{JA}, and the ambient temperature, T_A. The maximum allowable power dissipation is $P_{DMAX} = (T_{JMAX} - T_A) / \theta_{JA}$ or the number given in Absolute Maximum Ratings, whichever is lower. For the LM4859 operating in Mode 3, 8, or 13 with V_{DD} = 5V, 8Ω stereo loudspeakers and 32Ω stereo headphones, the total power dissipation is 1.348W. θ_{JA} = 62°C/W.
(4) Human body model, 100pF discharged through a 1.5kΩ resistor.
(5) Machine Model, 220pF-240pF discharged through all pins.
(6) The given θ_{JA} is for an LM4859SP mounted on a PCB with a $2in^2$ area of 10oz printed circuit board ground plane.
(7) The given θ_{JA} is for an LM4859TL mounted on a PCB with a $2in^2$ area of 10oz printed circuit board ground plane.

Operating Ratings

Temperature Range	$T_{MIN} \le T_A \le T_{MAX}$	−40°C ≤ T_A ≤ +85°C
Supply Voltage		2.7V ≤ V_{DD} ≤ 5.5V
		2.5V ≤ I^2CV_{DD} ≤ 5.5V

Audio Amplifier Electrical Characteristics V_{DD} = 5.0V (1) (2)

The following specifications apply for V_{DD} = 5.0V, unless otherwise specified. Limits apply for T_A = 25°C.

Symbol	Parameter	Conditions	LM4859		Units (Limits)
			Typical (3)	Limits (4) (5)	
I_{DD}	Supply Current	V_{IN} = 0V, No load; LD5 = RD5 = 0 (6)			
		Mode 4, 9, 14	5	8	mA (max)
		Mode 2, 3, 7, 8, 12, 13	13	21	mA (max)
I_{SD}	Shutdown Current	Output mode 0 (6)	0.2	3	µA (max)
P_O	Output Power	LM4859SP Speaker; THD+N = 1%; f = 1kHz; 4Ω BTL	1.6		W
		Speaker; THD+N = 1%; f = 1kHz; 8Ω BTL	1.2	0.9	W (min)
		Headphone; THD+N = 1%; f = 1kHz; 32Ω SE	75	60	mW (min)
THD+N	Total Harmonic Distortion Plus Noise	LD5 = RD5 = 0			
		Speaker; P_O = 400mW; f = 1kHz; 8Ω BTL	0.05		%
		Headphone; P_O = 15mW; f = 1kHz; 32Ω SE	0.04		%
V_{OS}	Offset Voltage	Speaker; LD5 = RD5 = 0	5	40	mV (max)
N_{OUT}	Output Noise	A-weighted, 0dB gain; (7) LD5 = RD5 = 0; Audio Inputs Terminated			
		Speaker; Mode 2, 3, 7, 8	27		µV
		Speaker; Mode 12, 13	38		µV
		Headphone; Mode 3, 4, 8, 9	10		µV
		Headphone; Mode 13, 14	14		µV
PSRR	Power Supply Rejection Ratio	f = 217Hz; V_{rip} = 200mV_{pp}; C_B = 2.2µF; 0dB gain; (7) LD5 = RD5 = 0; Audio Inputs Terminated			
		Speaker; Mode 2, 3, 7, 8	70		dB
		Speaker; Mode 12, 13,	64	54	dB (min)
		Headphone; Mode 3, 4, 8, 9	86		dB
		Headphone; Mode 13, 14	73	60	dB (min)
Xtalk	Crosstalk	LD5 = RD5 = 0			
		Loudspeaker; P_O = 400mW; f = 1kHz	85		dB
		Headphone; P_O = 15mW; f = 1kHz	85		dB
T_{WU}	Wake-up Time	CD5 = 0; C_B = 2.2µF	120		ms
		CD5 = 1; C_B = 2.2µF	230		ms

(1) All voltages are measured with respect to the GND pin unless otherwise specified.
(2) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional but do not guarantee specific performance limits. Electrical Characteristics state DC and AC electrical specifications under particular test conditions which guarantee specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not guaranteed for parameters where no limit is given, however, the typical value is a good indication of device performance.
(3) Typicals are measured at +25°C and represent the parametric norm.
(4) Limits are guaranteed to Texas Instruments' AOQL (Average Outgoing Quality Level).
(5) Datasheet min/max specification limits are guaranteed by design, test, or statistical analysis.
(6) Shutdown current and supply current are measured in a normal room environment. All digital input pins are connected to I^2CV_{DD}.
(7) "0dB gain" refers to the volume control gain setting of M_{IN}, L_{IN}, and R_{IN} set at 0dB.

Audio Amplifier Electrical Characteristics V_{DD} = 3.0V (1)(2)

The following specifications apply for V_{DD} = 3.0V, unless otherwise specified. Limits apply for T_A = 25°C.

Symbol	Parameter	Conditions	LM4859		Units (Limits)
			Typical (3)	Limits (4) (5)	
I_{DD}	Supply Current	V_{IN} = 0V, No load; LD5 = RD5 = 0 (6)			
		Mode 4, 9, 14	4.5	7.5	mA (max)
		Mode 2, 3, 7, 8, 12, 13	11.2	19	mA (max)
I_{SD}	Shutdown Current	Mode 0 (6)	0.06	2.5	µA (max)
P_O	Output Power	LM4859SP Speaker; THD+N = 1%; f = 1kHz; 4Ω BTL	530		mW
P_O	Output Power	Speaker; THD+N = 1%; f = 1kHz; 8Ω BTL	400	320	mW (min)
		Headphone; THD+N = 1%; f = 1kHz; 32Ω SE	25	20	mW (min)
THD+N	Total Harmonic Distortion Plus Noise	LD5 = RD5 = 0			
		Speaker; P_O = 200mW; f = 1kHz; 8Ω BTL	0.05		%
		Headphone; P_O = 10mW; f = 1kHz; 32Ω SE	0.04		%
V_{OS}	Offset Voltage	Speaker; LD5 = RD5 = 0	5	40	mV (max)
N_{OUT}	Output Noise	A-weighted; 0dB gain; (7) LD5 = RD5 = 0; All Inputs Terminated			
		Speaker; Mode 2, 3, 7, 8	27		µV
		Speaker; Mode 12, 13	38		µV
		Headphone; Mode 3, 4, 8, 9	10		µV
		Headphone; Mode 13, 14	14		µV
PSRR	Power Supply Rejection Ratio	f = 217Hz, V_{rip} = 200mV_{pp}; C_B = 2.2µF; 0dB gain; (7) LD5 = RD5 = 0; All Audio Inputs Terminated			
		Speaker; Mode 2, 3, 7, 8	70		dB
		Speaker; Mode 12, 13,	65	55	dB (min)
		Headphone; Mode 3, 4, 8, 9	87		dB
		Headphone; Mode 13, 14	75	62	dB (min)
Xtalk	Crosstalk	LD5 = RD5 = 0			
		Loudspeaker; P_O = 200mW; f = 1kHz	82		dB
		Headphone; P_O = 10mW; f = 1kHz	82		dB
T_{WU}	Wake-up Time	CD5 = 0; C_B = 2.2µF	80		ms
		CD5 = 1; C_B = 2.2µF	140		ms

(1) All voltages are measured with respect to the GND pin unless otherwise specified.
(2) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional but do not guarantee specific performance limits. Electrical Characteristics state DC and AC electrical specifications under particular test conditions which guarantee specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not guaranteed for parameters where no limit is given, however, the typical value is a good indication of device performance.
(3) Typicals are measured at +25°C and represent the parametric norm.
(4) Limits are guaranteed to Texas Instruments' AOQL (Average Outgoing Quality Level).
(5) Datasheet min/max specification limits are guaranteed by design, test, or statistical analysis.
(6) Shutdown current and supply current are measured in a normal room environment. All digital input pins are connected to I^2CV_{DD}.
(7) "0dB gain" refers to the volume control gain setting of M_{IN}, L_{IN}, and R_{IN} set at 0dB.

Volume Control Electrical Characteristics[1][2]

The following specifications apply for V_{DD} = 5.0V and V_{DD} = 3.0V, unless otherwise specified. Limits apply for T_A = 25°C.

Symbol	Parameter	Conditions	LM4859		Units (Limits)
			Typical[3]	Limits[4][5]	
	Stereo Volume Control Range	maximum gain setting	6	5.5 6.5	dB (min) dB (max)
		minimum gain setting	-40.5	-41 -40	dB (min) dB (max)
	Mono Volume Control Range	maximum gain setting	12	11.5 12.5	dB (min) dB (max)
		minimum gain setting	-34.5	-35 -34	dB (min) dB (max)
	Volume Control Step Size		1.5		dB
	Volume Control Step Size Error		+/-0.2	+/-0.5	dB (max)
	Stereo Channel to Channel Gain Mismatch		0.3		dB
	Mute Attenuation	Mode 12, V_{in} = $1V_{RMS}$			
		Headphone	85		dB
	L_{IN} and R_{IN} Input Impedance	maximum gain setting	33.5	25 42	kΩ (min) kΩ (max)
		minimum gain setting	100	75 125	kΩ (min) kΩ (max)
	M_{IN} Input Impedance	maximum gain setting	20	15 25	kΩ (min) kΩ (max)
		minimum gain setting	98	73 123	kΩ (min) kΩ (max)

(1) All voltages are measured with respect to the GND pin unless otherwise specified.
(2) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional but do not guarantee specific performance limits. Electrical Characteristics state DC and AC electrical specifications under particular test conditions which guarantee specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not guaranteed for parameters where no limit is given, however, the typical value is a good indication of device performance.
(3) Typicals are measured at +25°C and represent the parametric norm.
(4) Limits are guaranteed to Texas Instruments' AOQL (Average Outgoing Quality Level).
(5) Datasheet min/max specification limits are guaranteed by design, test, or statistical analysis.

Control Interface Electrical Characteristics[1][2]

The following specifications apply for V_{DD} = 5V and V_{DD} = 3V and 2.5V ≤ I^2CV_{DD} ≤ 5.5V, unless otherwise specified. Limits apply for T_A = 25°C.

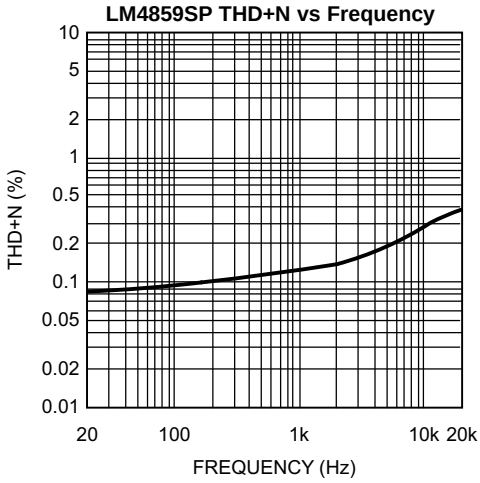
Symbol	Parameter	Conditions	LM4859		Units (Limits)
			Typical[3]	Limits[4][5]	
t_1	SCL period			2.5	µs (min)
t_2	SDA Set-up Time			100	ns (min)
t_3	SDA Stable Time			0	ns (min)
t_4	Start Condition Time			100	ns (min)
t_5	Stop Condition time			100	ns (min)
V_{IH}	Digital Input High Voltage			0.7 x I^2CVDD	V (min)
V_{IL}	Digital Input Low Voltage			0.3 x I^2CV_{DD}	V (max)

(1) All voltages are measured with respect to the GND pin unless otherwise specified.
(2) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional but do not guarantee specific performance limits. Electrical Characteristics state DC and AC electrical specifications under particular test conditions which guarantee specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not guaranteed for parameters where no limit is given, however, the typical value is a good indication of device performance.
(3) Typicals are measured at +25°C and represent the parametric norm.
(4) Limits are guaranteed to Texas Instruments' AOQL (Average Outgoing Quality Level).
(5) Datasheet min/max specification limits are guaranteed by design, test, or statistical analysis.

External Components Description

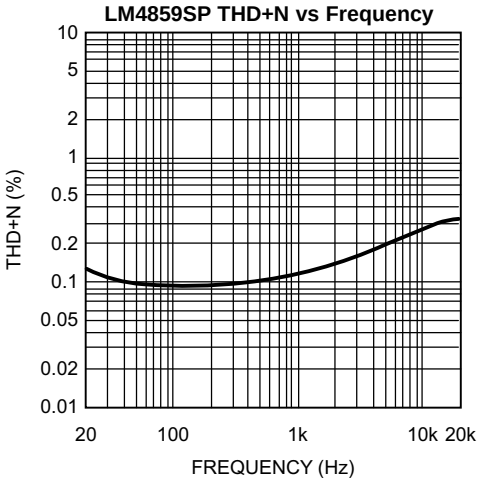
Components		Functional Description
1.	C_{IN}	This is the input coupling capacitor. It blocks the DC voltage and couples the input signal to the amplifier's input terminals. C_{IN} also creates a high pass filter with the internal resistor R_i (Input Impedance) at $f_C = 1/(2\pi R_i C_{IN})$.
2.	C_S	This is the supply bypass capacitor. It filters the supply voltage applied to the V_{DD} pin and helps reduce the noise at the V_{DD} pin.
3.	C_B	This is the BYPASS pin capacitor. It filters the V_{DD} / 2 voltage and helps maintain the LM4859's PSRR.
4.	C_{OUT}	This is the output coupling capacitor. It blocks the DC voltage and couples the output signal to the speaker load R_L. C_{OUT} also creates a high pass filter with R_L at $f_O = 1/(2\pi R_L C_{OUT})$.
5.	R_{3D}	This resistor sets the gain of the Texas Instruments 3D effect. Please refer to the **Texas Instruments 3D Enhancement** section for information on selecting the value of R_{3D}.
6.	C_{3D}	This capacitor sets the frequency at which the Texas Instruments 3D effect starts to occur. Please refer to the **Texas Instruments 3D Enhancement** section for information on selecting the value of C_{3D}.

Typical Performance Characteristics(1)



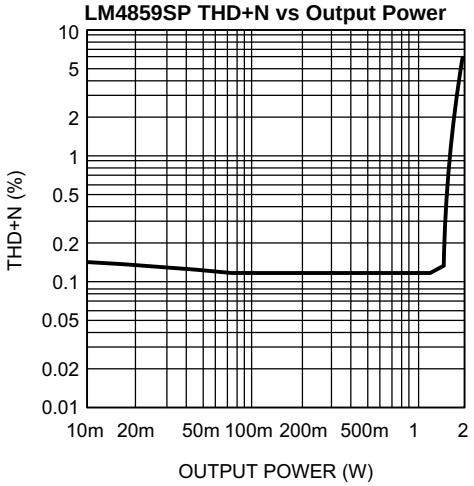
V_{DD} = 5V; LLS, RLS; P_O = 400mW;
R_L = 4Ω; Mode 7; 0dB Gain

Figure 4.



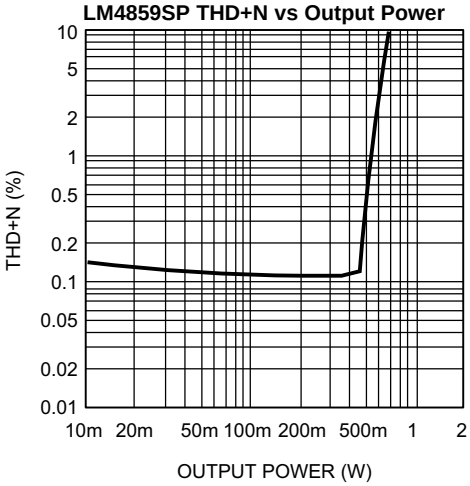
V_{DD} = 3V; LLS, RLS; P_O = 200mW;
R_L = 4Ω; Mode 7; 0dB Gain

Figure 5.



V_{DD} = 5V; LLS, RLS; f = 1kHz;
R_L = 4Ω; Mode 7; 0dB Gain

Figure 6.

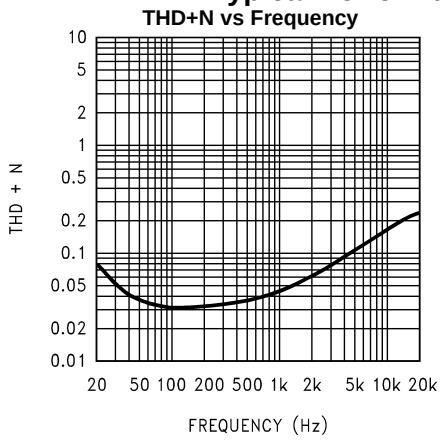


V_{DD} = 3V; LLS, RLS; f = 1kHz;
R_L = 4Ω; Mode 7; 0dB Gain

Figure 7.

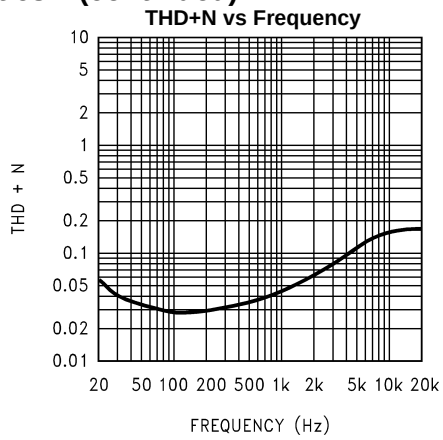
(1) "0dB gain" refers to the volume control gain setting of M_{IN}, L_{IN}, and R_{IN} set at 0dB.

Typical Performance Characteristics[1] (continued)



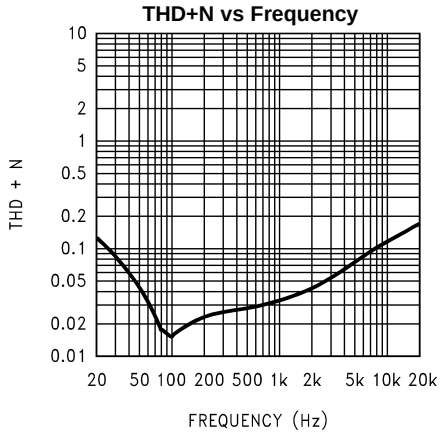
V_{DD} = 5V; LLS, RLS; P_O = 400mW;
R_L = 8Ω; Mode 7; 0dB Gain

Figure 8.



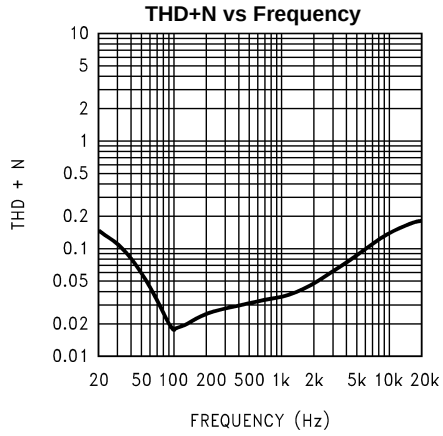
V_{DD} = 3V; LLS, RLS; P_O = 200mW;
R_L = 8Ω; Mode 7; 0dB Gain

Figure 9.



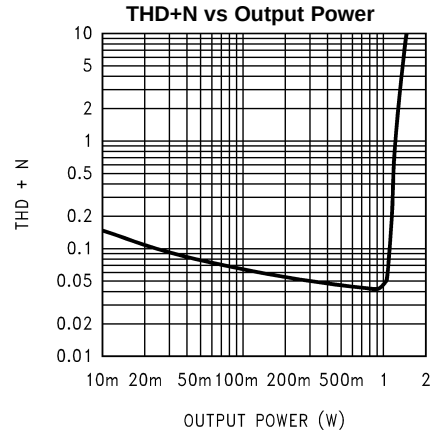
V_{DD} = 5V; LHP, RHP; P_O = 15mW;
R_L = 32Ω; Mode 9; 0dB Gain

Figure 10.



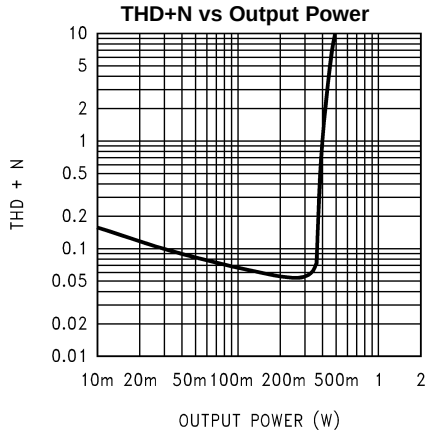
V_{DD} = 3V; LHP, RHP; P_O = 10mW;
R_L = 32Ω; Mode 9; 0dB Gain

Figure 11.



V_{DD} = 5V; LLS, RLS; f = 1kHz;
R_L = 8Ω; Mode 7; 0dB Gain

Figure 12.

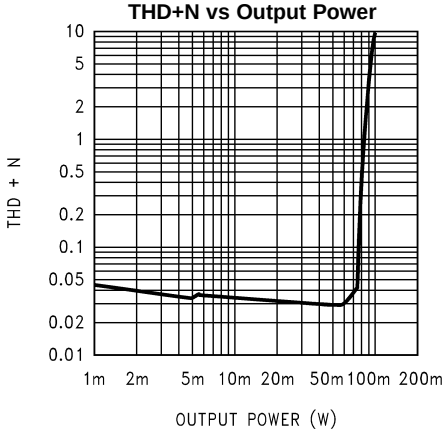


V_{DD} = 3V; LLS, RLS; f = 1kHz;
R_L = 8Ω; Mode 7; 0dB Gain

Figure 13.

Typical Performance Characteristics[1] (continued)

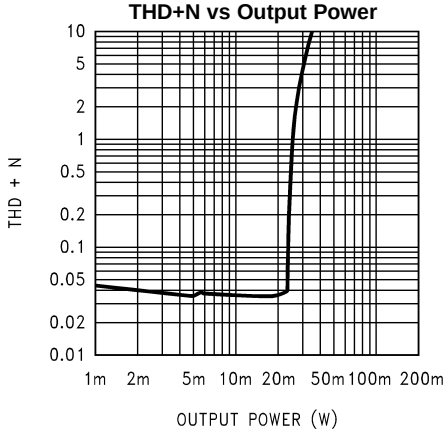
THD+N vs Output Power



V_{DD} = 5V; LHP, RHP; f = 1kHz;
R_L = 32Ω; Mode 9; 0dB Gain

Figure 14.

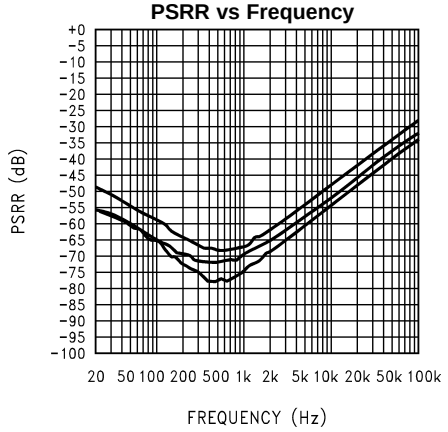
THD+N vs Output Power



V_{DD} = 3V; LHP, RHP; f = 1kHz;
R_L = 32Ω; Mode 9; 0dB Gain

Figure 15.

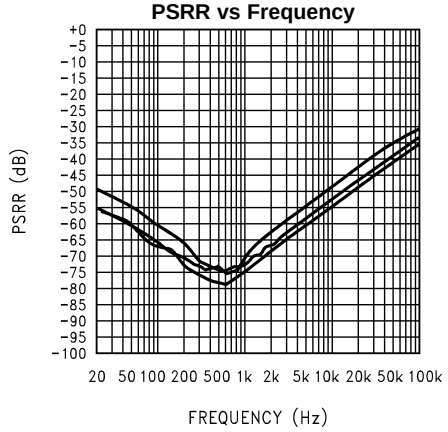
PSRR vs Frequency



V_{DD} = 5V; LLS, RLS; R_L = 8Ω; 0db Gain;
All audio inputs terminated
Top-Mode 12, 13; Mid-Mode 2, 3; Bot-Mode 7, 8

Figure 16.

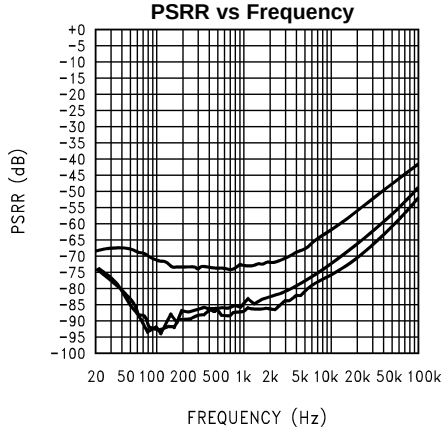
PSRR vs Frequency



V_{DD} = 3V; LLS, RLS; R_L = 8Ω; 0db Gain;
All audio inputs terminated
Top-Mode 12, 13; Mid-Mode 2, 3; Bot-Mode 7, 8

Figure 17.

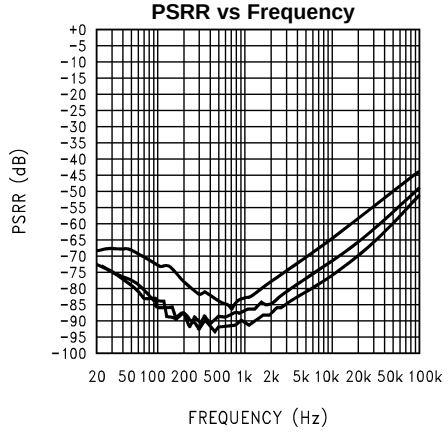
PSRR vs Frequency



V_{DD} = 5V; LHP, RHP; R_L = 32Ω; 0db Gain;
All audio inputs terminated
Top-Mode 13, 14; Mid-Mode 3, 4; Bot-Mode 8, 9

Figure 18.

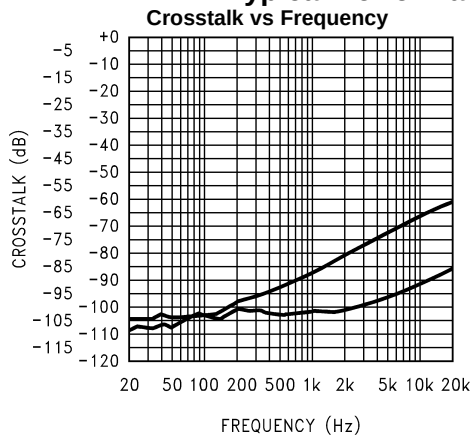
PSRR vs Frequency



V_{DD} = 3V; LHP, RHP; R_L = 32Ω; 0db Gain;
All audio inputs terminated
Top-Mode 13, 14; Mid-Mode 3, 4; Bot-Mode 8, 9

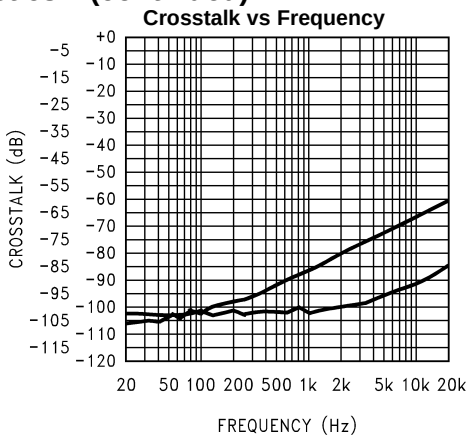
Figure 19.

Typical Performance Characteristics[1] (continued)



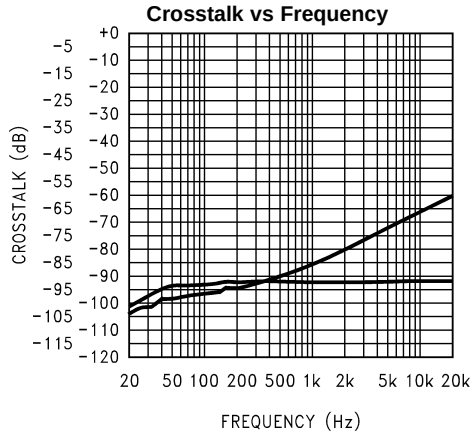
V_{DD} = 5V; LLS, RLS; P_O = 400mW; R_L = 8Ω;
Mode 7; 0db Gain; 3D off
Top-Left to Right; Bot-Right to Left

Figure 20.



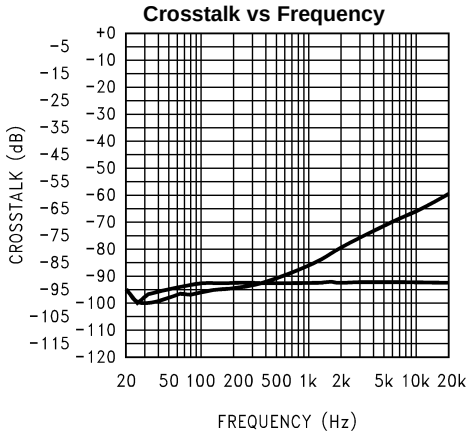
V_{DD} = 3V; LLS, RLS; P_O = 200mW; R_L = 8Ω;
Mode 7; 0db Gain; 3D off
Top-Left to Right; Bot-Right to Left

Figure 21.



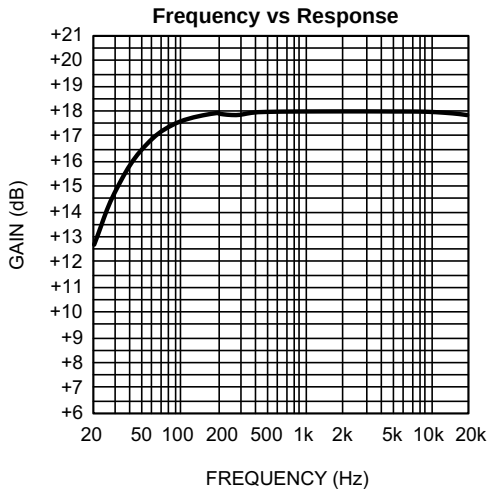
V_{DD} = 5V; LHP, RHP; P_O = 15mW; R_L = 32Ω;
Mode 9; 0db Gain; 3D off
Top-Left to Right; Bot-Right to Left

Figure 22.

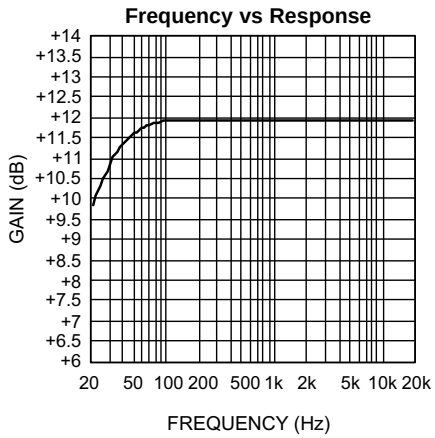


$_{DD}$ = 3V; LHP, RHP; P_O = 10mW; R_L = 32Ω;
Mode 9; 0db Gain; 3D off
Top-Left to Right; Bot-Right to Left

Figure 23. V



LLS, RLS; R_L = 8Ω;
Mode 2; Full Gain

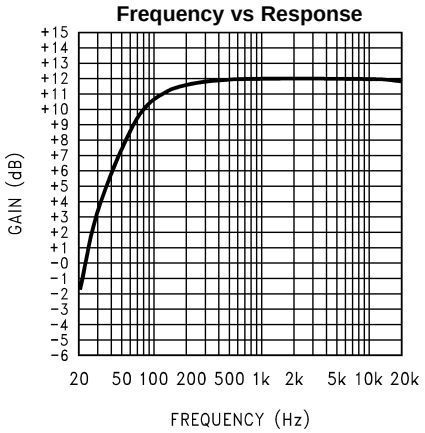


LLS, RLS; R_L = 8Ω;
Mode 7; Full Gain

Typical Performance Characteristics[1] (continued)

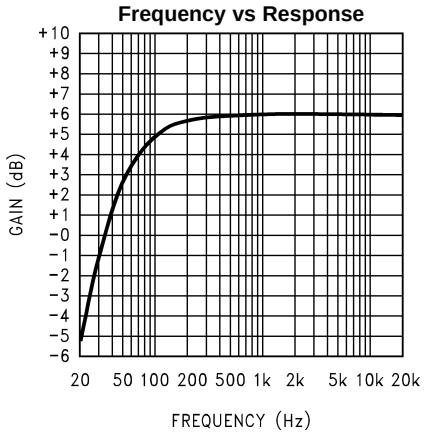
Figure 24.

Figure 25.



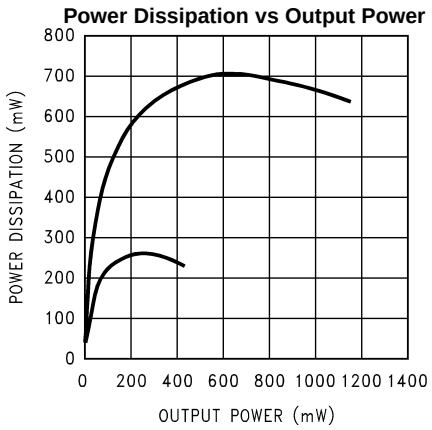
LHP, RHP; R_L = 32Ω; C_O = 100µF
Mode 4; Full Gain

Figure 26.



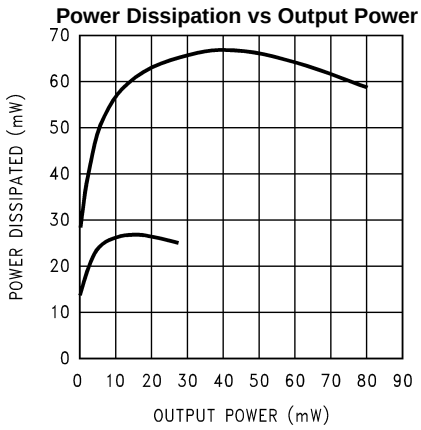
LHP, RHP; R_L = 32Ω; C_O = 100µF
Mode 9; Full Gain

Figure 27.



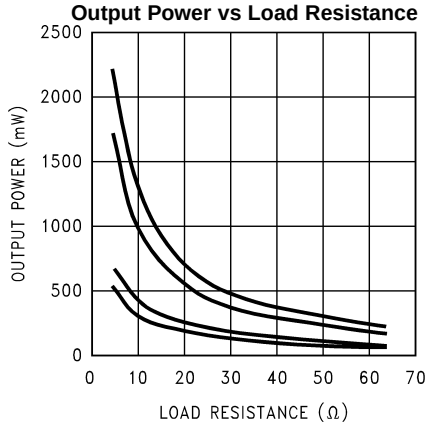
LLS, RLS; R_L = 8Ω; THD+N ≤ 1%
Top-V_{DD} = 5V; Bot-V_{DD} = 3V
per channel

Figure 28.



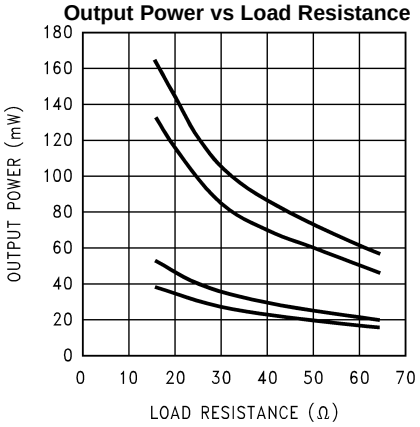
HP, RHP; R_L = 32Ω; THD+N ≤ 1%
Top-V_{DD} = 5V; Bot-V_{DD} = 3V
per channel

Figure 29. L



LLS, RLS; R_L = 8Ω;
Top-V_{DD} = 5V, 10% THD+N; Topmid-V_{DD} = 5V, 1% THD+N;
Botmid-V_{DD} = 3V, 10% THD+N; Bot-V_{DD} = 3V, 1% THD+N

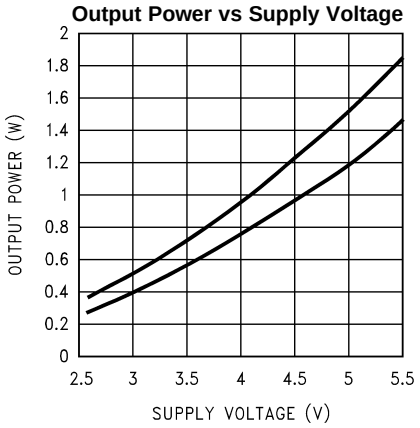
Figure 30.



LHP, RHP; R_L = 32Ω;
Top-V_{DD} = 5V, 10% THD+N; Topmid-V_{DD} = 5V, 1% THD+N;
Botmid-V_{DD} = 3V, 10% THD+N; Bot-V_{DD} = 3V, 1% THD+N

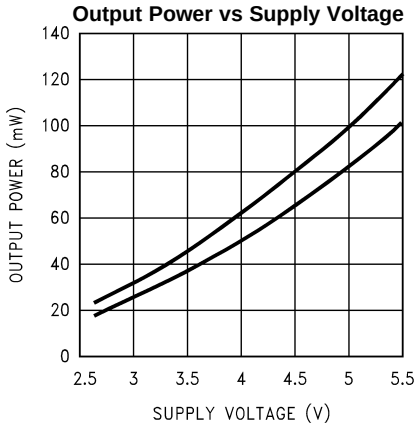
Figure 31.

Typical Performance Characteristics[1] (continued)



LLS, RLS; R_L = 8Ω;
Top–10% THD+N; Bot–1% THD+N

Figure 32.



LHP, RHP; R_L = 32Ω;
Top–10% THD+N; Bot–1% THD+N

Figure 33.

APPLICATION INFORMATION

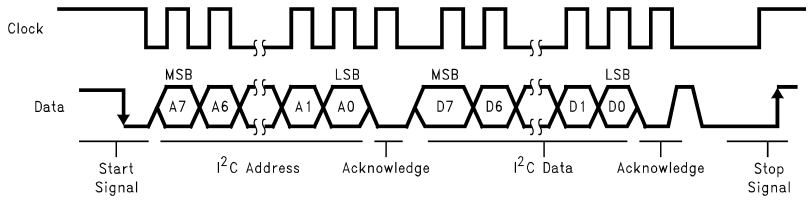


Figure 34. I²C Bus Format

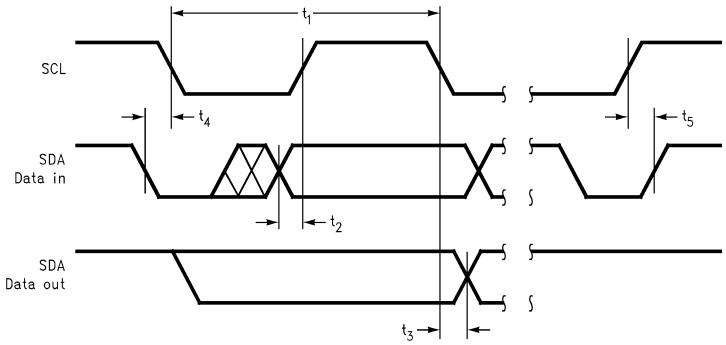


Figure 35. I²C Timing Diagram

Table 1. Chip Address(1)

	A7	A6	A5	A4	A3	A2	A1	A0
Chip Address	1	1	1	1	1	0	EC	0
ADR = 0	1	1	1	1	1	0	0	0
ADR = 1	1	1	1	1	1	0	1	0

(1) EC - externally configured by ADR pin

Table 2. Control Registers

	D7	D6	D5	D4	D3	D2	D1	D0
Mono Volume control	0	0	0	MD4	MD3	MD2	MD1	MD0
Left Volume control	0	1	LD5	LD4	LD3	LD2	LD1	LD0
Right Volume control	1	0	RD5	RD4	RD3	RD2	RD1	RD0
Mode control	1	1	CD5	0	CD3	CD2	CD1	CD0

Table 3. Mono Volume Control

MD4	MD3	MD2	MD1	MD0	Gain (dB)
0	0	0	0	0	-34.5
0	0	0	0	1	-33.0
0	0	0	1	0	-31.5
0	0	0	1	1	-30.0
0	0	1	0	0	-28.5
0	0	1	0	1	-27.0
0	0	1	1	0	-25.5
0	0	1	1	1	-24.0
0	1	0	0	0	-22.5
0	1	0	0	1	-21.0
0	1	0	1	0	-19.5

Table 3. Mono Volume Control (continued)

MD4	MD3	MD2	MD1	MD0	Gain (dB)
0	1	0	1	1	-18.0
0	1	1	0	0	-16.5
0	1	1	0	1	-15.0
0	1	1	1	0	-13.5
0	1	1	1	1	-12.0
1	0	0	0	0	-10.5
1	0	0	0	1	-9.0
1	0	0	1	0	-7.5
1	0	0	1	1	-6.0
1	0	1	0	0	-4.5
1	0	1	0	1	-3.0
1	0	1	1	0	-1.5
1	0	1	1	1	0.0
1	1	0	0	0	1.5
1	1	0	0	1	3.0
1	1	0	1	0	4.5
1	1	0	1	1	6.0
1	1	1	0	0	7.5
1	1	1	0	1	9.0
1	1	1	1	0	10.5
1	1	1	1	1	12.0

Table 4. Stereo Volume Control

LD4//RD4	LD3//RD3	LD2//RD2	LD1//RD1	LD0//RD0	Gain (dB)
0	0	0	0	0	-40.5
0	0	0	0	1	-39.0
0	0	0	1	0	-37.5
0	0	0	1	1	-36.0
0	0	1	0	0	-34.5
0	0	1	0	1	-33.0
0	0	1	1	0	-31.5
0	0	1	1	1	-30.0
0	1	0	0	0	-28.5
0	1	0	0	1	-27.0
0	1	0	1	0	-25.5
0	1	0	1	1	-24.0
0	1	1	0	0	-22.5
0	1	1	0	1	-21.0
0	1	1	1	0	-19.5
0	1	1	1	1	-18.0
1	0	0	0	0	-16.5
1	0	0	0	1	-15.0
1	0	0	1	0	-13.5
1	0	0	1	1	-12.0
1	0	1	0	0	-10.5
1	0	1	0	1	-9.0
1	0	1	1	0	-7.5

Table 4. Stereo Volume Control (continued)

LD4//RD4	LD3//RD3	LD2//RD2	LD1//RD1	LD0//RD0	Gain (dB)
1	0	1	1	1	-6.0
1	1	0	0	0	-4.5
1	1	0	0	1	-3.0
1	1	0	1	0	-1.5
1	1	0	1	1	0.0
1	1	1	0	0	1.5
1	1	1	0	1	3.0
1	1	1	1	0	4.5
1	1	1	1	1	6.0

Table 5. Mixer and Output Mode

Mode	CD3	CD2	CD1	CD0	Loudspeaker L	Loudspeaker R	Headphone L	Headphone R
0	0	0	0	0	SD	SD	SD	SD
1	0	0	0	1	RESERVED			
2	0	0	1	0	$2(G_M \times M)$	$2(G_M \times M)$	MUTE	MUTE
3	0	0	1	1	$2(G_M \times M)$	$2(G_M \times M)$	$(G_M \times M)$	$(G_M \times M)$
4	0	1	0	0	SD	SD	$(G_M \times M)$	$(G_M \times M)$
5	0	1	0	1	RESERVED			
6	0	1	1	0	RESERVED			
7	0	1	1	1	$2(G_L \times L)$	$2(G_R \times R)$	MUTE	MUTE
8	1	0	0	0	$2(G_L \times L)$	$2(G_R \times R)$	$(G_L \times L)$	$(G_R \times R)$
9	1	0	0	1	SD	SD	$(G_L \times L)$	$(G_R \times R)$
10	1	0	1	0	RESERVED			
11	1	0	1	1	RESERVED			
12	1	1	0	0	$2(G_L \times L) + 2(G_M \times M)$	$2(G_R \times R) + 2(G_M \times M)$	MUTE	MUTE
13	1	1	0	1	$2(G_L \times L) + 2(G_M \times M)$	$2(G_R \times R) + 2(G_M \times M)$	$(G_L \times L) + (G_M \times M)$	$(G_R \times R) + (G_M \times M)$
14	1	1	1	0	SD	SD	$(G_L \times L) + (G_M \times M)$	$(G_R \times R) + (G_M \times M)$
15	1	1	1	1	RESERVED			

M - M_{IN} Input Level

L - L_{IN} Input Level

R - R_{IN} Input Level

G_M - Mono Volume Control Gain

G_L - Left Stereo Volume Control Gain

G_R - Right Stereo Volume Control Gain

SD - Shutdown

MUTE - Mute

Table 6. Texas Instruments 3D Enhancement

LD5	0	Loudspeaker Texas Instruments 3D Off
	1	Loudspeaker Texas Instruments 3D On
RD5	0	Headphone Texas Instruments 3D Off
	1	Headphone Texas Instruments 3D On

Table 7. Wake-up Time Select

CD5	0	Fast Wake-up Setting
	1	Slow Wake-up Setting

I²C COMPATIBLE INTERFACE

The LM4859 uses a serial bus, which conforms to the I²C protocol, to control the chip's functions with two wires: clock (SCL) and data (SDA). The clock line is uni-directional. The data line is bi-directional (open-collector). The maximum clock frequency specified by the I²C standard is 400kHz. In this discussion, the master is the controlling microcontroller and the slave is the LM4859.

The I²C address for the LM4859 is determined using the ADR pin. The LM4859's two possible I²C chip addresses are of the form $111110X_10$ (binary), where $X_1 = 0$, if ADR is logic low; and $X_1 = 1$, if ADR is logic high. If the I²C interface is used to address a number of chips in a system, the LM4859's chip address can be changed to avoid any possible address conflicts.

The bus format for the I²C interface is shown in Figure 34. The bus format diagram is broken up into six major sections:

The "start" signal is generated by lowering the data signal while the clock signal is high. The start signal will alert all devices attached to the I²C bus to check the incoming address against their own address.

The 8-bit chip address is sent next, most significant bit first. The data is latched in on the rising edge of the clock. Each address bit must be stable while the clock level is high.

After the last bit of the address bit is sent, the master releases the data line high (through a pull-up resistor). Then the master sends an acknowledge clock pulse. If the LM4859 has received the address correctly, then it holds the data line low during the clock pulse. If the data line is not held low during the acknowledge clock pulse, then the master should abort the rest of the data transfer to the LM4859.

The 8 bits of data are sent next, most significant bit first. Each data bit should be valid while the clock level is stable high.

After the data byte is sent, the master must check for another acknowledge to see if the LM4859 received the data.

If the master has more data bytes to send to the LM4859, then the master can repeat the previous two steps until all data bytes have been sent.

The "stop" signal ends the transfer. To signal "stop", the data signal goes high while the clock signal is high. The data line should be held high when not in use.

I²C INTERFACE POWER SUPPLY PIN (I^2CV_{DD})

The LM4859's I²C interface is powered up through the I^2CV_{DD} pin. The LM4859's I²C interface operates at a voltage level set by the I^2CV_{DD} pin which can be set independent to that of the main power supply pin V_{DD}. This is ideal whenever logic levels for the I²C interface are dictated by a microcontroller or microprocessor that is operating at a lower supply voltage than the main battery of a portable system.

TEXAS INSTRUMENTS 3D ENHANCEMENT

The LM4859 features a 3D audio enhancement effect that widens the perceived soundstage from a stereo audio signal. The 3D audio enhancement improves the apparent stereo channel separation whenever the left and right speakers are too close to one another, due to system size constraints or equipment limitations.

An external RC network, shown in Figure 1, is required to enable the 3D effect. There are separate RC networks for both the stereo loudspeaker outputs as well as the stereo headphone outputs, so the 3D effect can be set independently for each set of stereo outputs.

The amount of the 3D effect is set by the R_{3D} resistor. Decreasing the value of R_{3D} will increase the 3D effect. The C_{3D} capacitor sets the low cutoff frequency of the 3D effect. Increasing the value of C_{3D} will decrease the low cutoff frequency at which the 3D effect starts to occur, as shown by Equation 1.

$$f_{3D(-3dB)} = 1 / 2\pi(R_{3D})(C_{3D}) \quad (1)$$

Activating the 3D effect will cause an increase in gain by a multiplication factor of (1 + 9kΩ/R_{3D}). Setting R_{3D} to 9kΩ will result in a gain increase by a multiplication factor of (1+ 9kΩ/9kΩ) = 2 or 6dB whenever the 3D effect is activated. The volume control can be programmed through the I^2C compatible interface to compensate for the extra 6dB increase in gain. For example, if the stereo volume control is set at 0dB (11011 from Table 4) before the 3D effect is activated, the volume control should be programmed to –6dB (10111 from Table 4) immediately after the 3D effect has been activated. Setting R_{3D} = 20kΩ and C_{3D} = 0.22µF allows the LM4859 to produce a pronounced 3D effect with a minimal increase in output noise.

EXPOSED-DAP MOUNTING CONSIDERATIONS

The LM4859's exposed-DAP (die attach paddle) package (SP) provides a low thermal resistance between the die and the PCB to which the part is mounted and soldered. This allows rapid heat transfer from the die to the surrounding PCB copper area heatsink, copper traces, ground plane, and finally, surrounding air. The result is a low voltage audio power amplifier that produces 1.6W dissipation in a 4Ω load at ≤ 1% THD+N and over 1.8W in a 3Ω load at 10% THD+N. This high power is achieved through careful consideration of necessary thermal design. Failing to optimize thermal design may compromise the LM4859's high power performance and activate unwanted, though necessary, thermal shutdown protection.

The SP package must have its DAP soldered to a copper pad on the PCB. The DAP's PCB copper pad is then, ideally, connected to a large plane of continuous unbroken copper. This plane forms a thermal mass, heat sink, and radiation area. Place the heat sink area on either outside plane in the case of a two-sided or multi-layer PCB. (The heat sink area can also be placed on an inner layer of a multi-layer board. The thermal resistance, however, will be higher.) Connect the DAP copper pad to the inner layer or backside copper heat sink area with 9 (3 X 3) (SP) vias. The via diameter should be 0.012in - 0.013in with a 1.27mm pitch. Ensure efficient thermal conductivity by plugging and tenting the vias with plating and solder mask, respectively.

Best thermal performance is achieved with the largest practical copper heat sink area. If the heatsink and amplifier share the same PCB layer, a nominal $2in^2$ area is necessary for 5V operation with a 4Ω load. Heatsink areas not placed on the same PCB layer as the LM4859 should be $4in^2$ for the same supply voltage and load resistance. The last two area recommendations apply for 25°C ambient temperature. Increase the area to compensate for ambient temperatures above 25°C. In all circumstances and under all conditions, the junction temperature must be held below 150°C to prevent activating the LM4859's thermal shutdown protection. An example PCB layout for the exposed-DAP SP package is shown in the Demonstration Board Layout section.

PCB LAYOUT AND SUPPLY REGULATION CONSIDERATIONS FOR DRIVING 3Ω AND 4Ω LOADS

Power dissipated by a load is a function of the voltage swing across the load and the load's impedance. As load impedance decreases, load dissipation becomes increasingly dependent on the interconnect (PCB trace and wire) resistance between the amplifier output pins and the load's connections. Residual trace resistance causes a voltage drop, which results in power dissipated in the trace and not in the load as desired. For example, 0.1Ω trace resistance reduces the output power dissipated by a 4Ω load from 1.6W to 1.5W. The problem of decreased load dissipation is exacerbated as load impedance decreases. Therefore, to maintain the highest load dissipation and widest output voltage swing, PCB traces that connect the output pins to a load must be as wide as possible.

Poor power supply regulation adversely affects maximum output power. A poorly regulated supply's output voltage decreases with increasing load current. Reduced supply voltage causes decreased headroom, output signal clipping, and reduced output power. Even with tightly regulated supplies, trace resistance creates the same effects as poor supply regulation. Therefore, making the power supply traces as wide as possible helps maintain full output voltage swing.

BRIDGE CONFIGURATION EXPLANATION

The LM4859 consists of two sets of bridged-tied amplifier pairs that drive the left loudspeaker (LLS) and the right loudspeaker (RLS). For this discussion, only the LLS bridge-tied amplifier pair will be referred to. The LM4859 drives a load, such as a speaker, connected between outputs, LLS+ and LLS-. In the LLS amplifier block, the output of the amplifier that drives LLS- serves as the input to the unity gain inverting amplifier that drives LLS+.

This results in both amplifiers producing signals identical in magnitude, but 180° out of phase. Taking advantage of this phase difference, a load is placed between LLS- and LLS+ and driven differentially (commonly referred to as 'bridge mode'). This results in a differential or BTL gain of:

$$A_{VD} = 2(R_f / R_i) = 2 \quad (2)$$

Both the feedback resistor, R_f, and the input resistor, R_i, are internally set.

Bridge mode amplifiers are different from single-ended amplifiers that drive loads connected between a single amplifier's output and ground. For a given supply voltage, bridge mode has a distinct advantage over the single-ended configuration: its differential output doubles the voltage swing across the load. Theoretically, this produces four times the output power when compared to a single-ended amplifier under the same conditions. This increase in attainable output power assumes that the amplifier is not current limited and that the output signal is not clipped.

Another advantage of the differential bridge output is no net DC voltage across the load. This is accomplished by biasing LLS- and LLS+ outputs at half-supply. This eliminates the coupling capacitor that single supply, single-ended amplifiers require. Eliminating an output coupling capacitor in a typical single-ended configuration forces a single-supply amplifier's half-supply bias voltage across the load. This increases internal IC power dissipation and may permanently damage loads such as speakers.

POWER DISSIPATION

Power dissipation is a major concern when designing a successful single-ended or bridged amplifier.

A direct consequence of the increased power delivered to the load by a bridge amplifier is higher internal power dissipation. The LM4859 has 2 sets of bridged-tied amplifier pairs driving LLS and RLS. The maximum internal power dissipation operating in the bridge mode is twice that of a single-ended amplifier. From Equation 3 and Equation 4, assuming a 5V power supply and an 8Ω load, the maximum power dissipation for LLS and RLS is 634mW per channel.

$$P_{DMAX\text{-}LLS} = 4(V_{DD})^2 / (2\pi^2 R_L)\text{: Bridged} \quad (3)$$

$$P_{DMAX\text{-}RLS} = 4(V_{DD})^2 / (2\pi^2 R_L)\text{: Bridged} \quad (4)$$

The LM4859 also has a pair of single-ended amplifiers driving LHP and RHP. The maximum internal power dissipation for ROUT and LOUT is given by Equation 5 and Equation 6. From Equation 5 and Equation 6, assuming a 5V power supply and a 32Ω load, the maximum power dissipation for LOUT and ROUT is 40mW per channel.

$$P_{DMAX\text{-}LHP} = (V_{DD})^2 / (2\pi^2 R_L)\text{: Single-ended} \quad (5)$$

$$P_{DMAX\text{-}RHP} = (V_{DD})^2 / (2\pi^2 R_L)\text{: Single-ended} \quad (6)$$

The maximum internal power dissipation of the LM4859 occurs during output modes 3, 8, and 13 when both loudspeaker and headphone amplifiers are simultaneously on; and is given by Equation 7.

$$P_{DMAX\text{-}TOTAL} = P_{DMAX\text{-}LLS} + P_{DMAX\text{-}RLS} + P_{DMAX\text{-}LHP} + P_{DMAX\text{-}RHP} \quad (7)$$

The maximum power dissipation point given by Equation 7 must not exceed the power dissipation given by Equation 8:

$$P_{DMAX}' = (T_{JMAX} - T_A) / \theta_{JA} \quad (8)$$

The LM4859's T_{JMAX} = 150°C. In the SP package, the LM4859's θ_{JA} is 42°C/W. At any given ambient temperature T_A, use Equation 8 to find the maximum internal power dissipation supported by the IC packaging. Rearranging Equation 8 and substituting $P_{DMAX\text{-}TOTAL}$ for P_{DMAX}' results in Equation 9. This equation gives the maximum ambient temperature that still allows maximum stereo power dissipation without violating the LM4859's maximum junction temperature.

$$T_A = T_{JMAX} - P_{DMAX\text{-}TOTAL}\, \theta_{JA} \quad (9)$$

For a typical application with a 5V power supply, stereo 8Ω loudspeaker load, and the stereo 32Ω headphone load, the maximum ambient temperature that allows maximum stereo power dissipation without exceeding the maximum junction temperature is approximately 93.4°C for the SP package.

$$T_{JMAX} = P_{DMAX\text{-}TOTAL}\, \theta_{JA} + T_A \quad (10)$$

Equation 10 gives the maximum junction temperature T_{JMAX}. If the result violates the LM4859's 150°C, reduce the maximum junction temperature by reducing the power supply voltage or increasing the load resistance. Further allowance should be made for increased ambient temperatures.

The above examples assume that a device is a surface mount part operating around the maximum power dissipation point. Since internal power dissipation is a function of output power, higher ambient temperatures are allowed as output power or duty cycle decreases. If the result of Equation 7 is greater than that of Equation 8, then decrease the supply voltage, increase the load impedance, or reduce the ambient temperature. If these measures are insufficient, a heat sink can be added to reduce θ_{JA}. The heat sink can be created using additional copper area around the package, with connections to the ground pin(s), supply pin and amplifier output pins. External, solder attached SMT heatsinks such as the Thermalloy 7106D can also improve power dissipation. When adding a heat sink, the θ_{JA} is the sum of θ_{JC}, θ_{CS}, and θ_{SA}. (θ_{JC} is the junction-to-case thermal impedance, θ_{CS} is the case-to-sink thermal impedance, and θ_{SA} is the sink-to-ambient thermal impedance.) Refer to the Typical Performance Characteristics(1) curves for power dissipation information at lower output power levels.

POWER SUPPLY BYPASSING

As with any power amplifier, proper supply bypassing is critical for low noise performance and high power supply rejection. Applications that employ a 5V regulator typically use a 10µF in parallel with a 0.1µF filter capacitors to stabilize the regulator's output, reduce noise on the supply line, and improve the supply's transient response. However, their presence does not eliminate the need for a local 1.0µF tantalum bypass capacitance connected between the LM4859's supply pins and ground. Keep the length of leads and traces that connect capacitors between the LM4859's power supply pin and ground as short as possible.

SELECTING EXTERNAL COMPONENTS

Input Capacitor Value Selection

Amplifying the lowest audio frequencies requires a high value input coupling capacitor (C_i in Figure 1). In many cases, however, the speakers used in portable systems, whether internal or external, have little ability to reproduce signals below 50Hz. Applications using speakers with this limited frequency response reap little improvement; by using a large input capacitor.

The internal input resistor (R_i) and the input capacitor (C_i) produce a high pass filter cutoff frequency that is found using Equation 11.

$$f_c = 1 / (2\pi R_i C_i) \quad (11)$$

As an example when using a speaker with a low frequency limit of 50Hz and R_i = 20kΩ, C_i, using Equation 11 is 0.19µF. The 0.22µF C_i shown in Figure 36 allows the LM4859 to drive high efficiency, full range speaker whose response extends below 40Hz.

Output Capacitor Value Selection

Amplifying the lowest audio frequencies also requires the use of a high value output coupling capacitor (C_O in Figure 1). A high value output capacitor can be expensive and may compromise space efficiency in portable design.

The speaker load (R_L) and the output capacitor (C_O) form a high pass filter with a low cutoff frequency determined using Equation 12.

$$f_c = 1 / (2\pi R_L C_O) \quad (12)$$

When using a typical headphone load of R_L = 32Ω with a low frequency limit of 50Hz, C_O is 99µF.

The 100µF C_O shown in Figure 36 allows the LM4859 to drive a headphone whose frequency response extends below 50Hz.

Bypass Capacitor Value Selection

Besides minimizing the input capacitor size, careful consideration should be paid to value of C_B, the capacitor connected to the BYPASS pin. Since C_B determines how fast the LM4859 settles to quiescent operation, its value is critical when minimizing turn-on pops. The slower the LM4859's outputs ramp to their quiescent DC voltage (nominally $V_{DD}/2$), the smaller the turn-on pop. Choosing C_B equal to 2.2µF along with a small value of C_i (in the range of 0.1µF to 0.39µF), produces a click-less and pop-less shutdown function. As discussed above, choosing C_i no larger than necessary for the desired bandwidth helps minimize clicks and pops. C_B's value should be in the range of 5 times to 10 times the value of C_i. This ensures that output transients are eliminated

(1) "0dB gain" refers to the volume control gain setting of M_{IN}, L_{IN}, and R_{IN} set at 0dB.

when the LM4859 transitions in and out of shutdown mode. Connecting a 2.2µF capacitor, C_B, between the BYPASS pin and ground improves the internal bias voltage's stability and improves the amplifier's PSRR. The PSRR improvements increase as the bypass pin capacitor value increases. However, increasing the value of C_B will increase wake-up time. The selection of bypass capacitor value, C_B, depends on desired PSRR requirements, click and pop performance, wake-up time, system cost, and size constraints.

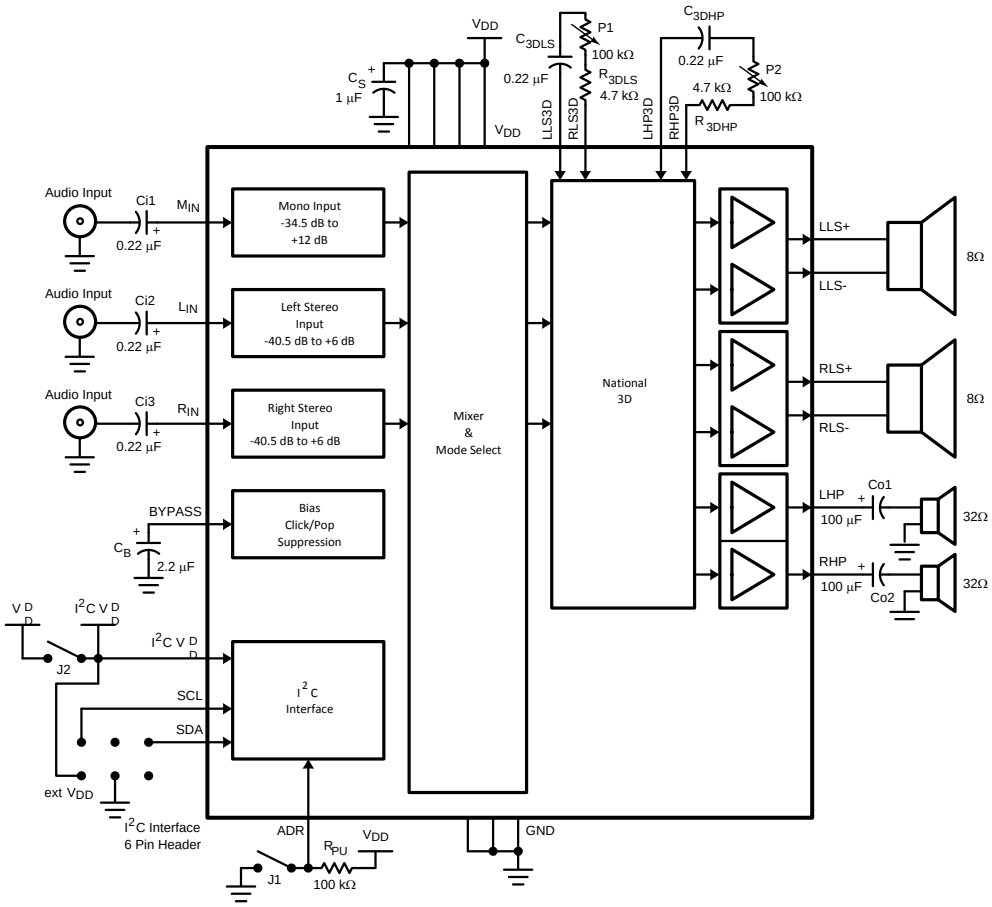


Figure 36. Reference Design Board Schematic

Demonstration Board Layout

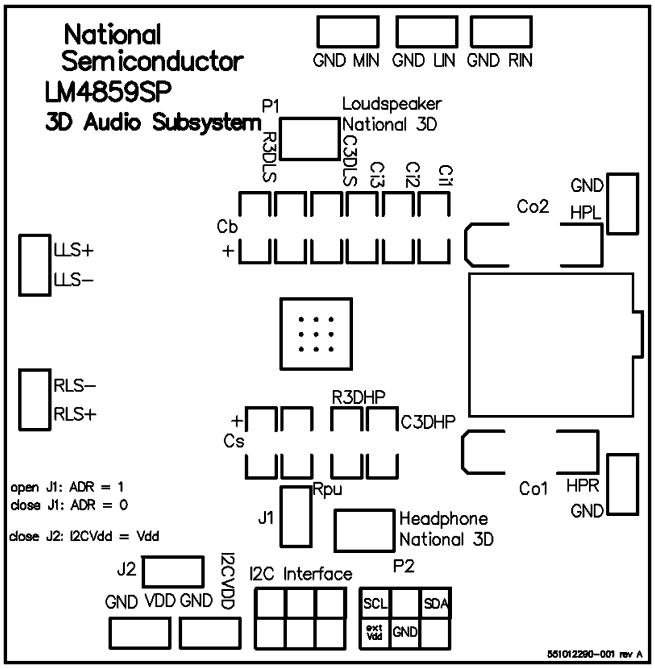


Figure 37. Recommended SP PCB Layout: Silkscreen Layer

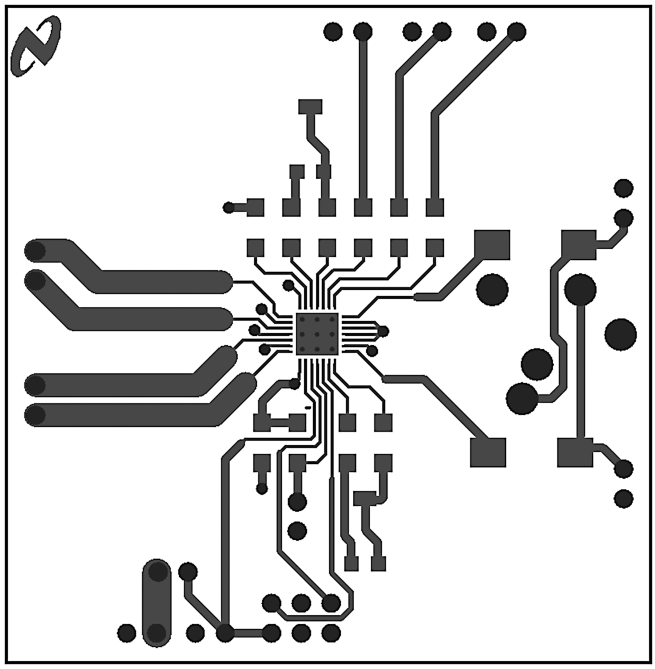


Figure 38. Recommended SP PCB Layout: Top Layer

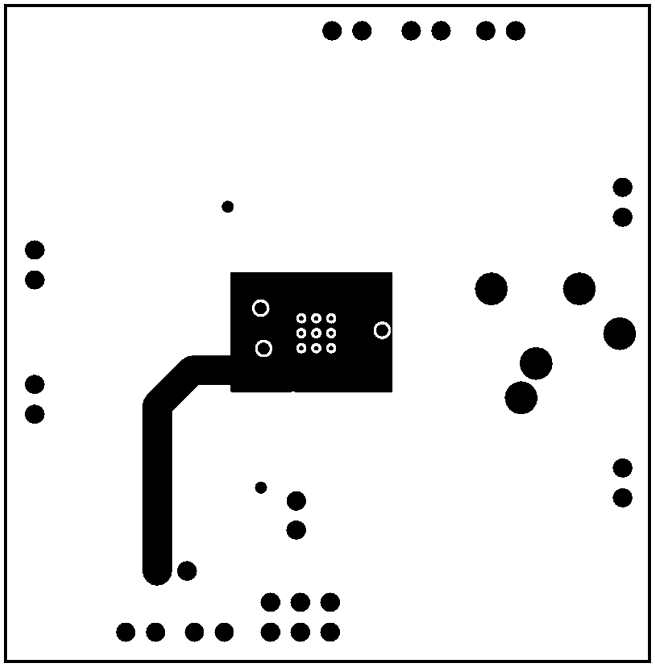


Figure 39. Recommended SP PCB Layout: Mid Layer

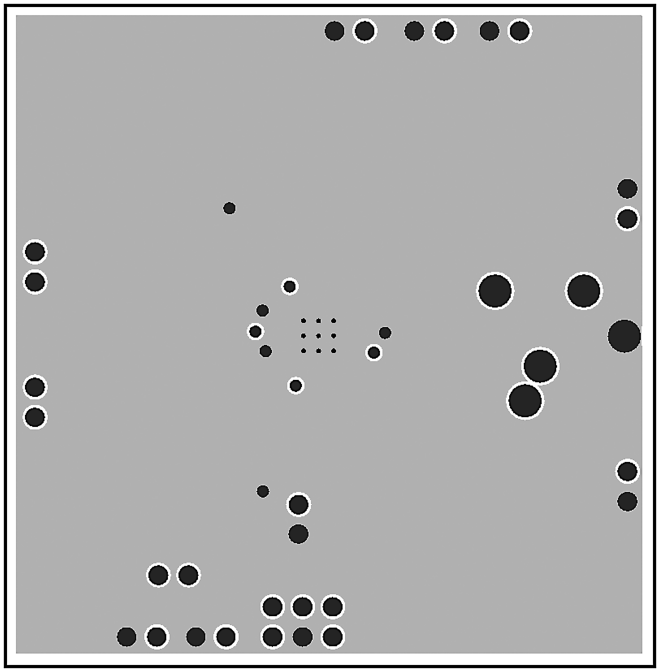


Figure 40. Recommended SP PCB Layout: Bottom Layer

Revision History

Rev	Date	Description
1.1	6/02/05	Added Modes 9 and 14 into Mode 4 (Conditions) for the Idd under Elect.Char tables 5V and 3V, then re-released D/S to the WEB (per Alvin Fok). (MC)
1.2	06/06/06	Edited the DSBGA markings (per Alvin F.), then re-released D/S to the WEB.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
LM4859SP/NOPB	ACTIVE	UQFN	NJD	28	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	L4859SP	Samples
LM4859SPX/NOPB	ACTIVE	UQFN	NJD	28	4500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	L4859SP	Samples
LM4859TL/NOPB	ACTIVE	DSBGA	YZR	30	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	GF1	Samples
LM4859TLX/NOPB	ACTIVE	DSBGA	YZR	30	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	GF1	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

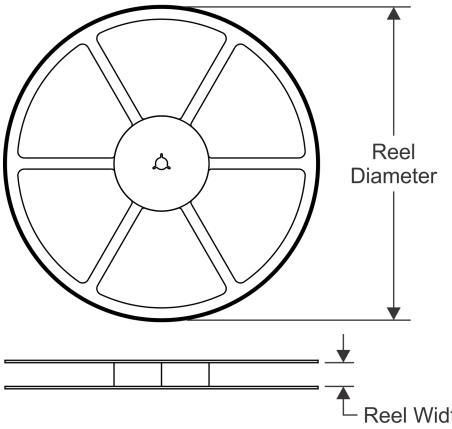
(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

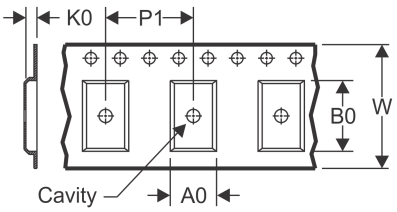
(4) Only one of markings shown within the brackets will appear on the physical device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

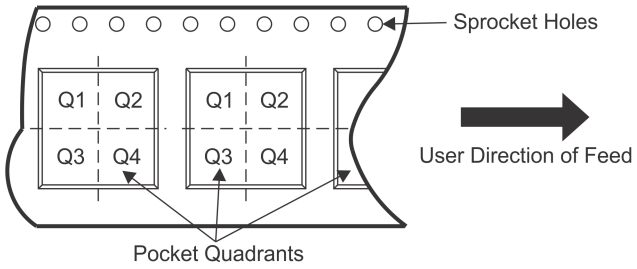


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

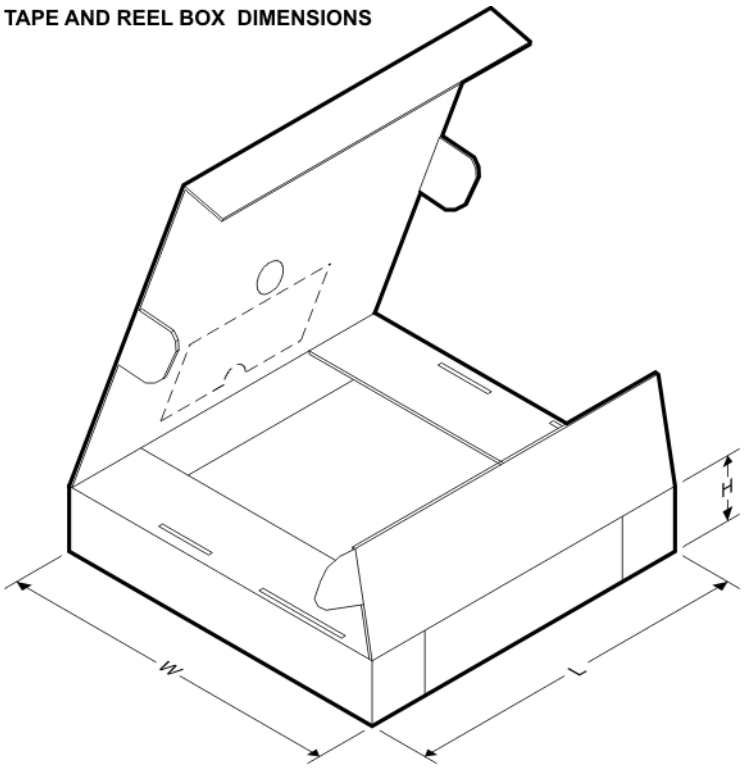
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM4859SP/NOPB	UQFN	NJD	28	1000	178.0	12.4	5.3	5.3	1.3	8.0	12.0	Q1
LM4859SPX/NOPB	UQFN	NJD	28	4500	330.0	12.4	5.3	5.3	1.3	8.0	12.0	Q1
LM4859TL/NOPB	DSBGA	YZR	30	250	178.0	8.4	2.74	3.15	0.76	4.0	8.0	Q1
LM4859TLX/NOPB	DSBGA	YZR	30	3000	178.0	8.4	2.74	3.15	0.76	4.0	8.0	Q1

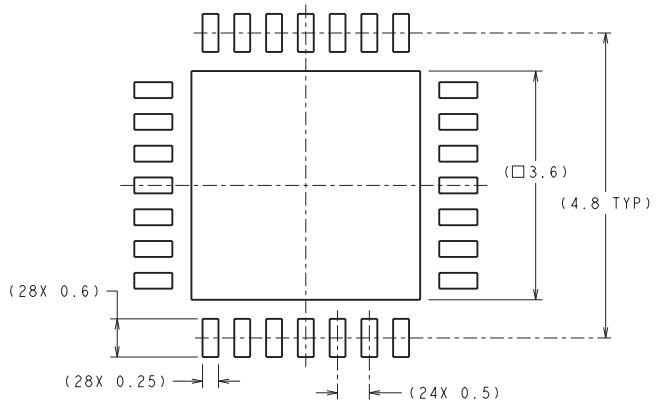
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

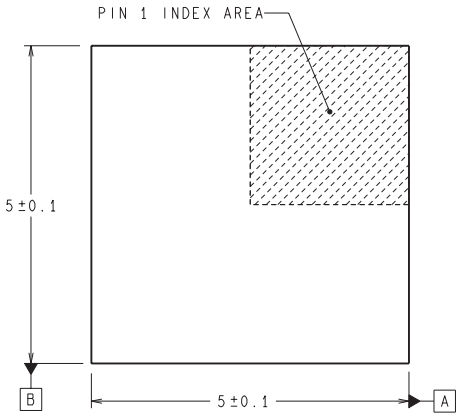
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM4859SP/NOPB	UQFN	NJD	28	1000	203.0	190.0	41.0
LM4859SPX/NOPB	UQFN	NJD	28	4500	349.0	337.0	45.0
LM4859TL/NOPB	DSBGA	YZR	30	250	203.0	190.0	41.0
LM4859TLX/NOPB	DSBGA	YZR	30	3000	206.0	191.0	90.0

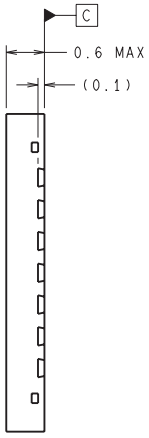
NJD0028A

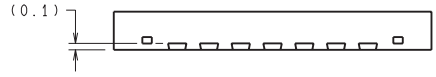


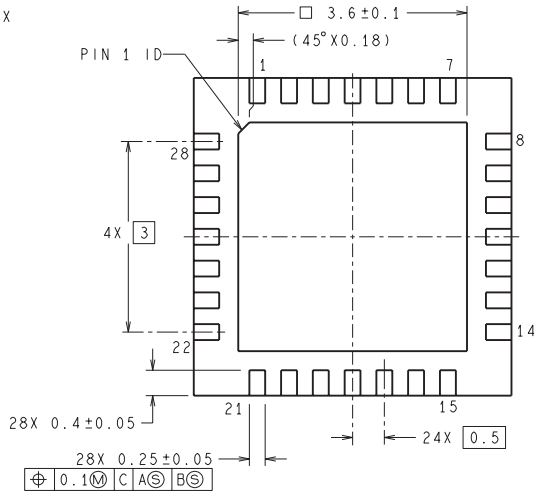
RECOMMENDED LAND PATTERN

DIMENSIONS ARE IN MILLIMETERS
DIMENSIONS IN ( ) FOR REFERENCE ONLY



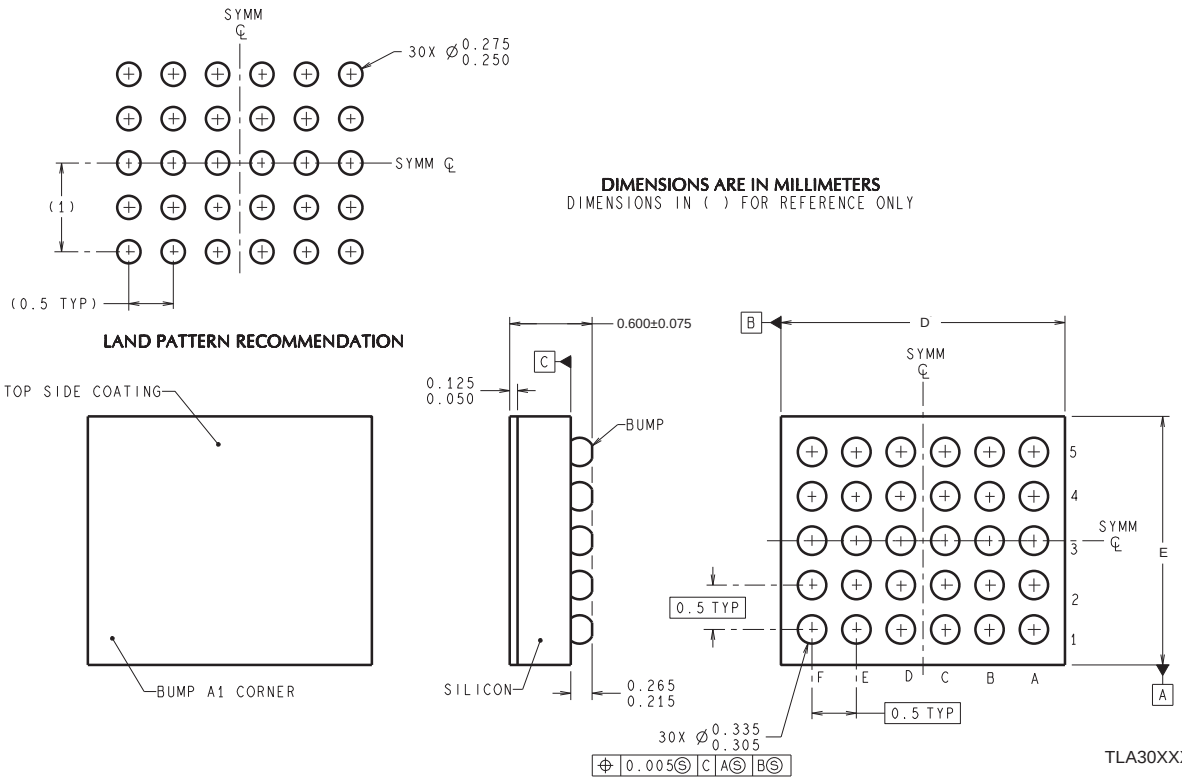






SPA28A (Rev A)

YZR0030



D: Max = 3.01 mm, Min = 2.909 mm

E: Max = 2.601 mm, Min = 2.5 mm

4215057/A 12/12

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.

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