LM48903 Boomer® Audio Power Amplifier Series Stereo Class D Spatial Array

Check for Samples: LM48903

FEATURES

- **Spatial Sound Processing**
- **I²S Input**
- **Stereo, Analog, Differential-Input ADC**
- **Edge Rate Control**
- **Short Circuit and Thermal Overload Protection**
- **Minimum external components**
- **Click and Pop suppression**
- **Micro-power shutdown**
- **Available in space-saving micro SMD package**

APPLICATIONS

- **Smart Phones**
- **Portable Gaming**
- **Tablets**
- **Multimedia Devices**
- **MP3 Player Accessories**

DESCRIPTION

The LM48903 is a stereo Class D amplifier that utilizes TI's proprietary spatial sound processor to create an enhanced sound stage for portable multimedia devices. The Class D output stages feature National's edge rate control (ERC) PWM architecture that significantly reduces RF emissions while preserving audio quality and efficiency.

The LM48903's flexible I^2S interface is compatible with standard serial audio interfaces. A stereo differential-input ADC gives the device the ability to process analog stereo audio signals.

The LM48903 is configured through an I^2C compatible interface and is capable of delivering 1.7W/channel of continuous output power into an 8Ω load with less than 10% THD+N.

Output short circuit and thermal overload protection prevent the device from being damaged during fault conditions. Click and pop suppression eliminates audible transients on power-up/down and during shutdown. The LM48903 is available in space saving micro SMD package.

Table 1. Key Specifications

	VALUE	UNIT
■ SNR (A-Weighted)	90dBA (typ)	■ Output Power/channel, PV_{DD} = 5V
R_L = 8Ω, THD+N ≤ 1%	1.3	W (typ)
■ THD+N	0.08% (typ)	
■ Efficiency/Channel	91% (typ)	
■ PSRR at 217Hz	69	dB (typ)

Typical Application

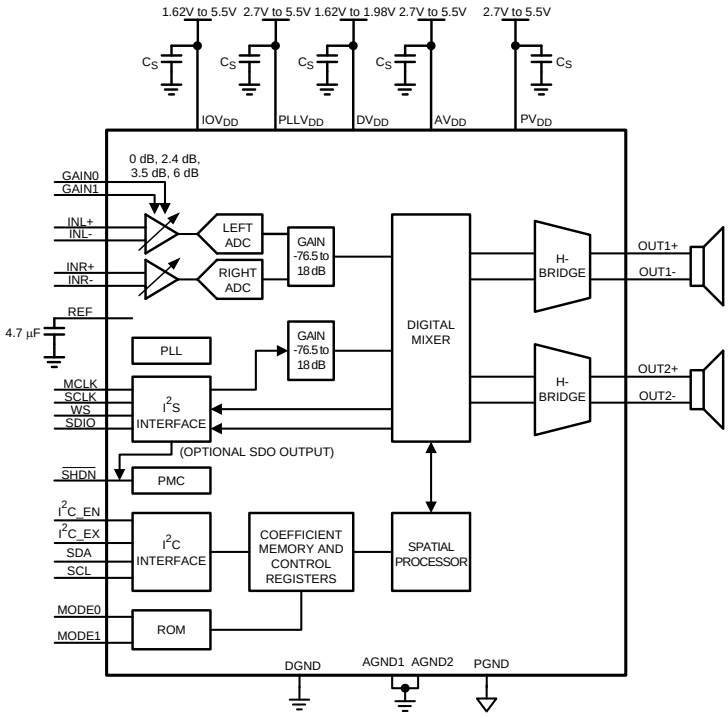

Figure 1. Typical Audio Amplifier Application Circuit

Connection Diagram

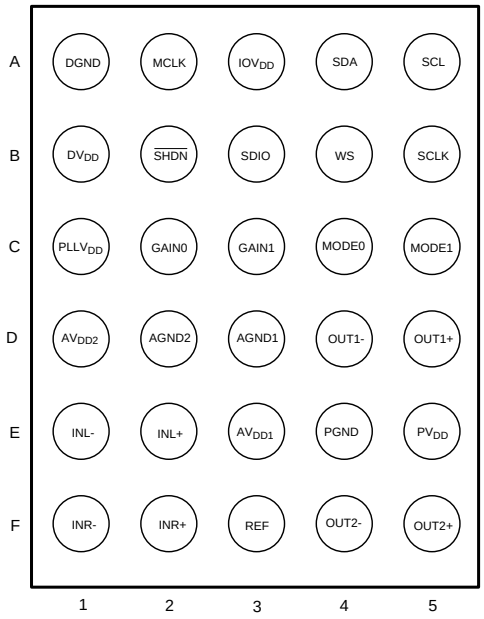

Figure 2. Top View

30–Bump Marking

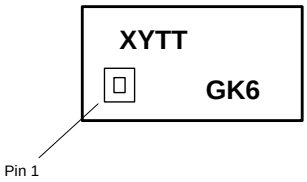

Figure 3. Top View
XY = Date code
TT = Die traceability
G = Boomer Family
K6 = LM48903TL

Table 2. Bump Description

BUMP	NAME	DESCRIPTION
A1	DGND	Digital Ground
A2	MCLK	Master Clock
A3	IOV_{DD}	Digital Interface Power Supply
A4	SDA	I^2C Serial Data Input
A5	SCL	I^2C Clock Input
B1	DV_{DD}	Digital Power Supply
B2	$\overline{SHDN}$	Active Low Shutdown. Connect to VDD for normal operation.
B3	SDIO	I^2S Serial Data Input/Output
B4	WS	I^2S Word Select Input
B5	SCLK	Serial Clock Input
C1	$PLLV_{DD}$	PLL Power Supply
C2	GAIN0	Gain Setting Input 0
C3	GAIN1	Gain Setting Input 1
C4	MODE0	Spatial Mode Control Input 0
C5	MODE1	Spatial Mode Control Input 1
D1	AV_{DD2}	ADC Analog Power Supply
D2	AGND2	ADC Analog Ground
D3	AGND1	Modulator Analog Ground
D4	OUT1-	Channel 1 Inverting Output. Connect to OUT2- in Parallel Mode
D5	OUT1+	Channel 1 Non-Inverting Output. Connect to OUT2+ in Parallel Mode
E1	INL-	Left Channel Inverting Analog Input
E2	INL+	Left Channel Non-Inverting Analog Input
E3	AV_{DD1}	Modulator Analog Power Supply
E4	PGND	Power Ground
E5	PV_{DD}	Class D Power Supply
F1	INR-	Right Channel Inverting Analog Input
F2	INR+	Right Channel Non-Inverting Analog Input
F3	REF	ADC Reference Bypass
F4	OUT2-	Channel 2 Inverting Output. Connect to OUT1- in Parallel Mode.
F5	OUT2+	Channel 2 Non-Inverting Output. Connect to OUT1+ in Parallel Mode.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings (1) (2)

Supply Voltage	
AV_{DD}, PV_{DD}, PLV_{DD}, IOV_{DD} (1)	6V
Supply Voltage, DV_{DD} (1)	2.2V
Storage Temperature	−65°C to + 150°C
Input Voltage	−0.3V to V_{DD} + 0.3V
Power Dissipation (3)	Internally limited
ESD Susceptibility (4)	2000V
ESD Susceptibility (5)	150V
Junction Temperature	150°C
Thermal Resistance	
θ_{JA} (TLA30)	54°C/W

(1) "*Absolute Maximum Ratings*" indicate limits beyond which damage to the device may occur, including inoperability and degradation of device reliability and/or performance. Functional operation of the device and/or non-degradation at the *Absolute Maximum Ratings* or other conditions beyond those indicated in the *Recommended Operating Conditions* is not implied. The *Recommended Operating Conditions* indicate conditions at which the device is functional and the device should not be operated beyond such conditions. All voltages are measured with respect to the ground pin, unless otherwise specified.
(2) The *Electrical Characteristics* tables list guaranteed specifications under the listed *Recommended Operating Conditions* except as otherwise modified or specified by the *Electrical Characteristics Conditions* and/or Notes. Typical specifications are estimations only and are not guaranteed.
(3) The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{JMAX}, θ_{JA}, and the ambient temperature, T_A. The maximum allowable power dissipation is $P_{DMAX} = (T_{JMAX} - T_A) / \theta_{JA}$ or the given in *Absolute Maximum Ratings*, whichever is lower.
(4) Human body model, applicable std. JESD22-A114C.
(5) Machine model, applicable std. JESD22-A115-A.

Operating Ratings

Temperature Range	
$T_{MIN} \le T_A \le T_{MAX}$	$-40°C \le T_A \le +85°C$
Supply Voltage	
AV_{DD}	$2.7V \le AV_{DD} \le 5.5V$
PV_{DD}	$2.7V \le PV_{DD} \le 5.5V$
$PLLV_{DD}$	$2.7V \le PLLV_{DD} \le 5.5V$
IOV_{DD}	$1.62V \le IOV_{DD} \le 5.5V$
DV_{DD}	$1.62V \le DV_{DD} \le 1.98V$

Electrical Characteristics $PV_{DD} = AV_{DD}$, $IOV_{DD} = PLLV_{DD} = 3.6V$, $DV_{DD} = 1.8$ (1) (2)

The following specifications apply for A_V = 0dB, C_{REF} = 4.7µF, R_L = 8Ω, f = 1kHz, unless otherwise specified. Limits apply for T_A = 25°C.

Symbol	Parameter	Conditions	LM48903			Units (Limits)
			Min (2)	Typ (3)	Max (2)	
AV_{DD}	Analog Supply Voltage Range		2.7		5.5	V
PV_{DD}	Amplifier Supply Voltage Range		2.7		5.5	V
$PLLV_{DD}$	PLL Supply Voltage Range		2.7		5.5	V
IOV_{DD}	Interface Supply Voltage Range		1.62		5.5	V
DV_{DD}	Digital Supply Voltage Range		1.62		1.98	V
AI_{DD}	Analog Quiescent Supply Current			15.2	19	mA
PI_{DD}	Amplifier Quiescent Supply Current	R_L = 8Ω		2.6		mA
$PLLI_{DD}$	PLL Quiescent Supply Current			1.3		mA
DI_{DD}	Quiescent Digital Power Supply Current			5.4	5.8	mA
I_{SD}	Shutdown Current (Analog, Amplifier and PLL Supplies)	Shutdown Enabled		0.4	3.5	µA
DI_{STBY}	Digital Standby Current			30		µA
DI_{SD}	Digital Shutdown Current	Shutdown Enabled		6.6	10	µA
V_{OS}	Differential Output Offset Voltage	V_{IN} = 0	–7.5	0.8	7.5	mV
T_{WU}	Wake-up Time	Power Up (Device Initialization)		150		ms
		From Shutdown		28.5		ms
f_{SW}	Switching Frequency	f_S = 48kHz		384		kHz
P_O	Output Power/Channel	R_L = 4Ω, THD+N = 10% f = 1kHz, 22kHz BW				
		V_{DD} = 5V		2.8		W
		V_{DD} = 3.6V		1.4		W
		R_L = 4Ω, THD+N = 1% f = 1kHz, 22kHz BW				
		V_{DD} = 5V		2.2		W
		V_{DD} = 3.6V		1.2		W
		R_L = 8Ω, THD+N = 10% f = 1kHz, 22kHz BW				
		V_{DD} = 5V		1.7		W
		V_{DD} = 3.6V		860		mW
		R_L = 8Ω, THD+N = 1% f = 1kHz, 22kHz BW				
		V_{DD} = 5V		1.3		W
		V_{DD} = 3.6V	500	650		mW
P_O	Output Power (Parallel Mode)	R_L = 4Ω, THD+N = 10%, f = 1kHz, 22kHz BW				
		V_{DD} = 5V		3.3		W
		V_{DD} = 3.6V		1.7		W
		R_L = 4Ω, THD+N = 1%, f = 1kHz, 22kHz BW				
		V_{DD} = 5V		2.5		W
		V_{DD} = 3.6V		1.2		W
THD+N	Total Harmonic Distortion + Noise	P_O = 350mW, f = 1kHz, R_L = 8Ω		0.08		%

(1) The *Electrical Characteristics* tables list guaranteed specifications under the listed *Recommended Operating Conditions* except as otherwise modified or specified by the *Electrical Characteristics Conditions* and/or Notes. Typical specifications are estimations only and are not guaranteed.
(2) R_L is a resistive load in series with two inductors to simulate an actual speaker load. For R_L = 8Ω, the load is 15µH+8Ω+15µH. For R_L = 4Ω, the load is 15µH+4Ω+15µH.
(3) Datasheet min/max specification limits are guaranteed by design, test, or statistical analysis.

Electrical Characteristics $PV_{DD} = AV_{DD}$, $IOV_{DD} = PLLV_{DD} = 3.6V$, $DV_{DD} = 1.8$ (1) (2) (continued)

The following specifications apply for A_V = 0dB, C_{REF} = 4.7µF, R_L = 8Ω, f = 1kHz, unless otherwise specified. Limits apply for T_A = 25°C.

Symbol	Parameter	Conditions	LM48903			Units (Limits)
			Min (2)	Typ (3)	Max (2)	
PSRR	Power Supply Rejection Ratio (ADC Path)	V_{RIPPLE} = 200mV_{P-P} sine, Inputs AC GND, C_{IN} = 1µF				
		f_{RIPPLE} = 217Hz, Applied to PV_{DD}		69		dB
		f_{RIPPLE} = 217Hz, Applied to DV_{DD}		64		dB
		f_{RIPPLE} = 1kHz, Applied to PV_{DD}	60	68		dB
		f_{RIPPLE} = 1kHz, Applied to DV_{DD}	56	62		dB
		f_{RIPPLE} = 10kHz, Applied to PV_{DD}		62		dB
		f_{RIPPLE} = 10kHz, Applied to DV_{DD}		52		dB
PSRR	Power Supply Rejection Ratio (I^2S Path)	V_{RIPPLE} = 200mV_{P-P} sine, Inputs –∞dBFS				
		f_{RIPPLE} = 217Hz, Applied to PV_{DD}		68		dB
		f_{RIPPLE} = 217Hz, Applied to DV_{DD}		72		dB
		f_{RIPPLE} = 1kHz, Applied to PV_{DD}	60	67		dB
		f_{RIPPLE} = 1kHz, Applied to DV_{DD}	55	69		dB
		f_{RIPPLE} = 10kHz, Applied to PV_{DD}		58		dB
		f_{RIPPLE} = 10kHz, Applied to DV_{DD}		56		dB
CMRR	Common Mode Rejection Ratio	V_{RIPPLE} = 1V_{P-P}, f_{RIPPLE} = 217Hz, A_V = 0dB		78		dB
η	Efficiency/Channel	V_{DD} = 5V, P_O = 1.1W		91		%
		V_{DD} = 3.6V, P_O = 400mW		90		%
η	Efficiency	V_{DD} = 5V, P_O = 1.1W		86		%
		V_{DD} = 3.6V, P_O = 400mW		83		%
SNR	Signal-to-NoiseRatio	ADC Input, P_O = 1W		89		dB
		I^2S Input, P_O = 1W		90		dB
ε_{OS}	Output Noise	Inputs AC GND, A-weighted, A_V = 0dB		130		µV
		I^2S Input		72		µV
X_{TALK}	Crosstalk			72		dB

I²C Interface Characteristics (1) (2)

The following specifications apply for R_{PU} = 1kΩ to IOV_{DD}, unless otherwise specified. Limits apply for T_A = 25°C.

Symbol	Parameter	Conditions	LM48903			Units
			Min (3)	Typ (4)	Max (3)	
V_{IH}	Logic Input High Threshold	SDA, SCL	0.7*IOV_{DD}			V
V_{IL}	Logic Input Low Threshold	SDA, SCL			0.3	mV
V_{OL}	Logic Output Low Threshold	SDA, I_{SDA} = 3.6mA			0.35	V
I_{OH}	Logic Output High Current	SDA, SCL			2	µA
	SCL Frequency				400	kHz
1	Hold Time (repeated START Condition)		0.6			µs
2	Clock Low Time		1.3			µs
3	Clock High Time		600			ns
4	Setup Time for Repeated START condition		600			ns
5	Data Hold Time	Output	300		900	ns
6	Data Setup Time		100			ns
7	SDA Rise Time				300	ns
8	SDA Fall Time				300	ns
9	Setup Time for STOP Condition		600			ns
10	Bus Free Time Between STOP and START Condition		1.3			µs

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(2) The *Electrical Characteristics* tables list guaranteed specifications under the listed *Recommended Operating Conditions* except as otherwise modified or specified by the *Electrical Characteristics Conditions* and/or Notes. Typical specifications are estimations only and are not guaranteed.
(3) Datasheet min/max specification limits are guaranteed by design, test, or statistical analysis.
(4) Typical values represent most likely parametric norms at T_A = +25ºC, and at the *Recommended Operation Conditions* at the time of product characterization and are not guaranteed.

I²S Timing Characteristics (1) (2)

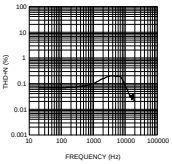
The following specifications apply for DV_{DD} = 1.8V, unless otherwise specified. Limits apply for T_A = 25°C.

Symbol	Parameter	Conditions	LM48903			Units (Limits)
			Min (3)	Typ (4)	Max (3)	
t_{MCLKL}	MCLK Pulse Width Low		16			ns
t_{MCLKH}	MCLK Pulse Width High		16			ns
t_{MCLKY}	MCLK Period		27			ns
t_{BCLKR}	SCLK rise time				3	ns
t_{BCLKCF}	SCLK fall time				3	ns
t_{BCLKDS}	SCLK Duty Cycle			50		%
T_{DL}	LRC Propagation Delay from SCLK falling edge				10	ns
T_{DST}	DATA Setup Time to SCLK Rising Edge		10			ns
T_{DHT}	DATA Hold Time from SCLK Rising Edge		10			ns

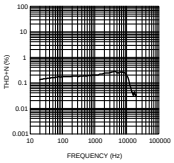
(1) The *Electrical Characteristics* tables list guaranteed specifications under the listed *Recommended Operating Conditions* except as otherwise modified or specified by the *Electrical Characteristics Conditions* and/or Notes. Typical specifications are estimations only and are not guaranteed.
(2) R_L is a resistive load in series with two inductors to simulate an actual speaker load. For R_L = 8Ω, the load is 15µH+8Ω+15µH. For R_L = 4Ω, the load is 15µH+4Ω+15µH.
(3) Datasheet min/max specification limits are guaranteed by design, test, or statistical analysis.
(4) Typical values represent most likely parametric norms at T_A = +25ºC, and at the *Recommended Operation Conditions* at the time of product characterization and are not guaranteed.

Typical Performance Characteristics

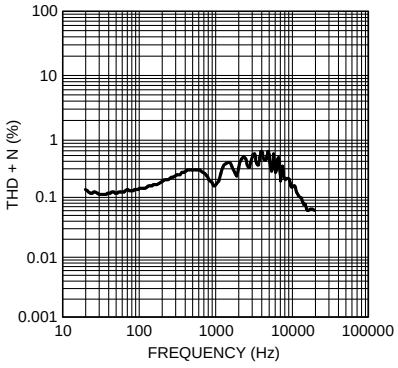
THD+N vs FREQUENCY
V_{DD} = 3.6V, P_{OUT} = 400mW, R_L = 8Ω
Stereo Mode, I^2S Input



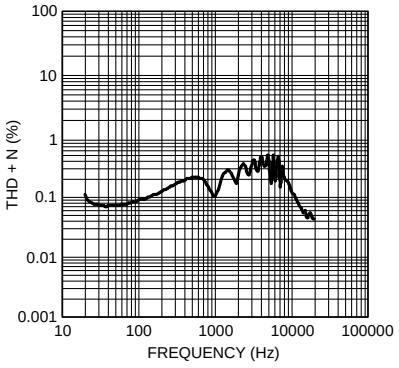
THD+N vs FREQUENCY
V_{DD} = 3.6V, P_{OUT} = 500mW, R_L = 4Ω
Stereo Mode, I^2S Input



THD+N vs FREQUENCY
V_{DD} = 3.6V, P_{OUT} = 250mW, R_L = 4Ω
Stereo Mode, ADC Input

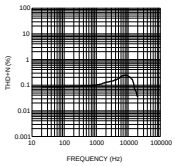


THD+N vs FREQUENCY
V_{DD} = 3.6V, P_{OUT} = 200mW, R_L = 8Ω
Stereo Mode, ADC Input

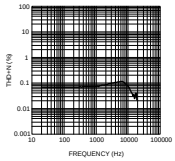


Typical Performance Characteristics (continued)

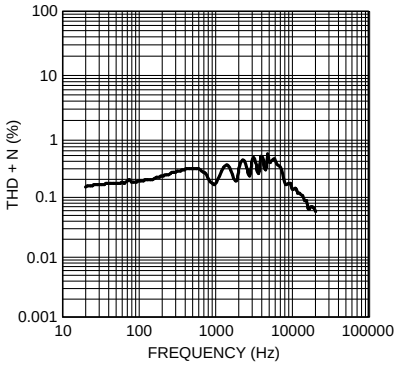
THD+N vs FREQUENCY
V_{DD} = 5V, P_{OUT} = 1.2W, R_L = 4Ω
Stereo Mode, I^2S Input



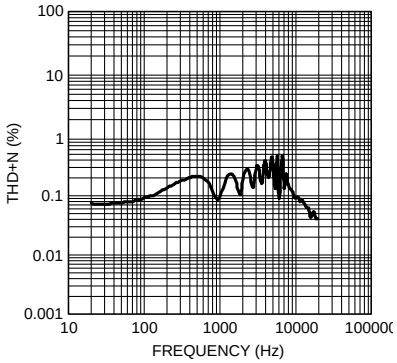
THD+N vs FREQUENCY
V_{DD} = 5V, P_{OUT} = 800mW, R_L = 8Ω
Stereo Mode, I^2S Input



THD+N vs FREQUENCY
V_{DD} = 5V, P_{OUT} = 550mW, R_L = 4 Ω
Stereo Mode, ADC Input

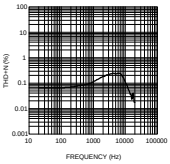


THD+N vs FREQUENCY
V_{DD} = 5V, P_{OUT} = 350mW, R_L = 8Ω
Stereo Mode, ADC Input

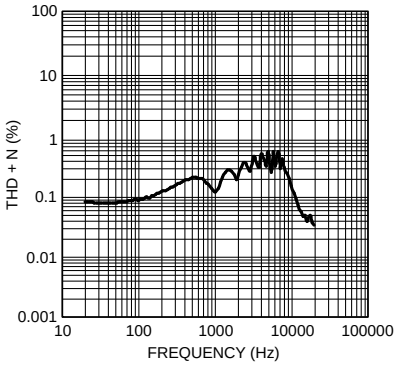


Typical Performance Characteristics (continued)

THD+N vs FREQUENCY
V_{DD} = 3.6V, P_{OUT} = 800mW, R_L = 4Ω
Parallel Mode, I^2S Input

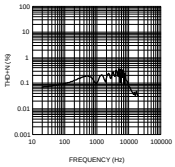


THD+N vs FREQUENCY
V_{DD} = 3.6V, P_{OUT} = 350mW, R_L = 4Ω
Parallel Mode, ADC Input

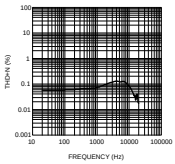


Typical Performance Characteristics (continued)

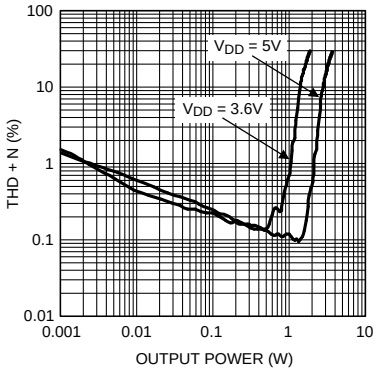
THD+N vs FREQUENCY
V_{DD} = 5V, P_{OUT} = 800mW, R_L = 4Ω
Parallel Mode, I^2S Input



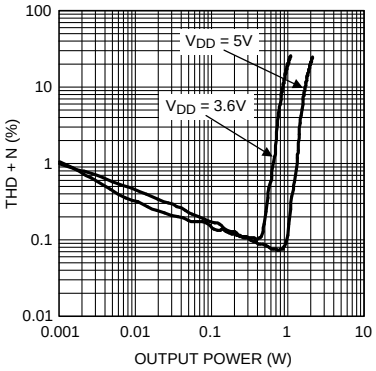
THD+N vs FREQUENCY
V_{DD} = 5V, P_{OUT} = 1.7W, R_L = 4Ω
Parallel Mode, I^2S Input



THD+N vs OUTPUT POWER
R_L = 4Ω, f = 1kHz, Stereo Mode, I^2S Input

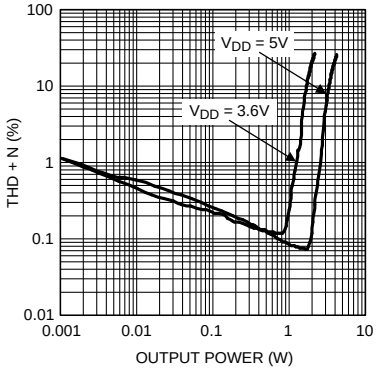


THD+N vs OUTPUT POWER
R_L = 8Ω, f = 1kHz, Stereo Mode, I^2S Input

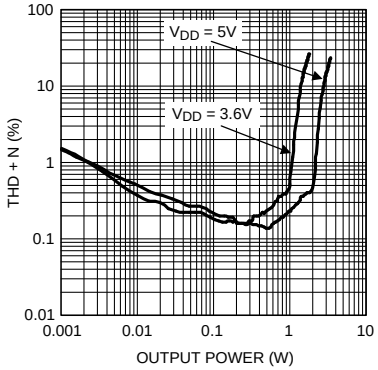


Typical Performance Characteristics (continued)

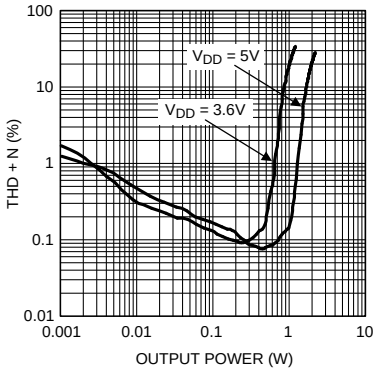
THD+N vs OUTPUT POWER
R_L = 4Ω, f = 1kHz, Parallel Mode, I^2S Input



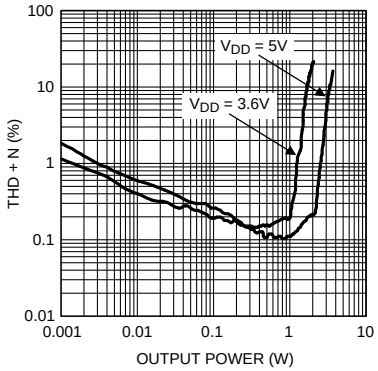
THD+N vs OUTPUT POWER
R_L = 4Ω, f = 1kHz, Stereo Mode, ADC Input



THD+N vs OUTPUT POWER
R_L = 8Ω, f = 1kHz, Stereo Mode, ADC Input

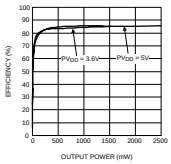


THD+N vs OUTPUT POWER
R_L = 4Ω, f = 1kHz, Parallel Mode, ADC Input

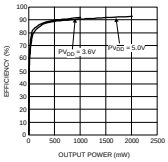


Typical Performance Characteristics (continued)

EFFICIENCY vs OUTPUT POWER
R_L = 4Ω, f = 1kHz, Stereo Mode, ADC Input

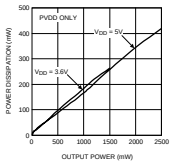


EFFICIENCY vs OUTPUT POWER
R_L = 8Ω, f = 1kHz, Stereo Mode, ADC Input

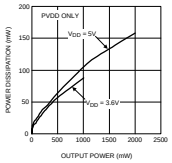


Typical Performance Characteristics (continued)

POWER DISSIPATION
vs
OUTPUT POWER
R_L = 4Ω, Per Channel, Stereo Mode, ADC Input

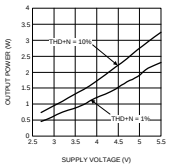


POWER DISSIPATION
vs
OUTPUT POWER
R_L = 8Ω, Per Channel, Stereo Mode, ADC Input

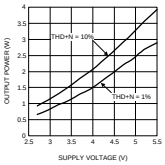


Typical Performance Characteristics (continued)

OUTPUT POWER vs SUPPLY VOLTAGE
R_L = 4Ω, Stereo Mode, ADC Input

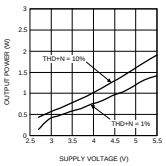


OUTPUT POWER vs SUPPLY VOLTAGE
R_L = 4Ω, Stereo Mode, ADC Input

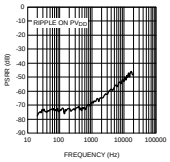


Typical Performance Characteristics (continued)

OUTPUT POWER vs SUPPLY VOLTAGE
R_L = 8Ω, Stereo Mode, ADC Input

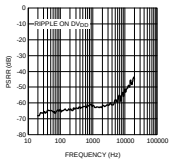


PSRR vs FREQUENCY
PV_{DD} = 5V, V_{RIPPLE} = 200mV_{P-P}, R_L = 8Ω, ADC Input = AC GND

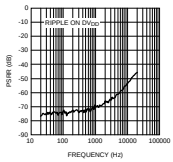


Typical Performance Characteristics (continued)

PSRR vs FREQUENCY
DV_{DD} = 1.8V, V_{RIPPLE} = 200mV_{P-P}, R_L = 8Ω, ADC Input = AC GND

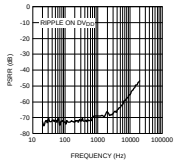


PSRR vs FREQUENCY
PV_{DD} = 5V, V_{RIPPLE} = 200mV_{P-P}, R_L = 8Ω, I^2S input = –120dBFS

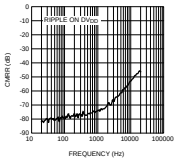


Typical Performance Characteristics (continued)

PSRR vs FREQUENCY
DV_{DD} = 1.8V, V_{RIPPLE} = 200mV_{P-P}, R_L = 8Ω, I^2S input = –120dBFS

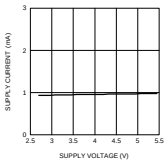


CMRR vs FREQUENCY
V_{RIPPLE} = 200mV_{P-P}, R_L = 8Ω,

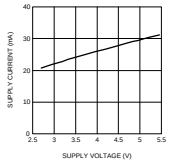


Typical Performance Characteristics (continued)

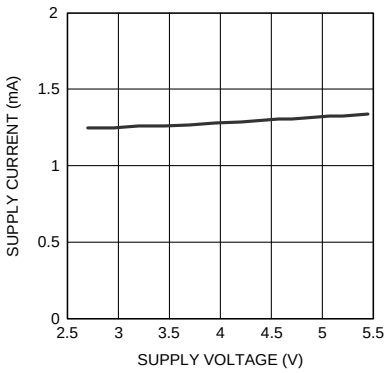
SUPPLY CURRENT vs SUPPLY VOLTAGE ADC Mode



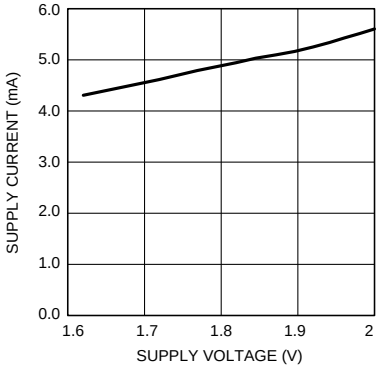
ANALOG SUPPLY CURRENT vs SUPPLY VOLTAGE ADC Mode



PLL SUPPLY CURRENT vs SUPPLY VOLTAGE

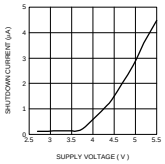


DIGITAL SUPPLY CURRENT vs SUPPLY VOLTAGE

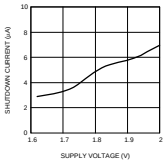


Typical Performance Characteristics (continued)

SHUTDOWN CURRENT vs SUPPLY VOLTAGE



DIGITAL SHUTDOWN CURRENT vs SUPPLY VOLTAGE



Application Information

I²C COMPATIBLE INTERFACE

The LM48903 is controlled through an I²C compatible serial interface that consists of a serial data line (SDA) and a serial clock (SCL). The clock and data lines are bi-directional (open drain). The LM48903 communicates at clock rates up to 400kHz. Figure 4 shows the I²C interface timing diagram. Data on the SDA line must be stable during the HIGH period of SCL. The LM48903 is a transmit/receive device, and can act as the I²C master, generating the SCL signal. Each transmission sequence is framed by a START condition and a STOP condition Figure 5.

Due to the number of data registers, the LM48903 employs a page mode scheme. Each data write consists of 7, 8 bit data bytes, device address (1 byte), 16 bit register address (2 bytes), and 32 bit register data (4 bytes). Each byte is followed by an acknowledge pulse Figure 6. Single byte read and write commands are ignored. The LM48903 device address is 0110000X.

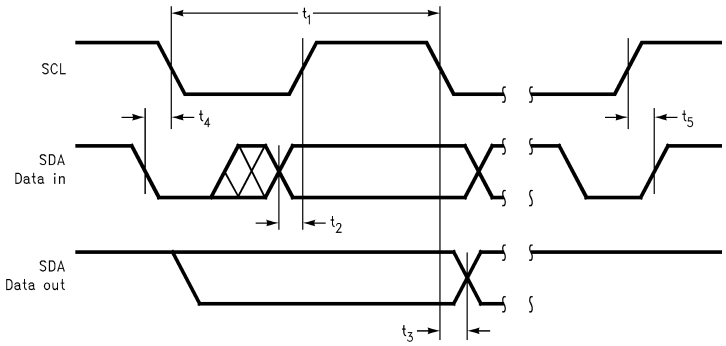


Figure 4. I²C Timing Diagram

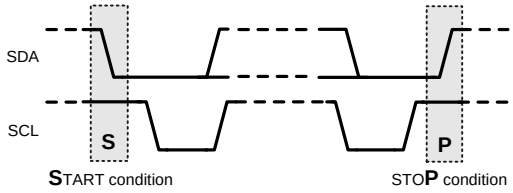


Figure 5. Start and Stop Diagram

WRITE SEQUENCE

The example write sequence is shown in Figure 6. The START signal, the transition of SDA from HIGH to LOW while SDA is HIGH, is generated, altering all devices on the bus that a device address is being written to the bus.

The 7-bit device address is written to the bus, most significant bit (MSB) first, followed by the R/$\overline{W}$ bit (R/$\overline{W}$ = 0 indicating the master is writing to the LM48903). The data is latched in on the rising edge of the clock. Each address bit must be stable while SDA is HIGH. After the R/W\ bit is transmitted, the master device releases SDA, during which time, an acknowledge clock pulse is generated by the slave device. If the LM48903 receives the correct address, the device pulls the SDA line low, generating and acknowledge bit (ACK).

Once the master device registers the ACK bit, the first 8-bit register address word is sent, MSB first [15:8]. Each data bit should be stable while SCL is HIGH. After the first 8-bit register address is sent, the LM48903 sends another ACK bit. Upon receipt of acknowledge, the second 8-bit register address word is sent [7:0], followed by another ACK bit. The register data is sent, 8-bits at a time, MSB first in the following order [7:0], [15:8], [23:16], [31.24]. Each 8-bit word is followed by an ACK, upon receipt of which the successive 8-bit word is sent. Following the acknowledgement of the last register data word [31:24], the master issues a STOP bit, allowing SDA to go high while SDA is high.

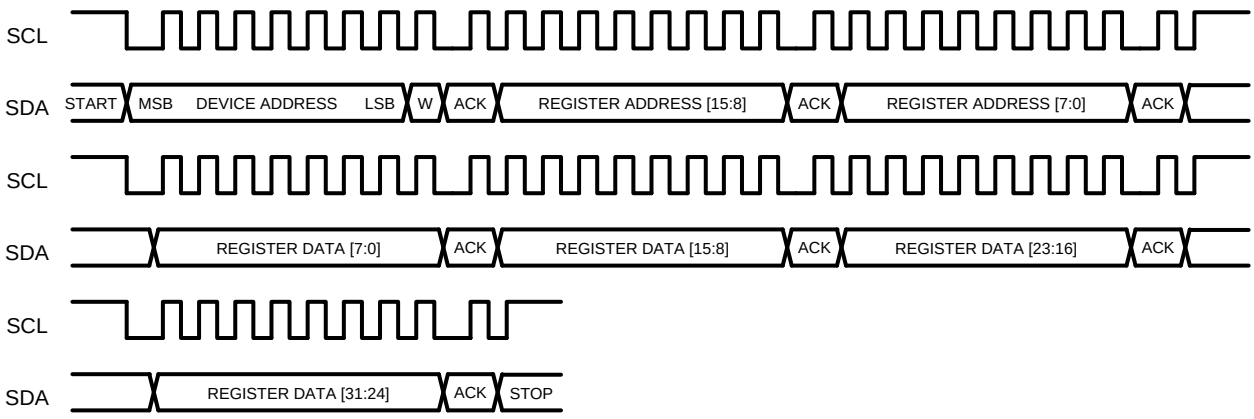


Figure 6. Example I²C Write Sequence

READ SEQUENCE

The example read sequence is shown in Figure 7. The START signal, the transition of SDA from HIGH to LOW while SDA is HIGH, is generated, altering all devices on the bus that a device address is being written to the bus.

The 7-bit device address is written to the bus, followed by the R/$\overline{W}$ = 0. After the R/$\overline{W}$ bit is transmitted, the master device releases SDA, during which time, an acknowledge clock pulse is generated by the slave device. If the LM48903 receives the correct address, the device pulls the SDA line low, generating and acknowledge bit (ACK). Once the master device registers the ACK bit, the first 8-bit register address word is sent, MSB first [15:8], followed by and ACK from the LM48903. Upon receipt of the acknowledge, the second 8-bit register address word is sent [7:0], followed by another ACK bit. Following the acknowledgment of the last register address, the master initiates a REPEATED START, followed by the 7-bit device address, followed by R/$\overline{W}$ = 1 (R/$\overline{W}$ = 1 indicating the master wants to read data from the LM48903). The LM48903 sends an ACK, followed by the selected register data. The register data is sent, 8-bits at a time, MSB first in the following order [7:0], [15:8], [23:16], [31:24]. Each 8-bit word is followed by an ACK, upon receipt of which the successive 8-bit word is sent. Following the acknowledgement of the last register data word [7:0], the master issues a STOP bit, allowing SDA to go high while SDA is high.

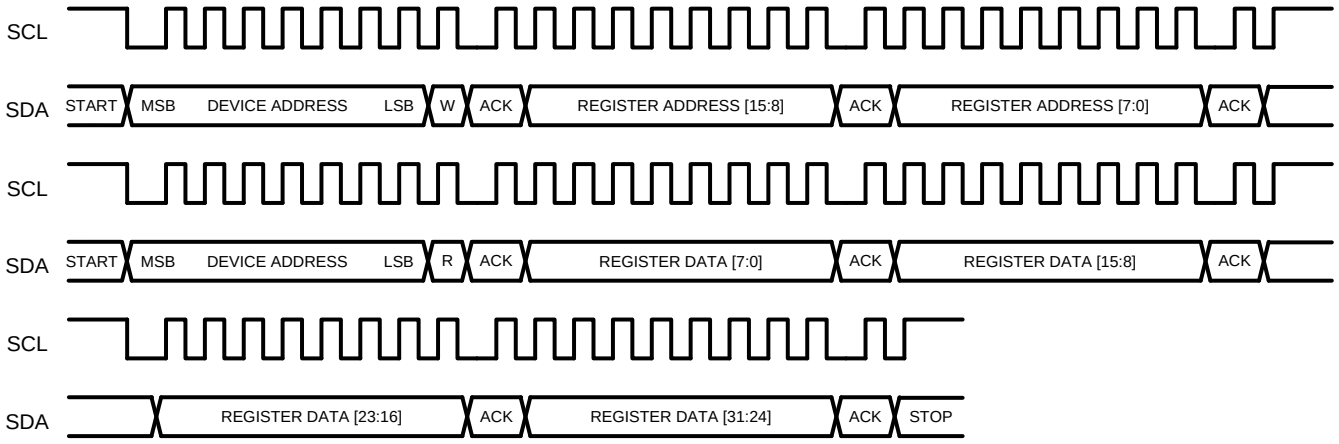


Figure 7. Example I²C Read Sequence

I²S DATA FORMAT

The LM48903 supports three I²S formats: Normal Mode Figure 8, Left Justified Mode Figure 9, and Right Justified Mode Figure 10. In Normal Mode, the audio data is transmitted MSB first, with the unused bits following the LSB. In Left Justified Mode, the audio data format is similar to the Normal Mode, without the delay between the LSB and the change in I²S_WS. In Right Justified Mode, the audio data MSB is transmitted after a delay of a preset number of bits.

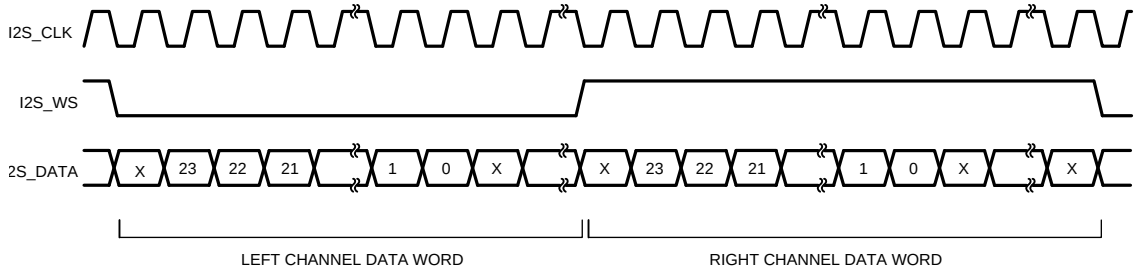


Figure 8. I²S Normal Input Format

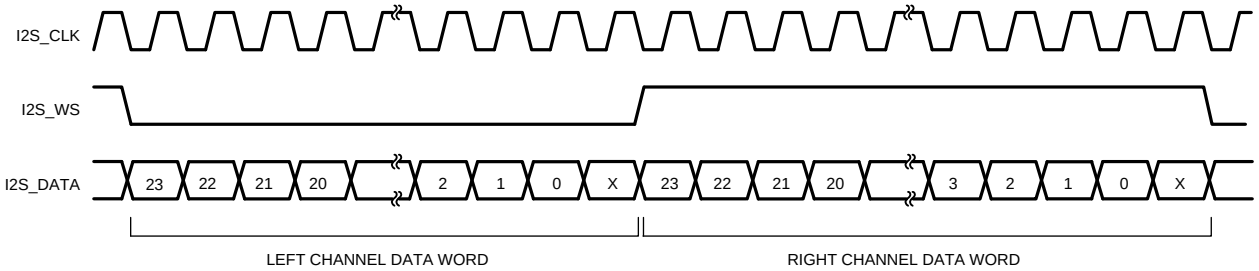


Figure 9. I^2S Left Justified Input Format

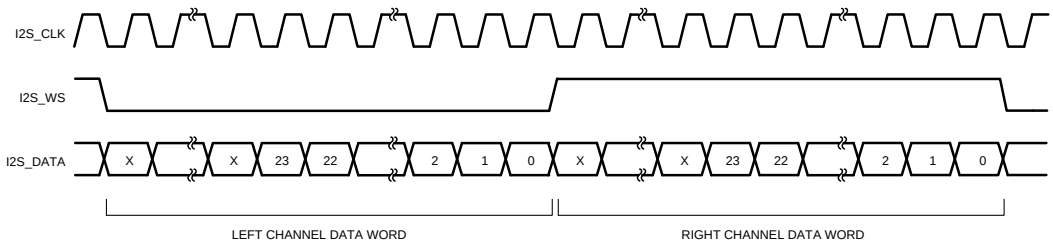


Figure 10. I^2S Right Justified Input Format

MEMORY ORGANIZATION

The LM48903 memory is organized into three main regions: a 32-bit wide Coefficient Space that holds the spatial coefficients, a 32-bit wide Register Space that holds the device configuration settings, and a 48-bit wide Audio Sample Space that holds the current audio data sampled from either the ADCs or the I2S interface, organized as shown in Figure 11.

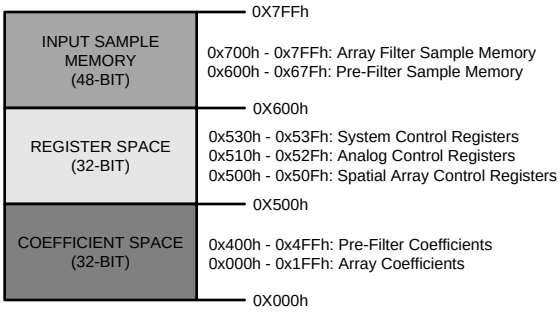


Figure 11. LM48903 Memory Organization

COEFFICIENT MEMORY

The device must be in Debug mode in order to write to the Coefficient memory. Set Bit 7 (DBG_ENABLE) in Filter Debug Register 1 (0x504h) = 1 to enable Debug mode. The Coefficient Memory Space is organized as follows.

Table 3. Coefficient Memory Space

REGISTER ADDRESS	REGISTER CONTENTS	
	(31:16)	(15:0)
0x000h - 0x0FFh	256x16 bit Array Taps	256x16 bit Array Taps
	(Right Input to OUT2)	(Left Input to OUT2)
0x100h - 0x1FFh	256x16 bit Array Taps	256x16 bit Array Taps
	(Right Input to OUT1)	(Left Input to OUT1)
0x400h - 0x47Eh (EVEN)	C2 128x16 bit Prefilter Taps	C0 128x16 bit Prefilter FIR Taps
	(Right to Right)	(Left to Left)
0x441h - 0x47Fh (ODD)	C3 128x16 bit Prefilter Taps	C1 128x16 bit Prefilter FIR Taps
	(Right to Left)	(Left to Right)

CONTROL REGISTERS

Table 4. Register Map

Register Name	Register Address	Default Value	7	6	5	4	3	2	1	0
FILTER CONTROL	0x500h [7:0]	0xFFh	ARRAY_TAP							
	0x500h [15:8]	0x7Fh	UNUSED	PRE_TAP						
	0x500h [23:16]	0xE4h	UNUSED				CH2_SEL		CH1_SEL	
	0x500h [31:24]	0xC1h	ARRAY_ ENABLE	PRE_ ENABLE	ARRAY_ BYPASS	PRE_ BYPASS	UNUSED			

Table 4. Register Map (continued)

Register Name	Register Address	Default Value	7	6	5	4	3	2	1	0
FILTER COMP1	0x501h [7:0]	0x98h	G1_GAIN			COMP_TH				
	0x501h [15:8]	0x11h	UNUSED	POST_GAIN			UNUSED	COMP_RATIO		
	0x501h [23:16]	0x00h	ARRAY_COMP_SELECT							
	0x501h [31:24]	0x00h	UNUSED							
FILTER COMP2	0x502h [7:0]	0XB8h	G1_GAIN			COMP_TH				
	0x502h [15:8]	0x11h	UNUSED	POST_GAIN			UNUSED	COMP_RATIO		
	0x502h [23:16]	0XB8h	G1_GAIN			COMP_TH				
	0x502h [31:24]	0x11h	UNUSED	POST_GAIN			UNUSED	COMP_RATIO		
FILTER DEBUG0	0x503h [7:0]	0x00h	DBG_DATA [7:0]							
	0x503h [15:8]	0x00h	DBG_DATA [15:8]							
	0x503h [23:16]	0x00h	DBG_DATA [23:16]							
	0x503h [31:24]	0x00h	UNUSED							
FILTER DEBUG1	0x504h [7:0]	0x00h	DBG_ ENABLE	STEP_ ENABLE	UNUSED	FILTER_ SELECT	ACC_ADDR			
	0x504h [15:8]	0x00h	UNUSED							
	0x504h [23:16]	0x00h	UNUSED							
	0x504h [31:24]	0x00h	UNUSED							
FILTER STATS	0x505h [7:0]	0x00h	PCOUNT1_MODE				PCH_SEL			
	0x505h [15:8]	0x80h	PCLEAR	UNUSED			PCOUNT2_MODE			
	0x505h [23:16]	0x00h	ACOUNT1_MODE				ACH_SEL			
	0x505h [31:24]	0x80h	ACLEAR	UNUSED			ACOUNT2_MODE			
FILTER DEBUG1	0x506h [7:0]	0x00h	DBG_DATA [7:0]							
	0x506h [15:8]	0x00h	DBG_DATA [15:8]							
	0x506h [23:16]	0x00h	DBG_DATA [23:16]							
	0x506h [31:24]	0x00h	DBG_DATA [31:24]							

Table 4. Register Map (continued)

Register Name	Register Address	Default Value	7	6	5	4	3	2	1	0
ACCUML DEBUG (READ-ONLY)	0x509h [7:0]	0xXXh	DBG_ACCL [7:0]							
	0x509h [15:8]	0xXXh	DBG_ACCL [15:8]							
	0x509h [23:16]	0xXXh	DBG_ACCL [23:16]							
	0x509h [31:24]	0xXXh	DBG_ACCL [31:24]							
ACCUMH DEBUG (READ-ONLY)	0x50Ah [7:0]	0xXXh	DBG_ACC [39:32]							
	0x50Ah [15:8]	0xXXh	DBG_ACC [47:40]							
	0x50Ah [23:16]	0xXXh	UNUSED							
	0x50Ah [31:24]	0xXXh	UNUSED							
DBG SAT (READ-ONLY)	0x50Bh [7:0]	0xXXh	DBG_SAT [7:0]							
	0x50Bh [15:8]	0xXXh	DBG_SAT [15:8]							
	0x50Bh [23:16]	0xXXh	DBG_SAT [23:16]							
	0x50Bh [31:24]	0xXXh	UNUSED							
STAT PCNT1 (READ-ONLY)	0x50Ch [7:0]	0xXXh	COUNT [7:0]							
	0x50Ch [15:8]	0xXXh	COUNT [15:8]							
	0x50Ch [23:16]	0xXXh	COUNT [23:16]							
	0x50Ch [31:24]	0xXXh	COUNT [31:24]							
STAT PCNT2 (READ-ONLY)	0x50Dh [7:0]	0xXXh	COUNT [7:0]							
	0x50Dh [15:8]	0xXXh	COUNT [15:8]							
	0x50Dh [23:16]	0xXXh	COUNT [23:16]							
	0x50Dh [31:24]	0xXXh	COUNT [31:24]							
STAT ACNT1 (READ-ONLY)	0x50Eh [7:0]	0xXXh	COUNT [7:0]							
	0x50Eh [15:8]	0xXXh	COUNT [15:8]							
	0x50Eh [23:16]	0xXXh	COUNT [23:16]							
	0x50Eh [31:24]	0xXXh	COUNT [31:24]							

Table 4. Register Map (continued)

Register Name	Register Address	Default Value	7	6	5	4	3	2	1	0
STAT ACNT2 (READ-ONLY)	0x50Fh [7:0]	0xXXh	COUNT [7:0]							
	0x50Fh [15:8]	0xXXh	COUNT [15:8]							
	0x50Fh [23:16]	0xXXh	COUNT [23:16]							
	0x50Fh [31:24]	0xXXh	COUNT [31:24]							
ADC OFFSET	0x510h [7:0]	0X00h	ADCR_VOS [7:0]							
	0x510h [15:8]	0X00h	ADCR_VOS [15:8]							
	0x510h [23:16]	0X00h	ADCL_VOS [7:0]							
	0x510h [31:24]	0X00h	ADCL_VOS [15:8]							
CLASS D OFFSET	0x511h [7:0]	0X00h	OUT1_VOS [7:0]							
	0x511h [15:8]	0X00h	OUT1_VOS [15:8]							
	0x511h [23:16]	0X00h	OUT2_VOS [7:0]							
	0x511h [31:24]	0X00h	OUT2_VOS [15:8]							
DELAY	0x520h [7:0]	0x06h	POWER_UP_DELAY [7:0]							
	0x520h [15:8]	0x00h	POWER_UP_DELAY [15:8]							
	0x520h [23:16]	0x20h	DEGLITCH_DELAY							
	0x520h [31:24]	0x09h	STATE_DELAY							
ENABLE & CLOCKS	0x521h [7:0]	0x00h	ADC_SYNC_SEL	ADC_DC_CORRECT	ADC_DC_CAL	PWM_DC_CORRECT	VREF_DELAY	PULSE	FORCE	ENABLE
	0x521h [15:8]	0x20h	QSA_MBIST	QSA_CLK_STOP	HIFI	PCM_CLK_SEL	I2S_CLK	MCLK_RATE		
	0x521h [23:16]	0x00h	UNUSED			ADC_HPF_TO_1_4	ADC_HPF_ENABLE	ADC_HPF_MODE		
	0x521h [31:24]	0x00h	UNUSED					OFFSET_READBACK_SELECT		
DIGITAL MIXER	0x522h [7:0]	0x33h	ZERO_CROSS	MUTE	ADC_LVL					
	0x522h [15:8]	0x33h	UNUSED		I2S_LVL					
	0x522h [23:16]	0x02h	UNUSED				I2SA_TX_SEL	ADC_DSP	I2S_DSP	
	0x522h [31:24]	0x05h	UNUSED				OUT2_SEL	OUT1_SEL		

Table 4. Register Map (continued)

Register Name	Register Address	Default Value	7	6	5	4	3	2	1	0
ANALOG	0x523h [7:0]	0x00h	BYPASS_MOD	AUTO_SD	ADCTRIM	ZERO_DIG	ZERO_ANA	PARALLEL	ANA_LVL	
	0x523h [15:8]	0x10h	UNUSED		SCAN_TRIG	SE_MOD	PMC_ TEST	TSD_DIS	SCKT_DIS	TST_SHT
	0x523h [23:16]	0x00h	UNUSED							
	0x523h [31:24]	0x00h	UNUSED							I2C_ANA_LEVEL
I2S PORT	0x524h [7:0]	0x01h	SYNC_ MODE	STEREO_SYNC_ PHASE	CLOCK_ PHASE	SYNC_MS	CLK_MS	TX_ ENABLE	RX_ ENABLE	STEREO
	0x524h [15:8]	0x00h	UNUSED		HALF_CYCLE_DIVIDER					
	0x524h [23:14]	0x00h	UNUSED				SYNTH_ DENOM	SYNTH_NUM		
	0x524h [31:24]	0x00h	UNUSED		MONO_SYNC_WIDTH			SYNC_RATE		
	0x525h [7:0]	0x00h	TX_BIT		TX_WIDTH			RX_WIDTH		
	0x525h [15:8]	0x02h	RX_ A/µLAW	RX_ COMPAND	RX_MSB_POSITION					RX_MODE
	0x525h [23:16]	0x02h	TX_ A/µLAW	TX_ COMPAND	TX_MSB_POSITION					TX_MODE
	0x525h [31:24]	0x00h	UNUSED							
ADC TRIM CO-EFFICIENT	0x526h [7:0]	0x00h	ADC_COMP_COEFF_C0 [7:0]							
	0x526h [15:8]	0x00h	ADC_COMP_COEFF_C0 [15:8]							
	0x526h [23:14]	0x00h	ADC_COMP_COEFF_C1 [7:0]							
	0x526h [31:24]	0x00h	ADC_COMP_COEFF_C1 [15:8]							
	0x527h [7:0]	0x00h	ADC_COMP_COEFF_C2 [7:0]							
	0x527h [15:8]	0x00h	ADC_COMP_COEFF_C2 [15:8]							
	0x527h [23:16]	0x00h	UNUSED							
	0x527h [31:24]	0x00h	UNUSED							
READ BACK0 (READ-ONLY)	0x528h [7:0]	0x00h	UNUSED		I2SL_LVL CLIP	I2SR_LVL CLIP	ADCL_LVL CLIP	ADCR_LVL CLIP	ADCL_ CLIP	ADCR_ CLIP
	0x528h [15:8]	0x00h	UNUSED			THERMAL			SHORT2	SHORT1
	0x528h [23:14]	0x00h	SPARE							
	0x528h [31:24]	0x00h	UNUSED							

Table 4. Register Map (continued)

Register Name	Register Address	Default Value	7	6	5	4	3	2	1	0
READ BACK1 (READ-ONLY)	0x529h [7:0]	0x00h	OFF_RD_BACK [3:0]				CE_STATE			
	0x529h [15:8]	0x00h	OFF_RD_BACK [11:4]							
	0x529h [23:14]	0x00h	OFF_RD_BACK [19:12]							
	0x529h [31:24]	0x00h	SPARE_RD_BACK							
SYS CONFIG	0x530h [7:0]	0x30h	I2C_MCLK _REQ	DEVICE_ID						
	0x530h [15:8]	0x00h	UNUSED				I2C_SP_MOD		USE_22C _ROM_SE L	USE_RAM
	0x530h [23:16]	0x8Ch	W_CLE _EN	UNUSED						
	0x530h [31:24]	0x00h	UNUSED						MBIST1_ ENABLE	MBIST0_ ENABLE
SPEAKER OVER DRIVE CONTROL	0x531h [7:0]	0x65h	W2				W1			
	0x531h [15:8]	0x43h	UNUSED	RL_RES			UNUSED	AT_RES		
	0x531h [23:16]	0x83h	MAX_GAIN				AT_GAIN			
	0x531h [31:24]	0x27h	SODP_EN ABLE	FS	SINP_MODE		UNUSED	INT_GAIN		
SODP THRES HOLD	0x532h [7:0]	0x70h	LEVEL1							
	0x532h [15:8]	0x20h	LEVEL2							
	0x532h [23:16]	0x64h	INT_TH1							
	0x532h [31:24]	0x64h	INT_TH2							
LOW POWER CONTROL	0x533h [7:0]	0x00h	UNUSED		LOW_PWR_MODE		UNUSED	AUDET_LEVEL		AUDET _ENABLE
	0x533h [15:8]	0x09h	ADC_TH [3:0]				TIMEOUT_DELAY			
	0x533h [23:16]	0x00h	ADC_TH [11:4]							
	0x533h [31:24]	0x00h	OVR_ADC L_ENABL E	OVR_ADC R_ENABL E	OVR_PLL _ENABLE	OVR_VRE F_ENABL E	OVR_OUT1 _ENABLE	OVR_OUT 2_ENABL E	OVR_OUT 1_RST	OVR_OUT 2_RST
SYSTEM STATUS	0x538h [7:0]	0x00h	2b0		MBIST_ENABLE		MBIST_GO		MBIST_DONE	
	0x538h [15:8]	0x00h	UNUSED					CL_ACTIV E	BUS_ERR OR	DEV_EXIS TS
	0x538h [23:16]	0x00h	MEM_ADDR [7:0]							
	0x538h [31:24]	0x00h	MEM_ADDR [15:8]							

Table 4. Register Map (continued)

Register Name	Register Address	Default Value	7	6	5	4	3	2	1	0
DEVICE ID	0x539h [7:0]	0XA0h	CHIP_ID [7:0]							
	0x539h [15:8]	0x3Ah	CHIP_ID [15:8]							
	0x539h [23:16]	0x90h	CHIP_ID [23:16]							
	0x539h [31:24]	0x48h	CHIP_ID [31:24]							
SPEAKER OVER DRIVE DEBUG	0x53Ah [7:0]		SODP_INT [7:0]							
	0x53Ah [15:8]		SODP_INT [15:8]							
	0x53Ah [23:16]		SODP_INT[23:16]							
	0x53Ah [31:24]		GAIN_INT_MAG							

FILTER CONTROL REGISTER (0x500h)

Configures the LM48903 Array and Pre-Array filters (Spatial Engine). The Filter Control Register sets the length of the Array and Pre-Array filter taps, and selects the filter channel source for each audio output. Set PRE_BYPASS and ARRAY_BYPASS to 1 to bypass the Spatial Engine, disabling the spatial effect without modifying the coefficients. Set PRE_ENABLE and ARRAY_ENABLE to 1 to enable the Spatial Engine. Set PRE_ENABLE and ARRAY_ENABLE to 0 to disable the spatial engine. Disabling the Spatial Engine does not affect the register contents. Disable the Spatial Engine during coefficient programming.

Table 5. Filter Control Register

BIT	NAME	VALUE	DESCRIPTION
7:0	ARRAY_TAP		Array Filter Tap Length
14:8	PRE_TAP		Pre-filter Tap Length. Pre-filter tap length should be less than or equal to the Array filter tap length
15	UNUSED		
17:16	CH1_SEL		Channel 1 Output Routing Selection
		0	Array Filter Channel 0 Output Select
		1	Array Filter Channel 1 Output Select
19:18	CH2_SEL		Channel 2 Output Routing Selection
		0	Array Filter Channel 0 Output Select
		1	Array Filter Channel 1 Output Select
27:20	UNUSED		
28	PRE_BYPASS	0	Pre-Array filter not bypassed
		1	Pre-Array filter bypassed
29	ARRAY_BYPASS	0	Array filter not bypassed
		1	Array filter bypassed
30	PRE_ENABLE	0	Pre-Array filter disabled. Disable the Pre-Array Filter during filter and coefficient programming. Disabling the Pre-Array Filter does not affect the device memory contents.
		1	Pre-Array filter enabled
31	ARRAY_ENABLE	0	Array filter disabled. Disable the Array Filter during filter and coefficient programming. Disabling the Array Filter does not affect the device memory contents.
		1	Array filter enabled

COMPRESSOR CONTROL REGISTER 1 (FILTER COMP1) (0x501h)

Table 6. Compressor Control Register

BIT	NAME	VALUE	DESCRIPTION
4:0	COMP_TH		Pre-Filter Compressor Threshold
7:5	G1_GAIN		Pre-Compression Gain
		000	2
		001	4
		010	8
		011	16
		100	32
		101	64
		110	128
		111	256
10:8	COMP_RATIO		Compression Ratio
		000	1:1
		001	2:1
		010	2.66:1
		011	4:1
		100	5.33:1
		101	8:1
		110	10.66:1
		111	16:1
11	UNUSED		
14:12	POST_GAIN		Post Compression Gain (V/V)
		000	1
		001	1.25
		010	1.5
		011	2
		100	2.5
		101	3
		110	4
		111	8
15	UNUSED		
23:16	ARRAY_COMP_SELECT		Array Filter Compression Control Register Select
31:24	UNUSED		

COMPRESSOR CONTROL REGISTER 2 (FILTER COMP2) (0x502h)

Table 7. Compressor Control Register 2

BIT	NAME	VALUE	DESCRIPTION
4:0	COMP_TH		Pre-Filter Compressor Threshold

Table 7. Compressor Control Register 2 (continued)

BIT	NAME	VALUE	DESCRIPTION
7:5	G1_GAIN		Pre-Compression Gain
		000	2
		001	4
		010	8
		011	16
		100	32
		101	64
		110	128
		111	256
10:8	COMP_RATIO		Compression Ratio
		000	1:1
		001	2:1
		010	2.66:1
		011	4:1
		100	5.33:1
		101	8:1
		110	10.66:1
		111	16:1
11	UNUSED		
14:12	POST_GAIN		Post Compression Gain (V/V)
		0	1
		1	1.25
		10	1.5
		11	2
		100	2.5
		101	3
		110	4
		111	8
15	UNUSED		
20:16	COMP_TH		Pre-Filter Compressor Threshold
23:21	G1_GAIN		Pre-Compression Gain
		0	2
		1	4
		10	8
		11	16
		100	32
		101	64
		110	128
		111	256

Table 7. Compressor Control Register 2 (continued)

BIT	NAME	VALUE	DESCRIPTION
24:26	COMP_RATIO		Compression Ratio
		000	1:001
		001	2:001
		010	2.66:1
		011	4:001
		100	5.33:1
		101	8:001
		110	10.66:1
		111	16:1
27	UNUSED		
30:28	POST_GAIN		Post Compression Gain (V/V)
		000	1
		001	1.25
		010	1.5
		011	2
		100	2.5
		101	3
		110	4
		111	8
31	UNUSED		

FILTER DEBUG REGISTER 0 (FILT_DBG0) (0x503h)

Table 8. Filter Debug Register 0

BIT	NAME	VALUE	DESCRIPTION
23:0	DBG_DATA		Audio Data. Common data for both left and right audio channels
31:24	UNUSED		

FILTER DEBUG REGISTER 1 (FILT_DBG1) (0x504h)

Table 9. Filter Debug Register 1

BIT	NAME	VALUE	DESCRIPTION
3:0	ACC_ADDR		Accumulator Address. Selects which accumulator is read during debug mode
4	FILTER_SELECT	0	Selects Pre-Filter Accumulators
		1	Selects Array Filter Accumulators
5	UNUSED		
6	STEP_ENABLE	0	Single Step Disabled
		1	Single Step Enabled
7	DBG_ENABLE	0	Debug Mode Disabled
		1	Debug Mode Enabled
31:8	UNUSED		

FILTER STATISTICS CONTROL REGISTER (FILT_STC) (0x505h)

Table 10. Filter Statistics Control Register

BIT	NAME	VALUE	DESCRIPTION
PRE-FILTER Counter			
3:0	PCH_SEL		Channel Select
		000	Channel 0
		001	Channel 1
		010	Channel 2
		011	Channel 3
		100	Channel 4
		101	Channel 5
		110	Channel 6
		111	Channel 7
7:4	PCOUNT1_MODE		Counter 1 Mode Select. Specifies input of Counter 1
		0000	Sample Count Mode. Every audio sample is counted
		0001	Overflow. Overflow events counted
		0010	Frequency Error. Indicates input frequency not sufficient for given filter length
		1000	MAGN[7}
		1001	MAGN[7:6]
		1010	MAGN[7:5}
		1011	MAGN[7:4}
		1100	MAGN[7:3}
		1101	MAGN[7:2]
		1110	MAGN[7:1}
		1111	MAGN[7:0]
11:8	PCOUNT2_MODE		Counter 2 Mode Select. Specifies input of Counter 2
		0000	Sample Count Mode. Every audio sample is counted
		0001	Overflow. Overflow events counted
		0010	Frequency Error. Indicates input frequency not sufficient for given filter length
		1000	MAGN[7}
		1001	MAGN[7:6]
		1010	MAGN[7:5}
		1011	MAGN[7:4}
		1100	MAGN[7:3}
		1101	MAGN[7:2]
		1110	MAGN[7:1}
		1111	MAGN[7:0]
14:12	UNUSED		
15	PCLEAR	0	Counter Enabled
		1	Counter Cleared
ARRAY-FILTER Counter			

Table 10. Filter Statistics Control Register (continued)

BIT	NAME	VALUE	DESCRIPTION
19:16	ACH_SEL		Channel Select
		000	Channel 0
		001	Channel 1
		010	Channel 2
		011	Channel 3
		100	Channel 4
		101	Channel 5
		110	Channel 6
		111	Channel 7
23:20	ACOUNT1_MODE		Counter 1 Mode Select. Specifies input of Counter 1
		0000	Sample Count Mode. Every audio sample is counted
		0001	Overflow. Overflow events counted
		0010	Frequency Error. Indicates input frequency not sufficient for given filter length
		1000	MAGN[7}
		1001	MAGN[7:6]
		1010	MAGN[7:5}
		1011	MAGN[7:4}
		1100	MAGN[7:3}
		1101	MAGN[7:2]
		1110	MAGN[7:1}
		1111	MAGN[7:0]
27:24	ACOUNT2_MODE		Counter 2 Mode Select. Specifies input of Counter 2
		0000	Sample Count Mode. Every audio sample is counted
		0001	Overflow. Overflow events counted
		0010	Frequency Error. Indicates input frequency not sufficient for given filter length
		1000	MAGN[7}
		1001	MAGN[7:6]
		1010	MAGN[7:5}
		1011	MAGN[7:4}
		1100	MAGN[7:3}
		1101	MAGN[7:2]
		1110	MAGN[7:1}
		1111	MAGN[7:0]
30:28	UNUSED		
31	ACLEAR	0	Counter Enabled
		1	Counter Cleared

FILTER DEBUG REGISTER 2 (FILTER DEBUG 2) (0x506h)

Table 11. Filter Debug Register 2

BIT	NAME	VALUE	DESCRIPTION
31:0	DGB_DATA		Debug Data. Read Only

ACCUMULATOR DEBUG LOWER REGISTER (ACCUML DEBUG) (0x509h)

Table 12. Accumulator Debug Lower Register

BIT	NAME	VALUE	DESCRIPTION
31:0	DBG_ACCL		Accumulator Debug Data. Read Only

ACCUMULATOR DEBUG UPPER REGISTER (ACCUML DEBUG) (0x50Ah)

Table 13. Accumulator Debug Upper Register

BIT	NAME	VALUE	DESCRIPTION
31:0	DBG_ACCL		Accumulator Debug Data. Read Only

COMPRESSOR OUTPUT DATA REGISTER (DBG_SAT) (0x50Bh)

Table 14. Compressor Output Data Register

BIT	NAME	VALUE	DESCRIPTION
23:0	DBG_SAT		24-Bit Compressor Output Data. Read Only
31:24	UNUSED		

FILTER STATISTICS COUNTER (STAT_ACNT) (0x50Ch)

Table 15. Filter Statistics Counter Register

BIT	NAME	VALUE	DESCRIPTION
31:0	COUNT		Statistics of Post-Processed Array and Pre-Filter Data. Read Only

FILTER STATISTICS COUNTER (STAT_ACNT) (0x50Dh)

Table 16. Filter Statistics Counter Register

BIT	NAME	VALUE	DESCRIPTION
31:0	COUNT		Statistics of Post-Processed Array and Pre-Filter Data. Read Only

FILTER STATISTICS COUNTER (STAT_ACNT) (0x50Eh)

Table 17. Filter Statistics Counter Register

BIT	NAME	VALUE	DESCRIPTION
31:0	COUNT		Statistics of Post-Processed Array and Pre-Filter Data. Read Only

FILTER STATISTICS COUNTER (STAT_ACNT) (0x50Fh)

Table 18. Filter Statistics Counter Register

BIT	NAME	VALUE	DESCRIPTION
31:0	COUNT		Statistics of Post-Processed Array and Pre-Filter Data. Read Only

ADC DC OFFSET REGISTER (ADC OFFSET) (0x510h)

Table 19. ADC DC Offset Register

BIT	NAME	VALUE	DESCRIPTION
15:0	ADCR_VOS		ADC Right Channel Output DC Offset
31:16	ADCL_VOS		ADC Left Channel Output DC Offset

CLASS D DC OFFSET REGISTER (CLASS D OFFSET) (0x511h)

Table 20. Class D DC Offset Register

BIT	NAME	VALUE	DESCRIPTION
15:0	OUT1_VOS		OUT1 Output DC Offset
31:16	OUT2_VOS		OUT2 Output DC Offset

DELAY REGISTER (DELAY) (0x520h)

Table 21. Delay Register

BIT	NAME	VALUE	DESCRIPTION
15:0	POWER_UP_DELAY		Sets I^2C Delay Time. Default 10ms delay.
23:16	DEGLITCH_DELAY		Sets ENABLE Bit Polling Timeout. Default 32ms delay
31:24	STATE_DELAY		Sets Delay Between Power Up/Down States

ENABLE AND CLOCK CONFIGURATION REGISTER (ENABLE & CLOCKS) (0x521h)

Table 22. Enable and Clock Configuration Register

BIT	NAME	VALUE	DESCRIPTION
0	ENABLE	0	Device Disabled in Manual Mode
		1	Device Enabled in Manual Mode
1	FORCE	0	Device Enabled Via $\overline{\text{SHDN}}$ Pin
		1	Device Enabled Via I^2C
2	PULSE	0	$\overline{\text{SHDN}}$ Requires a Stable Logic Level
		1	$\overline{\text{SHDN}}$ Accepts a Pulse Input
3	RELY_ON_VREF	0	Device waits for delay time determined by STATE_DELAY to enable.
		1	Device waits for stable VREF
4	PWM_DC_CORRECT	0	Disable Class D Offset Correction
		1	Enable Class D Offset Correction
5	ADC_DC_CAL	0	Disable ADC Offset Calibration
		1	Enable ADC Offset Calibration
6	ADC_DC_CORRECT	0	Disable ADC Offset Correction
		1	Enable ADC Offset Correction
7	ADC_SYNC_SEL	0	Normal Operation
		1	Invert SYNC Signal. Increases timing margin at low supplies

Table 22. Enable and Clock Configuration Register (continued)

BIT	NAME	VALUE	DESCRIPTION
10:8	MCLK_RATE		Selects PLL Input Divider
		000	32fs (1.536MHz)
		001	64fs (3.072MHz)
		010	128fs (6.114MHz)
		011	256fs (12.288MHz)
		100	512fs (24.576MHz)
		101	UNUSED
		110	UNUSED
		111	UNUSED
11	I2S_CLK	0	MCLK Input to PLL
		1	I^2S_CLK Input to PLL
12	PMC_CLK_SEL	0	Oscillator Clock Input to Power Management Circuitry
		1	MCLK or I^2S_CLK Input to Power Management Circuitry. Clock source depends on the state of I^2S_CLK
13	HIFI	0	HiFi Mode Disabled
		1	HiFi Mode Enabled. PLL always produces a 4096fs clock.
14	SAP_CLK_STOP	0	SAP Clock Enabled
		1	SAP Clock Disabled Following Device Configuration
15	SAP_MBIST	0	Disable MBIST
		1	Enable MBIST
18:16	ADC_HPF_MODE		ADC High Pass Filter Mode
		000	
		001	
		010	
		011	
		100	
		101	
		110	
		111	
19	ADC_HPF_ENABLE	0	ADC High Pass Filter Disabled
		1	ADC High Pass Filter Enabled
31:20	UNUSED		

DIGITAL MIXER CONTROL REGISTER (DIGITAL MIXER) (0x522h)

Table 23. Digital Mixer Control Register

BIT	NAME	VALUE	DESCRIPTION
5:0	ADC_LVL		Sets the Gain of the ADC Path (dB)
		000000	-76.5
		000001	-75
		-	1.5dB steps
		110010	-1.5
		110011	0
		110100	1.5
		-	1.5dB Steps
		111111	18
6	MUTE	0	Normal Operation
		1	Mute

Table 23. Digital Mixer Control Register (continued)

BIT	NAME	VALUE	DESCRIPTION
7	ZXD_DISABLE	0	Zero Crossing Detection Enabled
		1	Zero Crossing Detection Disabled
13:8	I2S_LVL		Sets the Gain of the I^2S Path (dB)
		000000	-76.5
		000001	-75
		-	1.5dB steps
		110010	-1.5
		110011	0
		110100	1.5
		-	1.5dB Steps
		111111	18
15:14	UNUSED		
16	I2S_DSP	0	I^2S Data Not Passed to DSP
		1	I^2S Data Passed to DSP
17	ADC_DSP	0	ADC Output Not Passed to DSP
		1	ADC Output Passed to DSP
19:18	ISA_TX_SEL		Selects Input of Primary I^2S Transmitter
		00	None
		01	ADC
		10	DSP
		11	UNUSED
23:20	UNUSED		
25:24	OUT1_SEL		Selects OUT1 Amplifier Input Source
		00	OUT1 Disabled
		01	DSP
		10	I^2S
		11	ADC
27:26	OUT2_SEL		Selects OUT2 Amplifier Input Source
		00	OUT2 Disabled
		01	DSP
		10	I^2S
		11	ADC
31:28	UNUSED		

ANALOG CONFIGURATION REGISTER (ANALOG) (0x523h)

Table 24. Analog Configuration Register

BIT	NAME	VALUE	DESCRIPTION
1:00	ANA_LVL		Sets ADC Preamplifier Gain (dB)
		00	0
		11	2.4
		10	3.5
		11	6
2	PARALLEL	0	Normal Operation. OUT1 and OUT2 operate as separate amplifiers.
		1	Parallel Operation. OUT1 and OUT2 operate in parallel as a single amplifier.

Table 24. Analog Configuration Register (continued)

BIT	NAME	VALUE	DESCRIPTION
3	ZERO_ANA	0	Normal Operation
		1	Auto-Shutdown Mode. Automatically disables the amplifiers when no analog input is detected.
4	ZERO_DIG	0	Normal Operation
		1	Auto-Shutdown Mode. Automatically disables the amplifiers when there is no I^2S input.
5	ADCTRIM	0	ADC Trim Disabled
		1	ADC Trim Enabled. Use ADC_COMP_COEFF_C0-C2 to trim ADC.
6	AUTO_SD	0	Normal Operation
		1	Fault Conditions Disable the Amplifiers
7	BYPASS_MOD	0	Normal Operation
		1	Pulse Correction Bypass. Amplifier output stages act as a buffer, passing PWM signal without correction to output.
8	TST_SHT	0	Normal Operation
		1	Short Amplifier Inputs. Sets amplifier outputs to 50% duty cycle, minimizing click and pop during power up/down.
9	SCKT_DIS	0	Normal Operation
		1	Output Short Circuit Protection Disabled
10	TSD_DIS	0	Normal Operation
		1	Thermal Shutdown Disabled
11	PMC_TEST	0	Normal Operation
		1	PMC uses PLL Source Clock
12	SE_MOD	0	Normal Operation
		1	Single Edge Modulation Mode
23:13	UNUSED		
24	I2C_ANA_LVL	0	External ADC Gain Control. ADC gain set by G0 and G1
		1	Internal ADC Gain Control. ADC gain set by ANA_LVL.
31:25	UNUSED		

I^2S PORT CONFIGURATION REGISTER (I^2S PORT) (0x524h/0x525h)

Table 25. I^2S Port Configuration Register

BIT	NAME	VALUE	DESCRIPTION
0x524h			
0	STEREO	0	Mono Mode
		1	Stereo Mode
1	RX_ENABLE	0	Receive Mode Disabled
		1	Receive Mode Enabled
2	TX_ENABLE	0	Transmit Mode Disabled
		1	Transmit Mode Enabled
3	CLK_MS	0	I^2S Clock Slave. Device requires an external SCLK for proper operation.
		1	I^2S Clock Master. Device generates SCLK and transmits when either RX or TX mode are enabled.
4	SYNC_MS	0	I^2S WS Slave. Device requires an external WS for proper operation.
		1	I^2S WS Master. Device generates WS and transmits when either RX or TX mode are enabled.

Table 25. I²S Port Configuration Register (continued)

BIT	NAME	VALUE	DESCRIPTION
5	CLOCK_PHASE	0	I²S Clock Phase. Transmit on falling edge, receive on rising edge.
		1	PCM Clock Phase. Transmit on rising edge, receive on falling edge.
6	STEREO_SYNC _PHASE	0	I²S Data Format: Left, Right
		1	I²S Data Format: Right, Left
7	SYNC_MODE	Mono	Rising edge indicates start of data word.
		0	SYNC low = Left, SYNC high = Right
		1	SYNC low = Right, SYNC high = left
13:8	HALF_CYCLE _DIVIDER		Configures the I²S port master clock half-cycle divider. Program the half-cycle divider by: (ReqDiv*2) 1
		000000	BYPASS
		000001	1
		000010	1.5
		000011	2
		-	-
		111101	31
		111110	31.5
		111111	32
15:14	UNUSED		
18:16	SYNTH_NUM		Sets the Clock Generator Numerator
		000	SYNTH_DENOM (1/)
		001	100/SYNTH_DENOM
		010	96/SYNTH_DENOM
		011	80/SYNTH_DENOM
		100	72/SYNTH_DENOM
		101	64/SYNTH_DENOM
		110	48/SYNTH_DENOM
		111	0/SYNTH_DENOM
19	SYNTH_DENOM	0	Clock Generator Denominator = 128
		1	Clock Generator Denominator = 125
23:20	UNUSED		

Table 25. I²S Port Configuration Register (continued)

BIT	NAME	VALUE	DESCRIPTION
26:24	SYNC_RATE		Sets number of clock cycles before SYNC pattern repeats.
			MONO MODE
		000	8
		001	12
		010	16
		011	18
		100	20
		101	24
		110	25
		111	32
			STEREO MODE
		000	16
		001	24
		010	32
		011	36
		100	40
		101	48
		110	50
		111	64
29:27	MONO_SYNC_WIDTH		Sets SYNC symbol width in Mono Mode
		000	1
		001	2
		010	4
		011	7
		100	8
		101	11
		110	15
		111	16
31:30	UNUSED		
0x525h			
2:0	RX_WIDTH		Sets number of valid RECEIVE bits.
		000	24
		001	20
		010	18
		011	16
		100	14
		101	13
		110	12
		111	8

Table 25. I²S Port Configuration Register (continued)

BIT	NAME	VALUE	DESCRIPTION
5:3	TX_WIDTH		Sets number of TRANSMIT bits.
		000	24
		001	20
		010	18
		011	16
		100	14
		101	13
		110	12
		111	8
7:6	TX_BIT		Sets number of pad bits after the valid Transmit bits.
		00	0
		01	1
		10	High-Z
		11	High-Z
8	RX_MODE	0	MSB Justified Receive Mode
		1	LSB Justified Receive Mode

Table 25. I²S Port Configuration Register (continued)

BIT	NAME	VALUE	DESCRIPTION
13:9	RX_MSB_POSITION		MSB location from the frame start (MSB Justified) or LSB location from the frame end (LSB Justified)
		00000	0 (DSP/PCM LONG)
		00001	1 (I^2S/PCM SHORT)
		00010	2
		00011	3
		00100	4
		00101	5
		00110	6
		00111	7
		01000	8
		01001	9
		01010	10
		01011	11
		01100	12
		01101	13
		01110	14
		01111	15
		10000	16
		10001	17
		10010	18
		10011	19
		10100	20
		10101	21
		10110	22
		10111	23
		11000	24
		11001	25
		11010	26
		11011	27
		11100	28
		11101	29
		11110	30
		11111	31
14	RX_COMPAND	0	Normal Operation
		1	Audio Data Companded
15	RX_A/µLAW	0	µLaw Compand Mode
		1	A-Law Compand Mode
16	TX_MODE	0	MSB Justified Transmit Mode
		1	LSB Justified Transmit Mode

Table 25. I²S Port Configuration Register (continued)

BIT	NAME	VALUE	DESCRIPTION
21:17	TX_MSB_POSITION		MSB location from the frame start (MSB Justified) or LSB location from the frame end (LSB Justified)
		00000	0 (DSP/PCM LONG)
		00001	1 (I²S/PCM SHORT)
		00010	2
		00011	3
		00100	4
		00101	5
		00110	6
		00111	7
		01000	8
		01001	9
		01010	10
		01011	11
		01100	12
		01101	13
		01110	14
		01111	15
		10000	16
		10001	17
		10010	18
		10011	19
		10100	20
		10101	21
		10110	22
		10111	23
		11000	24
		11001	25
		11010	26
		11011	27
		11100	28
		11101	29
		11110	30
		11111	31
22	TX_COMPAND	0	Normal Operation
		1	Audio Data Companded
23	TX_A/µLAW	0	µLaw Compand Mode
		1	A-Law Compand Mode
31:24	UNUSED		

ADC TRIM COEFFICIENT REGISTER (ADC_TRIM) (0x526h/0x527)

Table 26. ADC Trim Coefficient Register

BIT	NAME	VALUE	DESCRIPTION
0x526h			
15:0	ADC_COMP_COEFF_C0		Sets ADC Trim Coefficient C0
31:16	ADC_COMP_COEFF_C1		Sets ADC Trim Coefficient C1
0x527h			

Table 26. ADC Trim Coefficient Register (continued)

BIT	NAME	VALUE	DESCRIPTION
15:0	ADC_COMP_COEFF_C2		Sets ADC Trim Coefficient C2
31:16	UNUSED		

READBACK REGISTER 0(READBACK0) (0x528h) READ-ONLY

Table 27. Readback Register 0

BIT	NAME	VALUE	DESCRIPTION
0	ADCR_CLIP	1	Right Channel ADC Input Clipped
1	ADCL_CLIP	1	Left Channel ADC Input Clipped
2	ADCR_LVLCLIP	1	Right Channel ADC Output Clipped
3	ADCL_LVLCLIP	1	Left Channel ADC Output Clipped
4	I2SR_LVLCLIP	1	Right Channel I^2S Output Clipped
5	I2SL_LVLCLIP	1	Left Channel I^2S Output Clipped
7:6	UNUSED		
8	SHORT1	1	OUT1 Output Short Circuit
9	SHORT2	1	OUT2 Output Short Circuit
11:10	UNUSED		
12	THERMAL	1	Thermal Shutdown Threshold Exceeded
23:13	SPARE		
31:24	UNUSED		

READBACK REGISTER 1(READBACK1) (0x528h) READ-ONLY

Table 28. Readback Register 1

BIT	NAME	VALUE	DESCRIPTION
3.0	CE_STATE	0000	Wait for supply
		0001	Wait For I^2C CLK REQ
		0010	Enable I^2C CLOCK
		0011	Power up delay
		0100	Standby
		0101	Enable REF
		0110	Enable Inputs
		0111	Enable Outputs
		1000	Unmute
		1001	Enabled
		1010	Off Deglitch
		1011	Mute
		1100	Disable Outputs
		1101	Disable Inputs
		1111	UNUSED
31:4	UNUSED		

SYSTEM CONFIGURATION REGISTER (SYS_CONFIG) (0x530h)

Table 29. System Configuration Register

BIT	NAME	VALUE	DESCRIPTION
6:0	DEVICE_ID		Sets LM48903 Device ID in slave mode. Default is 0x30h.

Table 29. System Configuration Register (continued)

BIT	NAME	VALUE	DESCRIPTION
7	I2C_MCLK_REQ	0	I^2C does not require MCLK
		1	I^2C requires MCLK
8	USE_RAM	0	Disable RAM Memory Usage
		1	Enable RAM Memory Usage
9	USE_I2C_ROM_SEL	0	MODE0, MODE1, Selects SPATIAL mode
		1	I^2C_SP_MD, Selects Spatial mode
11:10	I2C_SP_MD		ROM mode spatial effects select. Selects which ROM page is loaded into coefficient memory.
		00	4.5cm speaker spacing
		01	6cm speaker spacing
		10	11.5cm speaker spacing
		11	DSP bypassed, stereo mode
22	UNUSED		
23	W_CLE_EN	0	Write clock disabled
		1	Write clock enabled
24	MBIST0_ENABLE	0	Memory BIST Controller 0 Disabled
		1	Memory BIST Controller 0 Enabled.
25	MBIST1_ENABLE	0	Memory BIST Controller 1 Disabled
		1	Memory BIST Controller 1 Enabled.
31:26	UNUSED		

SPEAKER OVERDRIVE CONTROL REGISTER (SPEAKER OVERDRIVE) (0x531h)

Table 30. Speaker Overdrive Protection Register

BIT	NAME	VALUE	DESCRIPTION
3:0	W1		Window 1. Sets the sample window time the device uses to estimate audio energy for samples between LEVEL1 and LEVEL2 (0x532h)
		0000	5ms
		0001	10ms
		0010	20ms
		0011	50ms
		0100	100ms
		0101	200ms
		0110	500ms
		0111	800ms
		1000	1s
		1001	2s
		1010	5s
		1011	10s
		1100-1111	UNUSED

Table 30. Speaker Overdrive Protection Register (continued)

BIT	NAME	VALUE	DESCRIPTION
7:4	W2		Window 2. Sets the sample window time the device uses to estimate audio energy for samples above INT_TH1 (0x532h)
		0000	5ms
		0001	10ms
		0010	20ms
		0011	50ms
		0100	100ms
		0101	200ms
		0110	500ms
		0111	800ms
		1000	1s
		1001	2s
		1010	5s
		1011	10s
		1100-1111	UNUSED
10:8	AT_RES		Attack Time Resolution
		000	1ms
		001	2ms
		010	5ms
		011	10ms
		100	20ms
		101	50ms
		110	100ms
		111	200ms
11	UNUSED		
14:12	RL_RES		Release Time Resolution
		000	1ms
		001	2ms
		010	5ms
		011	10ms
		100	20ms
		101	50ms
		110	100ms
		111	200ms
15	UNUSED		
19:16	AT_GAIN		Attack Mode Gain Reduction
		000	0dB. No gain reduction
		001	3dB
		—	3dB steps
		110	18dB
		111	21dB
23:17	MAX_GAIN		Maximum Gain
		000	0dB
		001	3dB
		—	3dB steps
		110	18dB
		111	21dB

Table 30. Speaker Overdrive Protection Register (continued)

BIT	NAME	VALUE	DESCRIPTION
26:24	INT_GAIN		Integrator Gain
		000	0dB
		001	6dB
		—	6dB steps
		110	36dB
		111	42dB
27	UNUSED		
29:28	SINP_MODE		SODP Input Mode
		00	No Signal Applied
		01	OUT1 Input to SODP
		10	OUT2 Input to SODP
		11	Average (OUT1+OUT2/2)
30	FS	0	48ksps
		1	44.1ksps
31	SODP_EN	0	Speaker Overdrive protection Disabled
		1	Speaker Overdrive protection Enabled

SPEAKER OVERDRIVE PROTECTION THRESHOLD REGISTER (SODP_THRESHOLD) (0x532h)

Table 31. Filter Debug Register 1

BIT	NAME	VALUE	DESCRIPTION
7:0	LEVEL1		Output Level Threshold. Set LEVEL1 such that signals above LEVEL1 increase die temperature. Signal levels above LEVEL1 are added to the estimated audio energy in a given time window.
15:8	LEVEL2		Output Level Threshold. Set LEVEL2 such that signals below LEVEL2 reduce die temperature. Signal levels below LEVEL2 are subtracted from the estimated audio energy in a given time window.
23:16	INT_TH1		Attack Threshold. Integrator level above INT_TH1 enables the SOPD, reducing device gain.
31:24	INT_TH2		Release Threshold. Integrator level below INT_TH2 disables the SOPD, increasing device gain.

LOW POWER CONTROL REGISTER (0x533h)

Table 32. Low Power Configuration Register

BIT	NAME	VALUE	DESCRIPTION
0	AUDET_EN	0	Disable Wake up On Audio Signal
		1	Enable Wake up On Audio Signal
2:1	AUDET_LEVEL		Wake Up Detection Threshold
		00	25mV
		01	50mV
		10	75mV
		11	100mV
3	UNUSED		

Table 32. Low Power Configuration Register (continued)

BIT	NAME	VALUE	DESCRIPTION
5:4	LPWR_MODE		Low Power Mode
		00	Normal Mode. No power saving modes enabled
		01	Analog Audio Detect Mode. Input signal compared to AUDET_LEVEL.
		10	ADC Audio Detect Mode
		11	Digital Audio Detect Mod. Rising edge on I2S WS enables the device.
7:6	UNUSED		
11:8	TIMEOUT_DLY		Time Out Delay. Delay time between no audio detected and the device entering low power mode.
		0000	10ms
		0001	20ms
		0010	50ms
		0011	100ms
		0100	200ms
		0101	500ms
		0110	1s
		0111	2s
		1000	5s
		1001	10s
		1010	20s
		1011	50s
		1100	60s
		1101	80s
		1110	100s
		1111	200s
23:12	ADC_TH		ADC Audio Detection Threshold
24	OVR_OUT2_RST	1	Override OUT2 Reset
25	OVR_OUT1_RST	1	Override OUT1 Reset
26	OVR_OUT1_EN	1	Override OUT1 Enable
27	OVR_OUT2_EN	1	Override OUT2 Enable
28	OVR_VREF_EN	1	Override Reference Enable
29	OVR_PLL_EN	1	Override PLL Enable
30	OVR_ADCR_EN	1	Override Right Channel ADC Enable
31	OVR_ADCL_EN	1	Override Left Channel ADC Enable

SYSTEM STATUS REGISTER (SYS_STAT) (0x538h) READ ONLY

Table 33. MBIST Status Register

BIT	NAME	VALUE	DESCRIPTION
1:0	MBIST_DONE		Logic HIGH indicates memory test complete
3:2	MBIST_GO		Logic Low indicates memory fault when MBIST_DONE is HIGH
5:4	MBIST_EN	0	MBIST Read-back Disabled
		1	MBIST Read-back Enabled
8:6	UNUSED		
9	DEV_EXISTS		Logic HIGH indicates the presence of an EEPROM
10	BUS_ERR		Logic HIGH indicates an I^2C bus error during EEPROM read
11	CL_ACTIVE		Logic HIGH indicates the I^2C master is active and loading from the EEPROM

Table 33. MBIST Status Register (continued)

BIT	NAME	VALUE	DESCRIPTION
16:12	UNUSED		
31:16	MEM_ADDR		Memory Address

DEVICE ID REGISTER (0x539h) READ ONLY

Table 34. Device ID Register

BIT	NAME	VALUE	DESCRIPTION
31:0	CHIP_ID	4890_3AA0h	32-bit Device ID

SPEAKER OVERDRIVE PROTECTION DEBUG REGISTER (0x53Ah) READ ONLY

Table 35. Speaker Overdrive Debug Register

BIT	NAME	VALUE	DESCRIPTION
23:0	SODP_INT		Current Integrator Value
31:24	GAINED_INT_MAG		Integrator Magnitude. 8 most significant bits of the integrator magnitude

DEVICE ADDRESS

The 0110000X is the defaultLM48903 I^2C address hard coded into the device. An alternate device address can be programmed, via the SYS CONFIG (0x530h) Register. Use the default address during initial device configuration.

GENERAL AMPLIFIER FUNCTION

Class D Amplifier

The LM48903 features stereo efficiency Class D audio power amplifiers that utilizes Texas Instruments' filterless modulation scheme external component count, conserving board space and reducing system cost. The Class D outputs transition from V_{DD} to GND with a 384kHz switching frequency. With no signal applied, the outputs switch with a 50% duty cycle, in phase, causing the two outputs to cancel. This cancellation results in no net voltage across the speaker, thus there is no current to the load in the idle state.

With the input signal applied, the duty cycle (pulse width) of the LM48903 outputs changes. For increasing output voltage, the duty cycle of OUT_+ increases while the duty cycle of OUT_- decreases. For decreasing output voltages, the converse occurs. The difference between the two pulse widths yield the differential output voltage.

Edge Rate Control (ERC)

The LM48903 features Texas Instruments' advanced edge rate control (ERC) that reduces EMI, while maintaining high quality audio reproduction and efficiency. The LM48903 ERC greatly reduces the high frequency components of the output square waves by controlling the output rise and fall times, slowing the transitions to reduce RF emissions, while maximizing THD+N and efficiency performance. The overall result of the E^2S system is a filterless Class D amplifier that passes FCC Class B radiated emissions standards with 24in of twisted pair cable, with excellent 0.08% THD+N and high 91% efficiency.

POWER DISSIPATION AND EFFICIENCY

The major benefit of a Class D amplifier is increased efficiency versus a Class AB. The efficiency of the LM48903 is attributed to the region of operation of the transistors in the output stage. The Class D output stage acts as current steering switches, consuming negligible amounts of power compared to their Class AB counterparts. Most of the power loss associated with the output stage is due to the IR loss of the MOSFET on-resistance, along with switching losses due to gate charge.

ANALOG INPUT

The LM48903 features a stereo, 18-bit, differential ADC for systems without a digital audio source. The ADC front end includes a variable gain preamplifier with 4 gain settings, 0dB, 2.4dB, 3.5dB, and 6dB. The preamplifier gain is controlled by bits 0 and 1 (ANA_LVL) of the Analog Configuration Register (0x523h). The analog inputs can be configured as either differential or single ended inputs. The differential configuration SNR is 6dB higher than single-ended configuration. The differential input configuration also offers improved common mode rejection (CMRR). The increased CMRR reduces sensitivity to ground offset related noise injection. Configure the LM48903 for single-ended inputs as shown in Figure 12.

The ADC input range is dependent on AV_{DD}. The maximum input swing of each single ADC input, ie INL+, referenced to GND is $0.7*AV_{DD}$. This gives a maximum differential input of $7V_{P-P}$ when AV_{DD} = 5V.

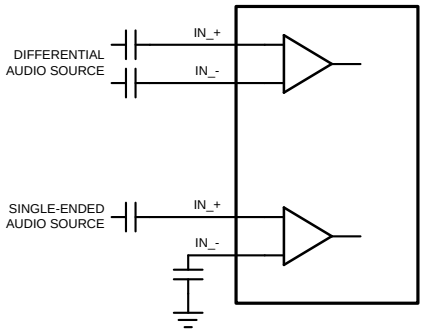


Figure 12. ADC Input Configurations

POWER SUPPLY REQUIREMENTS

At power up, sequence the LM48903 power supplies in the following order:

1) PV_{DD}
2) AV_{DD}/$PLLV_{DD}$
3) DV_{DD}/IOV_{DD}

Ensure $PV_{DD}$is higher or equal to AV_{DD}/$PLLV_{DD}$, and PV_{DD} is always higher than DV_{DD}.

MODULATOR POWER SUPPLY

The AV_{DD1} powers the class D modulators. For maximum output swing, set AV_{DD1} and PV_{DD} to the same voltage. Table 36 shows the output voltage for different AV_{DD1} levels.

Table 36. Amplifier Output Voltage with variable AV_{DD1} Voltage

AV_{DD1} (V)	V_{OUT} (V_{RMS}) @PV_{DD} = 5V, THD+N = 1%	V_{OUT} (V_{RMS}) @PV_{DD} = 3.6V, THD+N = 1%
5	3.3	—
4.5	3.1	—
4.2	2.9	—
4	2.7	—
3.6	2.5	2.4
3.3	2.3	2.2
3	2.1	2.1
2.8	1	1.9

PARALLEL MODE

In Parallel mode, channels OUT1 and OUT2 are driven from the same audio source, allowing the two channels to be connected in parallel, increasing output power to 3.3W into 4Ω at 10% THD+N. Set bit 2 (PARALLEL) of the Analog Configuration Register (0x532h) = 1 to configured the device in Parallel mode. After the device is set to Parallel mode, make an external connection between OUT1+ and OUT2+, and a connection between OUT1- and OUT2- Figure 13. In Parallel mode, the combined channels are driven from the OUT1 source. Signal routing, mixing, filtering, and equalization are done through the Spatial Engine.

Make sure the device is configured in Parallel mode, before connecting OUT1 and OUT2 and enabling the outputs. Do not make a connection between OUT1 and OUT2 together while the outputs are enabled. Disable the outputs first, then make the connections between OUT1 and OUT2.

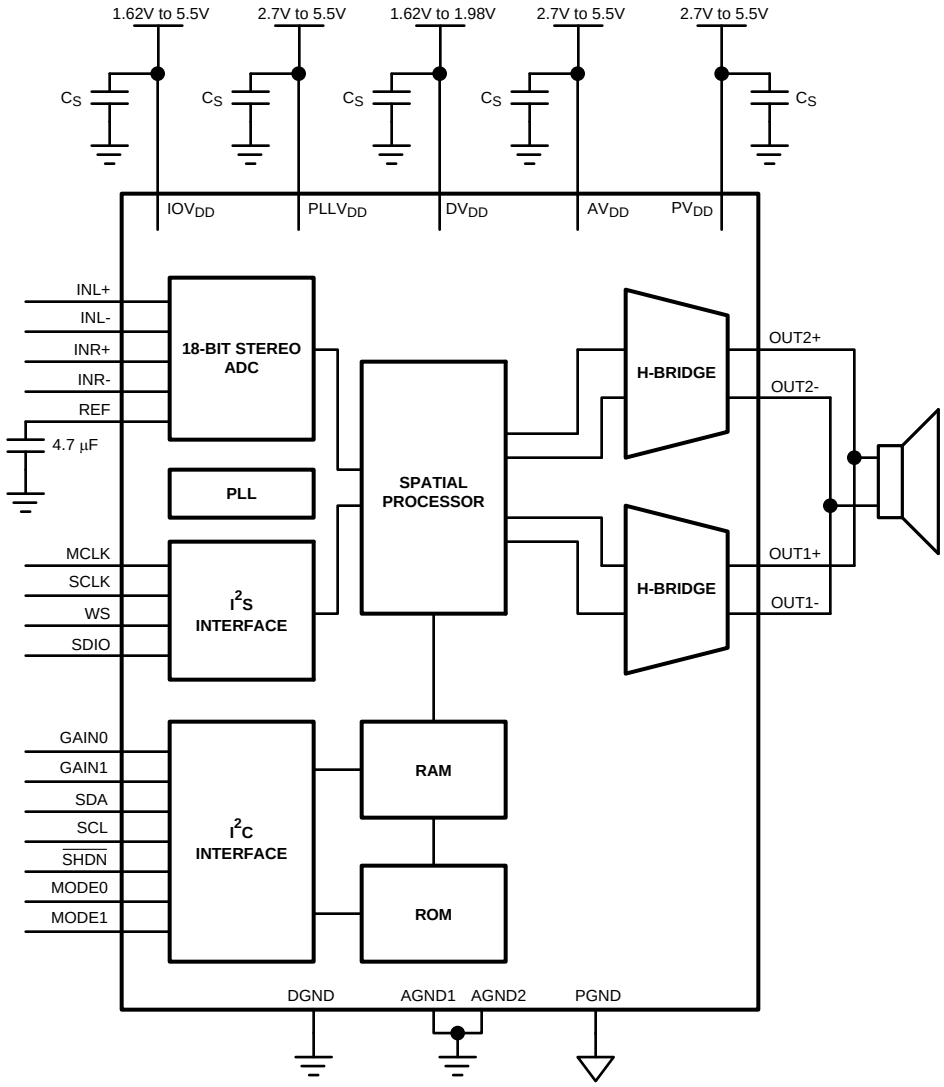


Figure 13. Parallel Mode

GAIN SETTING

I²C Gain Setting

The LM48903 has three gain stages, the ADC preamplifier, and two independent volume controls in the Digital Mixer, one for the ADC path and one for the I²S path. The ADC preamplifier has four gain settings (0dB, 2.4dB, 3.5dB, and 6dB). The preamplifier gain is set by bits 0 and 1 (ANA_LVL) of the Analog Configuration Register (0x523h). The Digital Mixer has two 64 step volume controls. The ADC path volume control is set by bits 5:0 (ADC_LVL) in the Digital Mixer Control Register (0x522h). The I²S path volume control is set by bits 13:8 (I2S_LVL) in the Digital Mixer Control Register (0x522h). Both volume controls have a range of -76.5dB to 18dB in 1.5dB increments.

GAIN1 and GAIN0 Gain Setting

For systems without I2C control, the ADC preamplifier gain is set by GAIN1 and GAIN0. The gain settings are shown in Table 37. The I²C preamplifier gain settings override GAIN1 and GAIN0.

Table 37. Hardware Gain Setting

GAIN1	GAIN0	GAIN (dB)
0	0	0
0	1	2.4
1	0	3.5
1	1	6

ROM MODE

The LM48903 features a ROM with four preset operating modes; three spatial modes, and a stereo mode. The spatial modes are designed for three different speaker distances, 4.5cm, 6cm and 11.5cm. Due to the spatial processing, there may be a perceived Left/Right channel swap when switching between Stereo and the three preset spatial configurations in ROM mode.

The ROM modes are selected through both the I^2C interface and by MODE1/MODE0. For systems without I^2C, MODE1 and MODE0 select the ROM mode as shown in Table 38. For systems with I^2C, bits 11:10 (I2C_SP_MD1 and I2C_SP_MD0) of the SYS_CONFIG register (0x530h) select the ROM mode as shown in Table 39. Set bit 9 (USE_I2C_SP_MD) of the SYS_CONFIG register = 1 to select the ROM mode through I^2C. Set bit 8 (USE_RAM) of the SYS_CONFIG register = 0 (default) to use the preset ROM modes. Set USE_RAM = 1 to use custom spatial coefficients. The LM48903 only accepts analog inputs in ROM mode, I^2S inputs are ignored.

Table 38. ROM Settings, Hardware Mode (USE_I2C_SP_MD = 0)

MODE1	MODE0	DESCRIPTION
0	0	4.5cm Speaker Spacing
0	1	6cm Speaker Spacing
1	0	11.5 Speaker Spacing
1	1	DSP Bypassed, Stereo Mode

Table 39. ROM Settings, I^2C Mode (USE_I2C_SP_MD = 1)

USE_RAM	I2C_SP_MD1	I2C_SP_MD0	DESCRIPTION
0	0	0	4.5cm Speaker Spacing
0	0	1	6cm Speaker Spacing
0	1	0	11.5 Speaker Spacing
0	1	1	DSP Bypassed, Stereo Mode
1	X	X	Custom Spatial Mode. The device bypasses the ROM and loads coefficients from an external source.

SPEAKER OVERDRIVE PROTECTION

Speaker overdrive protection (SODP) monitors the DSP outputs and adjusts the signal path gain to prevent speaker overheating. SODP monitors two levels, LEVEL1, the output amplitude above which the voice coil temperature rises, and LEVEL2 the output amplitude below which the voice coil temperature falls. Speaker Overdrive Protection Threshold Register (0x532h) bits 7:0 set LEVEL1. Bits 15:8 set LEVEL2.

The difference between LEVEL1 and LEVEL2 is the amplitude where the voice coil temperature remains stable. The device integrates the difference between the output signal and LEVEL1 for signals above LEVEL1, and the difference between the output signal and LEVEL2 for signals below LEVEL2. There are two integration time windows. Bits 3:0, (W1), of the Speaker Overdrive Control Register (0x531h), set the duration of Window 1. Window 1 is integration time when during normal operation. Bits 7:4 (W2) set the duration of Window 2. Window 2 is the integration time when the SODP is active, and the device gain is reduced.

At the end of Window 1, the device compares the integrator output the INT_TH1 (0x532h, bits 23:16), or the attack threshold. Bits 19:16, (AT_GAIN), of register 0x531h, set the gain reduction step. Bits 10:8 (AT_RES) set the attack time. For example, if AT_GAIN = 6dB and AT_RES = 5ms, once the integrator output exceeds INT_TH1, the signal path gain is reduced by 6dB in 1.5dB steps over 5ms. Following the gain reduction, the device switches to integrator Window 2. If the integrator output exceeds INT_TH1 again, the gain reduction is repeated until the integrator output no longer exceeds INT_TH1.

The device remains in the reduced gain state until the integrator output falls below INT_TH2 (0x532h, bits 31:24), or the release threshold. Once the integrator output falls below INT_TH2, the device gain is increased to the original gain setting in 1.5dB steps. The release time set by bits 14:12 (RL_RES). Following the gain release, the device switches back to integrator Window 1.

Set register 0x531h bit 21 (SODP_EN) = 1 to enable the speaker overdrive protection.

DSP Output Selection

The DSP outputs to the Digital Mixer can be selected from either of the two Array Filter signal paths. This allows the left and right inputs to be swapped or mixed before being output to the Class Ds. Filter Control Register (0x500h) bits 17:16 (CH1_SEL) the select the Array filter source for DSP1. Bits 19:18 (CH2_SEL) select the Array filter source for DSP2. Use channel routing to correct the perceived left/right channel swap that can occur with certain spatial configurations.

Low Power Mode

The LM48903 features three low power modes that enable and disable the device based on the presence of an input signal. Mode 1 monitors the ADC input signal. Mode 2 monitors the ADC output, and offers a faster wake up time (<10ms) compared to Mode 1. Mode 3 monitors the I^2S interface and enables the device on the rising edge of WS.

The low power mode is configured through the Low Power Control Register (0x533h) (Table 29). Bit 0 (AUDET_EN) enables the automatic signal detection. Bits 2:1 (AUDET_LEVEL) set the ADC input threshold. Bits 5:4 (LPWR_MODE) select the operating mode. Bits 11:8 (TIMEOUT_DLY) sets the delay time between loss of audio signal/WS clock to device disable. Bits 23:12 (ADC_TH) sets the ADC output threshold.

DIGITAL MIXER

The digital mixer Figure 14 is responsible for routing the digital audio signals within the LM48903. The digital mixer is configured through the Digital Mixer register (0x522h). There are six inputs to the digital mixer, left and right ADC data, left and right I^2S RX data, and two DSP output channels. ADC and I^2S RX data can be routed to the DSP inputs (DSP_L and DSP_R), the class D amplifiers (OUT1-OUT2), and the I^2S TX buses. The DSP output data can be routed to the class D amplifiers, and the I^2S TX bus.

The digital mixer includes independent digital gain blocks for the ADC and I^2S RX data. The gain range is -76.5dB to 18dB in 1.5dB steps. The ADC gain is set by bits 5:0 (ADC_LVL) of the Digital Mixer Control Register (0x522h). The I^2S gain is set by bits 13:8 (I2S_LVL) of the Digital Mixer Control Register. With a 0dBFS input and I2S_LVL = 110011 (0dB), the output voltage is $3.36V_{RMS}$.

For additional output routing flexibility, use the digital mixer in conjunction with the Array filter channel routing. The Array filter channel routing control selects which filter channel is output on each DSP output. The DSP must be active to use the Array filter channel routing, however, no coefficients are required. With no spatial effect, Array filter channel contains left channel audio data, channel contains right channel audio data. The Array filter channel routing is controlled by bits 19:16 in the Filter Control Register (0X500h). See DSP Output Selection section.

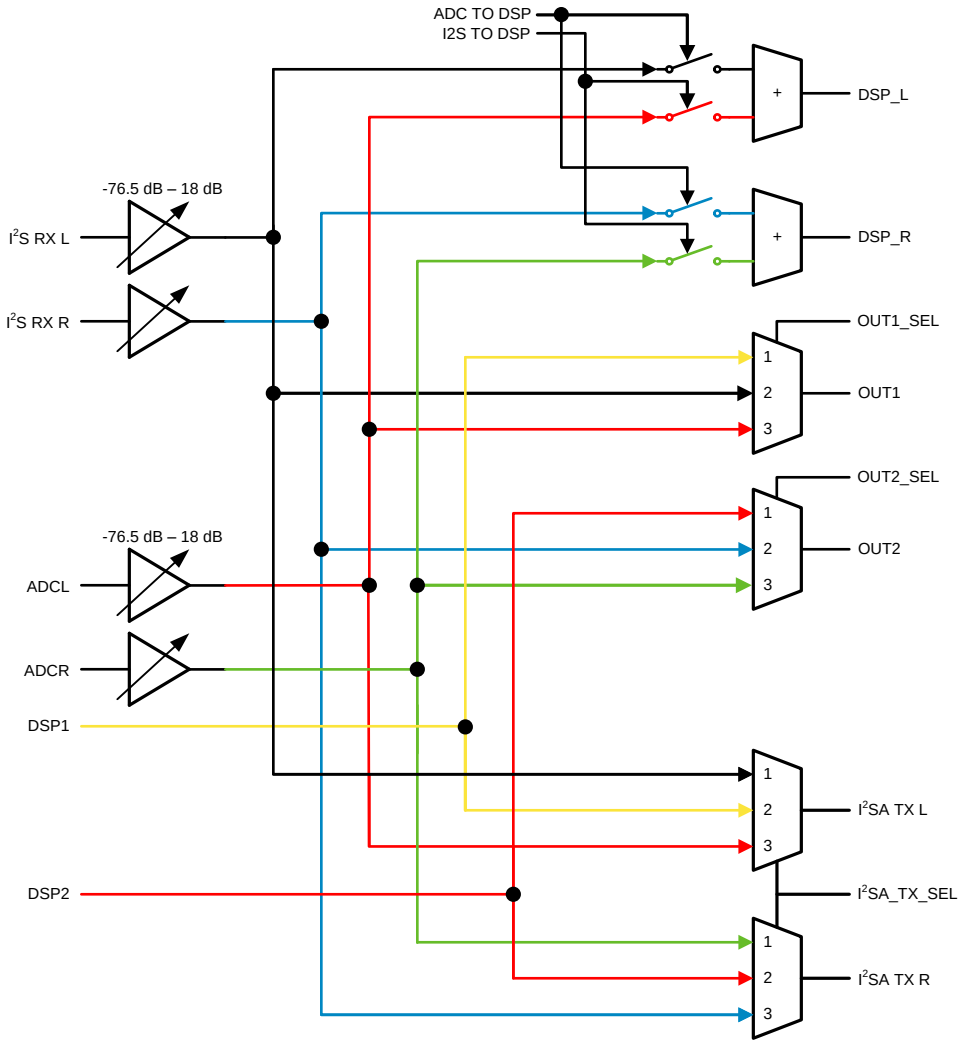


Figure 14. Digital Mixer

SPATIAL ENGINE (DSP)

The LM48903 Spatial Engine is a specialized DSP that is optimized for TI's proprietary spatial audio algorithm. The Spatial Engine consists of two processing stages, the Pre Filter and Array Filter (Figure 14). The filters perform different portions of the spatial processing, and are configured and controlled independent of each other. The Pre Filter uses virtual speaker positioning to set the width of the sound stage. The Array Filter is responsible for equalization and positioning the audio content within the virtual sound stage created by the Pre Filter.

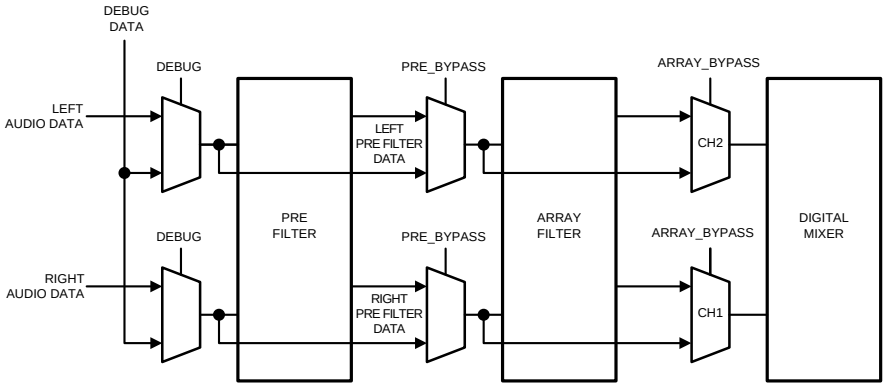


Figure 15. DSP Routing

Filter Enable and Filter Bypass

The Pre Filter and Array Filter are enabled independently. Filter Control Register (0x500h) bit 30 (PRE_ENABLE) enables the Pre Filter, bit 31 (ARRAY_ENABLE) enables the Array Filter. The independent filter enables maximize power savings when only a portion of the LM48903's DSP processing is required.

The filter bypass allows audio data to pass through the DSP without any processing. The Pre Filter and Array Filter can be independently bypassed. Filter Control Register (0x500h) bit 28 (PRE_BYPASS) bypasses the Pre Filter, bit 29 (ARRAY_BYPASS) bypasses the Array Filter. When using a portion of the DSP path, bypass the filter that is not in use. Audio data will not pass through the disabled filter. For example, if the Pre Filter is disabled while the Array Filter is enabled, bypass the Pre Filter.

Compressor

The Pre filter and Array filter each have a compressor that monitors the filter output and maintains the amplitude below the set threshold (Figure 15). The compressors have four user configurable settings, compressor threshold (COMP_TH), pre-compression gain (G1_GAIN), compression ratio (COMP_RATIO), and post compression gain (POST_GAIN). COMP_TH sets the threshold above which the compression is applied to the filter output signal. G1_GAIN sets the gain applied before compression. COMP_RATIO sets the linear compression ratio applied to the filter output signal. POST_GAIN sets the post compression gain, increasing the compressor output signal when either COMP_TH is low or COMP_RATIO is high.

Compressor Control Register 1 (0x501h) configures the Pre Filter compressor. Bits 4:0 (COMP_TH) set the Pre Filter compressor threshold. Bits 7:5 (G1_GAIN set the Pre Filter pre-compression gain. Bits 10:8 (COMP_RATIO) set the Pre Filter compression ratio. Bits 14:12 (POST_GAIN) set the post compression gain.

The Array Filter outputs can be routed through one of two compressors, allowing different signal paths to have different compression profiles. This feature is useful if the LM48903 outputs are driving different speakers, for example, two tweeters and two subwoofers. One compression profile is applied to the tweeter channels, while the second compression profile is applied to the subwoofer channels. Bits 19:16 of Compressor Control Register 1 and Compressor Control Register 2 (0x502h) configure the Array Filter. Bits 14:0 of the Compressor Control Register 2 configure the Array Filter compressor 0. Bits 30:16 configure the Array Filter compressor 1. The Compressor Control Register 1 bits 17:16 (ARRAY_COMP_SELECT) selects the compressor setting used by each Array Filter channel. Bit 16 controls DSP channel 1, bit 17 controls DSP channel 2. Set the desired channel ARRAY_COMP_SELECT bit = 0 to select compressor 0, set the desired channel ARRAY_COMP_SELECT bit = 1 to select compressor 1.

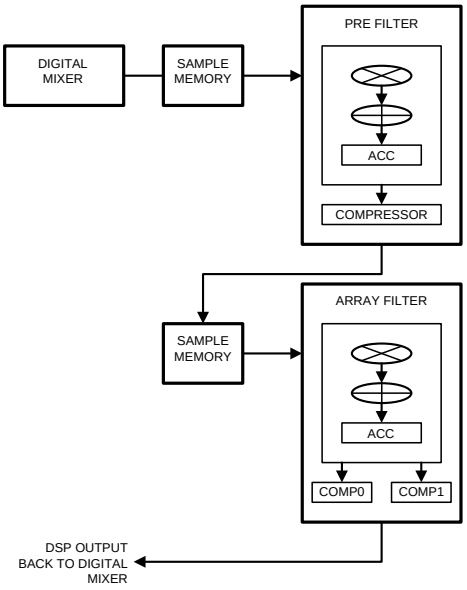


Figure 16. DSP Core Diagram

DSP Output Selection

CLOCK REQUIREMENTS

The LM48903 requires an external clock source for proper operation, regardless of input source or device configuration. The device derives the ADC, digital mixer, DSP, I^2S port, and PWM clocks from the external clock. The clock can be derived from either MCLK or SCLK inputs. Set bit 11 (I^2S_CLK) of the Enable and Clock configuration register (0x521h) to 0 to select MCLK, set I^2S_CLK to 1 to select SCLK. The LM48903 accepts five different clock frequencies, 1.536, 3.072, 6.114, 12.288, and 24.576MHz. Set bits 10:8 (MCLK_RATE) of the Enable and Clock Configuration Register to the appropriate clock frequency. In systems where both MCLK and SCLK are available, choose the lower frequency clock for improved power consumption.

SHUTDOWN FUNCTION

There are two ways to shutdown the LM48903, hardware mode, and software mode. The default is hardware mode.

Set bit 1 (FORCE) of the Enable and Clock Configuration Register (0x521h) to 0 to enable hardware shutdown mode. In hardware mode, the device is enabled and disabled through $\overline{SHDN}$. Connect $\overline{SHDN}$ to V_{DD} for normal operation. Connect $\overline{SHDN}$ to GND to disable the device. Hardware shutdown mode supports a one shot, or momentary switch $\overline{SHDN}$ input. When bit 2 (PULSE) of the Enable and Clock Configuration Register (0x521h) is set to 1, the LM48903 responds to a rising edge on $\overline{SHDN}$ to change the device state. When PULSE = 0, the device requires a stable logic level on $\overline{SHDN}$.

Set FORCE = 1 to enable software shutdown mode. In software shutdown mode, the device is enabled and disabled through bit 0 (ENABLE) of the Enable and Clock Configuration Register (0x512h). Set ENABLE = 0 to disable the LM48903. Set ENABLE = 1 to enable the LM48903.

In either hardware or software mode, the content of the LM48903 memory registers is retained after the device is disabled, as long as power is still applied to the device. Minimize power consumption by disabling the PMC clock oscillator when the LM48903 is shutdown. Set bit 12 (PMC_CLK_SEL) and bit 14 (QSA_CLK_STOP) of the Enable and Clock configuration Register (0x521h) = 1 to disable the PMC clock oscillator.

EXTERNAL CAPACITOR SELECTION

Power Supply Bypassing and Filtering

Proper power supply bypassing is critical for low noise performance and high PSRR. Place the supply bypass capacitors as close to the device as possible. Typical applications employ a voltage regulator with 10µF and 0.1µF bypass capacitors that increase supply stability. These capacitors do not eliminate the need for bypassing of the LM48903 supply pins. A 1µF capacitor is recommended for IOV_{DD}, $PLLV_{DD}$, DV_{DD}, and AV_{DD}. A 2.2µF capacitor is recommended for PV_{DD}.

REF and BYPASS Capacitor Selection

For best performance, bypass REF with a 4.7µF ceramic capacitor.

INPUT CAPACITOR SELECTION

The LM48903 analog inputs require input coupling capacitors. Input capacitors block the DC component of the audio signal, eliminating any conflict between the DC component of the audio source and the bias voltage of the LM48903. The input capacitors create a high-pass filter with the input resistors R_{IN}. The -3dB point of the high pass filter is found using Equation (1) below.

$$f = 1 / 2\pi R_{IN} C_{IN} \quad (1)$$

Where the value of R_{IN} is 20kΩ.

The input capacitors can also be used to remove low frequency content from the audio signal. Small speakers cannot reproduce, and may even be damaged by low frequencies. High pass filtering the audio signal helps protect the speakers. When the LM48903 is using a single-ended source, power supply noise on the ground is seen as an input signal. Setting the high-pass filter point above the power supply noise frequencies, 217Hz in a GSM phone, for example, filters out the noise such that it is not amplified and heard on the output. Capacitors with a tolerance of 10% or better are recommended for impedance matching and improved CMRR and PSRR.

PCB LAYOUT GUIDELINES

As output power increases, interconnect resistance (PCB traces and wires) between the amplifier, load, and power supply create a voltage drop. The voltage loss due to the traces between the LM48903 and the load results in lower output power and decreased efficiency. Higher trace resistance between the supply and the LM48903 has the same effect as a poorly regulated supply, increasing ripple on the supply line, and reducing peak output power. The effects of residual trace resistance increases as output current increases due to higher output power, decreased load impedance or both. To maintain the highest output voltage swing and corresponding peak output power, the PCB traces that connect the output pins to the load and the supply pins to the power supply should be as wide as possible to minimize trace resistance.

The use of power and ground planes will give the best THD+N performance. In addition to reducing trace resistance, the use of power planes creates parasitic capacitors that help to filter the power supply line.

The inductive nature of the transducer load can also result in overshoot on one of both edges, clamped by the parasitic diodes to GND and V_{DD} in each case. From an EMI standpoint, this is an aggressive waveform that can radiate or conduct to other components in the system and cause interference. In is essential to keep the power and output traces short and well shielded if possible. Use of ground planes beads and micros-strip layout techniques are all useful in preventing unwanted interference.

As the distance from the LM48903 and the speaker increases, the amount of EMI radiation increases due to the output wires or traces acting as antennas become more efficient with length. Ferrite chip inductors places close to the LM48903 outputs may be needed to reduce EMI radiation.

Revision History

Rev	Date	Description
1.0	04/12/12	Initial WEB released.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
LM48903TLE/NOPB	ACTIVE	DSBGA	YZR	30	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	
LM48903TLX/NOPB	ACTIVE	DSBGA	YZR	30	1000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	

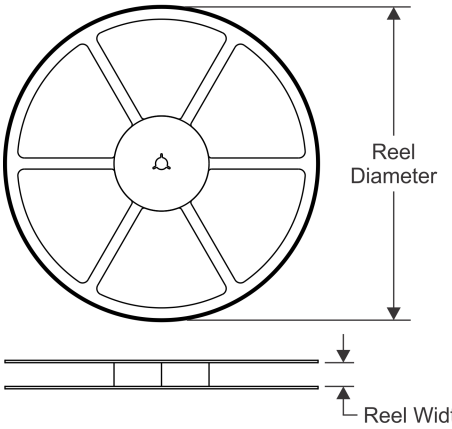
(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

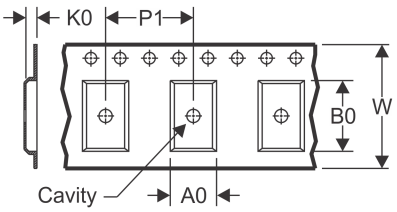
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

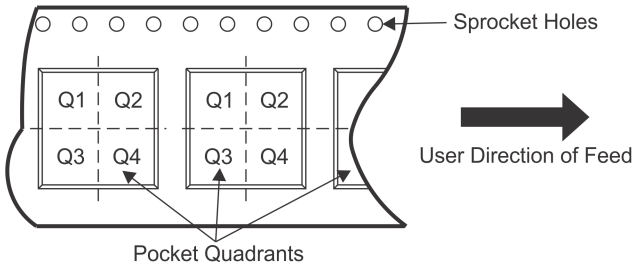


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

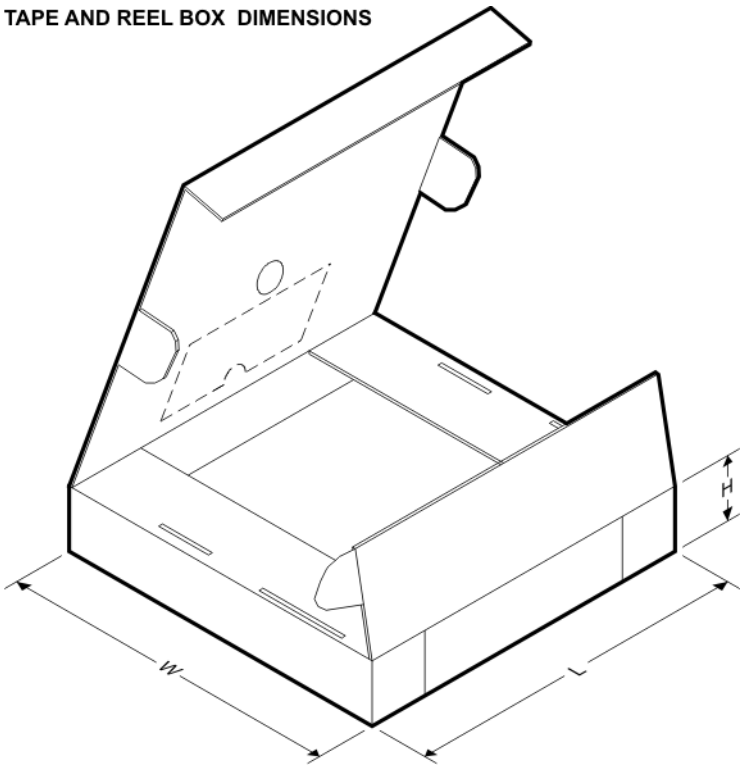
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM48903TLE/NOPB	DSBGA	YZR	30	250	178.0	12.4	2.87	3.39	0.76	8.0	12.0	Q1
LM48903TLX/NOPB	DSBGA	YZR	30	1000	178.0	12.4	2.87	3.39	0.76	8.0	12.0	Q1

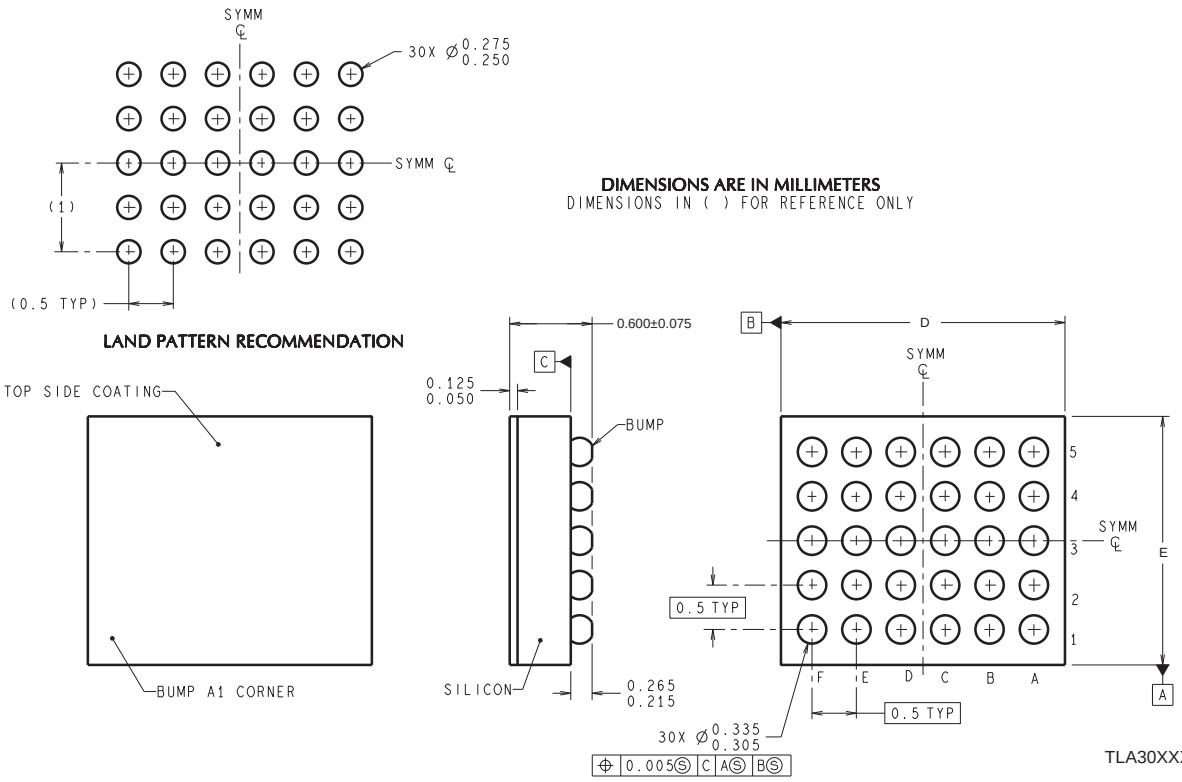
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM48903TLE/NOPB	DSBGA	YZR	30	250	203.0	190.0	41.0
LM48903TLX/NOPB	DSBGA	YZR	30	1000	206.0	191.0	90.0

YZR0030



D: Max = 3.232 mm, Min =3.132 mm

E: Max = 2.708 mm, Min =2.608 mm

4215057/A 12/12

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.

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