LM4931 Boomer™ Audio Power Amplifier Series Audio Subsystem with Mono High Efficiency Loudspeaker and Stereo Headphone Amplifiers

Check for Samples: LM4931

FEATURES

- **18-bit 44.1kHz or 48kHz Stereo DAC**
- **16-bit 8kHz , 12kHz , 16kHz, or 24kHz Voice-Band Codec**
- **PLL for Operation from Common System Clocks**
- **Either I^2C or SPI Compatible Serial Interface**
- **I^2S Digital Audio Data Serial Interface**
- **PCM Voice Audio Data Serial Interface**
- **Differential Analog Microphone Input**
- **26mW/Channel Stereo Headphone Amplifier**
- **570mW Mono High Efficiency BTL 8Ω Amplifier**
- **32-step Volume Control for Audio Output Amplifiers with 1.5dB Step Size.**
- **Unity-Gain Stable Headphone Amplifiers**
- **No Snubber Networks or Bootstrap Capacitors are Required by the Headphone or Hands-Free Amplifiers**
- **Adjustable Digital Side-Tone Attenuation**
- **16-step Volume Control for Microphone Preamp with 2dB Step Size**
- **Configurable GPIO/Status Port**
- **Available in the 42 bump DSBGA Package**

APPLICATIONS

- **2.5 and 3G Mobile Phones and Multimedia Terminals**
- **PDAs, Internet Appliances and Portable Gaming**
- **Portable DVD/CD/AAC/MP3 Players**
- **Digital Cameras and Toys**

APPLICATIONS

- **$P_{LS\ OUT}$ at AV_{DD} = 5V, 8Ω**
  - **1% THD+N, 1.1W (Typ)**
- **$P_{LS\ OUT}$ at AV_{DD} = 3.3V, 8Ω**
  - **1% THD+N, 570mW (Typ)**
- **$P_{H/P\ OUT}$ at AV_{DD} = 5V & AV_{DD} = 3.3V, 32Ω**
  - **1% THD+N, 26mW (Typ)**
- **Supply Voltage Range**
  - **DV_{DD}, 2.7V to 4.0V**
  - **AV_{DD}, 2.7V to 5.0V(1)**
- **Shutdown Current, 1.1µA**
- **PSRR at 217Hz, AV_{DD} = 3V, 62dB (Typ)**
- **SNR (Voice Codec), 75dB (Typ)**
- **SNR (Audio DAC), 86dB (Typ)**

DESCRIPTION

The LM4931 is an integrated audio subsystem that supports voice and digital audio functions. The LM4931 includes a high quality stereo DAC, voice band codec, a stereo headphone amplifier and a high-power high efficiency mono speaker amplifier. It is primarily designed for demanding applications in mobile phones and other portable devices.

The LM4931 features an I^2S serial interface for full range audio, a 16-bit PCM bi-directional serial interface for the voice band codec and an I^2C/SPI compatible interface for control. The full range music path features an SNR of 86dB with an 18-bit 48kHz input. The headphone amplifier delivers at least $26mW_{RMS}$ to a 32Ω single-ended stereo load with less than 1% distortion (THD+N) when AV_{DD} = $3.3V_{DC}$. The mono speaker amplifier delivers up to $570mW_{RMS}$ into an 8Ω load with less than 1% distortion when AV_{DD} = $3.3V_{DC}$.

(1) Best operation is achieved by maintaining $3.0V \le AV_{DD} \le 5.0$ and $3.0V \le DV_{DD} \le 3.6V$ and $AV_{DD} \ge DV_{DD}$.

DESCRIPTION (CONTINUED)

The LM4931 employs advanced techniques to reduce power consumption, to reduce controller overhead, and to eliminate click and pop. Boomer audio power amplifiers were designed specifically to provide high quality output power with a minimal amount of external components. It is therefore ideally suited for mobile phone and other low voltage applications where minimal power consumption, PCB area, and cost are primary requirements.

Typical Application

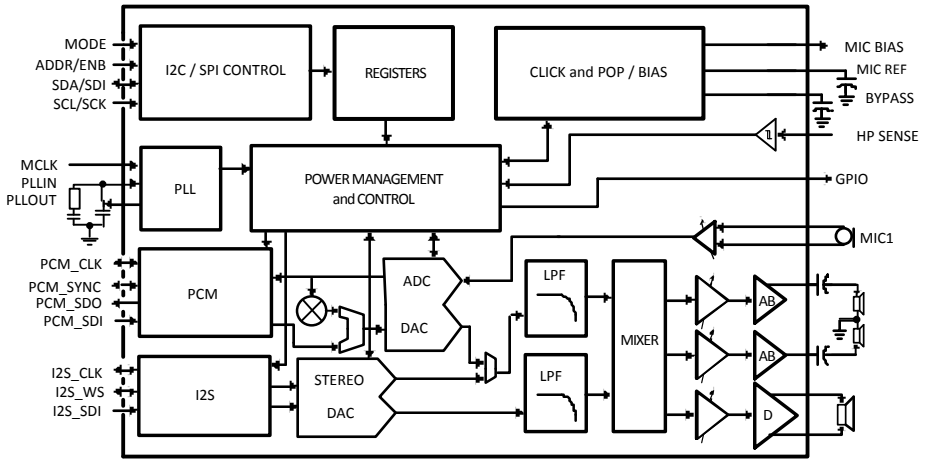


Figure 1. Typical I^2S + Voice codec application circuit for mobile phones

Connection Diagram

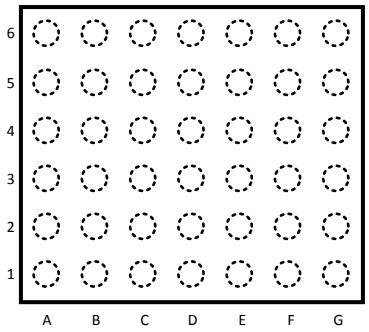


Figure 2. 42-Bump DSBGA
(Top View)
See Package Number YZR0042

PIN DESCRIPTIONS

PIN	PIN NAME	D/A	I/O	DESCRIPTION
A1	MIC_P	A	I	Microphone positive differential input
A2	MIC_N	A	I	Microphone negative differential input
A3	VDD(MIC)	A	I	Analog Vdd for microphone section
A4	MODE	D	I	Selects between SPI and I^2C control interfaces (I^2C = 0, SPI = 1)
A5	SDA/SDI	D	I/O	I^2C_SDA or SPI_SDI depending on the MODE control
A6	NC	N/A	N/A	No Connect
B1	MIC_P	A	I	Microphone positive differential input
B2	MIC_BIAS	A	O	2V ultra clean power supply for microphones
B3	BYPASS	A	I	Click and Pop / VDD/2 reference filter
B4	ADDR/ENB	D	I	I^2C_ADDR or SPI_ENB depending on the MODE control
B5	SCL/SCK	D	I	I^2C_SCL or SPI_SCK depending on the MODE control
B6	PCM_SDI	D	I	PCM_SDI voice data input
C1	VSS(MIC)	A	I	Analog Vss for microphone section
C2	MIC_REF	A	I	Filter for microphone power supply
C3	NC	N/A	N/A	No Connect
C4	PCM_SDO	D	O	PCM_SDO serial data output
C5	PCM_SYNC	D	I/O	PCM_SYNC pulse for the PCM bus
C6	PCM-CLK	D	I/O	PCM_SYNC pulse for the PCM bus
D1	HPL	A	O	Left Headphone output
D2	VSS(HP)	A	I	Analog Vss for Headphone and Mixer sections
D3	VSS(HP)	A	I	Analog Vss for Headphone and Mixer sections
D4	I^2S_SDI	D	I	I^2S serial data input
D5	I^2S_CLK	D	I/O	I^2S clock signal
D6	VSSD	D	I	Digital Vss
E1	VDD(HP)	A	I	Analog Vdd for Headphone and Mixer sections
E2	HPR	A	O	Right Headphone output
E3	GPIO	D	O	Configurable multi purpose output
E4	I^2S_WS	D	I/O	I^2S word select signal
E5	MCLK	D	I	Input clock from 10MHz - 24.576MHz
E6	VDDD	D	I	Digital Vdd
F1	LS+	A	O	Loudspeaker positive output
F2	VDD(LS)	A	I	Analog Vdd for Loudspeaker section
F3	HP_SENSE	A	I	Input for headphone connection sense circuit
F4	NC	N/A	N/A	No Connect
F5	PLL_OUT	D	O	PLL filter output
F6	VDD(PLL)	D	I	Digital Vdd for PLL section
G1	LS+	A	O	Loudspeaker positive output
G2	VSS(LS)	A	I	Analog Vss for Loudspeaker section
G3	LS-	A	O	Loudspeaker negative output
G4	VSS(PLL)	D	I	Digital Vss for PLL section
G5	PLL_IN	D	I	PLL filter input
G6	VDD(PLL)	D	I	Digital Vdd for PLL section

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings(1)(2)

Analog Supply Voltage		6.0V
Digital Supply Voltage		6.0V
Storage Temperature		-65°C to +150°C
Power Dissipation(3)		Internally Limited
ESD Susceptibility	Human Body Model(4)	2500V
	Machine Model(5)	200V
Junction Temperature		150°C
Thermal Resistance	θ_{JA} - YZR0042	105°C/W

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional but do not guarantee specific performance limits. Electrical Characteristics state DC and AC electrical specifications under particular test conditions which guarantee specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not guaranteed for parameters where no limit is given, however, the typical value is a good indication of device performance.
(2) All voltages are measured with respect to the relevant GND pin unless otherwise specified. All grounds should be coupled as close as possible to the device.
(3) The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{JMAX} ,θ_{JA}, and the ambient temperature, T_A. The maximum allowable power dissipation is $P_{DMAX} = (T_{JMAX} – T_A) / \theta_{JA}$ or the number given in Absolute Maximum Ratings, whichever is lower. For the LM4931, see power derating currents for more information.
(4) Human body model: 100pF discharged through a 1.5kΩ resistor.
(5) Machine model: 220pF - 240pF discharged through all pins.

Operating Ratings

Temperature Range	$T_{MIN} \le T_A \le T_{MAX}$	$-40°C \le T_A \le +85°C$
Supply Voltage	DV_{DD}(1)	2.7V - 4.0V
	AV_{DD}(1)	2.7V - 5.0V

(1) Best operation is achieved by maintaining $3.0V \le AV_{DD} \le 5.0$ and $3.0V \le DV_{DD} \le 3.6V$ and $AV_{DD} \ge DV_{DD}$.

Electrical Characteristics DV_{DD} = 3V, AV_{DD} = 3V, R_{LHP} = 32Ω, R_{LHF} = 8Ω(1)(2)

The following specifications apply for the circuit shown in Figure 62, unless otherwise specified. Limits apply for T_A = 25°C.

Symbol	Parameter	Conditions	LM4931		Units (Limits)
			Typical(3)	Limits(4)	
Power					
DI_{SD}	Digital Shutdown Current	Mode 0			
		f_{MLCK} = 12MHz(5)	400	500	µA (max)
		No MCLK	1	2	µA (max)
DI_{ST}	Digital Standby Current	Mode 1, f_{MCLK} = 12MHz	400	1200	µA (max)
DI_{DD}	Digital Power Supply Current	f_{MLCK} = 12MHz			
		Mode 2, 3, 4	1.3	3.2	mA (max)
		Mode 5, 6, 7	2.8	7	mA (max)
		Mode 8, 9, 10	3.2	7.5	mA (max)
$PLLI_{DD}$	PLL Quiescent Current	f_{MCLK} = 12MHz	2.8	3.5	mA (max)
AI_{SD}	Analog Shutdown Current	Mode 0, No load	0.1	2.5	µA (max)
AI_{ST}	Analog Standby Current	Mode 1, No load	100	200	µA (max)

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional but do not guarantee specific performance limits. Electrical Characteristics state DC and AC electrical specifications under particular test conditions which guarantee specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not guaranteed for parameters where no limit is given, however, the typical value is a good indication of device performance.
(2) All voltages are measured with respect to the relevant GND pin unless otherwise specified. All grounds should be coupled as close as possible to the device.
(3) Typicals are measured at 25°C and represent the parametric norm.
(4) Limits are guaranteed to National's AOQL (Average Outgoing Quality Level).
(5) Digital shutdown current is measured with system clock set for PLL output while the PLL is disabled.

Electrical Characteristics DV_{DD} = 3V, AV_{DD} = 3V, R_{LHP} = 32Ω, R_{LHF} = 8Ω[1][2] (continued)

The following specifications apply for the circuit shown in Figure 62, unless otherwise specified. Limits apply for T_A = 25°C.

Symbol	Parameter	Conditions	LM4931		Units (Limits)
			Typical[3]	Limits[4]	
AI_{DD}	Analog Power Supply Quiescent Current	No Load			
		Mode 2	7.8	19	mA (max)
		Mode 3	5.3	10	mA (max)
		Mode 4	8.6	15	mA (max)
		Mode 5	8.4	15	mA (max)
		Mode 6	6.0	15	mA (max)
		Mode 7	9.2	15	mA (max)
		Mode 8, 9, 10	10.1	16	mA (max)
Loudspeaker Amplifier					
V_{FS}	Full-Scale Output Voltage Loudspeaker Amplifier)	8Ω load, 0dB gain setting	2.6		V_{P-P}
THD+N	Total Harmonic Distortion + Noise	f_{OUT} = 1kHz, P_{OUT} = 200mW	0.4		%
P_{OLS}	Loudspeaker Amplifier Output Power	THD = 1% (max), f_{OUT} = 1kHz	470	350	mW (min)
PSRR	Power Supply Rejection Ratio (Loudspeaker Amplifier)	C_B = 1.0µF V_{RIPPLE} = 200mV_{P-P} f_{RIPPLE} = 217Hz	54		dB
SNR (Voice)	Signal-to-Noise Ratio of Voice Channel (Loudspeaker Amplifier)	Signal = V_O at 0dBFS, f = 1kHz, Noise = digital zero, A-weighted, 0dB gain setting[6]			
		f_{MCLK} = 12.288MHz, PLL disabled	71		dB
		f_{MCLK} = 12MHz, PLL active	70		dB
SNR (Music)	Signal-to-Noise Ratio of Music Channel (Loudspeaker Amplifier) Output Noise	Signal = V_O at 0dBFS, f = 1kHz, Noise = digital zero, A-weighted, 0dB gain setting[6]			
		f_{MCLK} = 12.288MHz, PLL disabled	78		dB
		f_{MCLK} = 12MHz, PLL active	76		dB
e_N (Music)	Output Noise	A-weighted filter, V_{in} = digital zero[7]			
		f_{MCLK} = 12.288MHz, PLL disabled	120		µV
		f_{MCLK} = 12MHz, PLL active	140		µV
V_{OS}	Offset Voltage		10		mV
VCR	Volume Control Range (Loudspeaker Amplifier)	Minimum Gain	–34.5		dB
		Maximum Gain	12		dB
SS	Volume Control Step Size (Loudspeaker Amplifier)		1.5		dB
Headphone Amplifier					
V_{FS}	Full Scale Ouput Voltage (Headphone Amplifier)	32Ω load, 0dB gain setting	2.6		V_{P-P}
THD+N	Total Harmonic Distortion + Noise (Headphone Amplifier)	f_{IN} = 1kHz, P_{OUT} = 7.5mW, 32Ω stereo load	0.04		%
P_{OHP}	Output Power (Headphone Amplifier)	THD = 0.5%, f_{OUT} = 1KHz	26	19	mW (min)
PSRR	Power Supply Rejection Ratio (Headphone Amplifier)	C_B = 1.0µF V_{RIPPLE} = 200mV_{PP} f_{RIPPLE} = 217Hz	62		dB

(6) Disabling or bypassing the PLL will result in an improvement in noise measurements.
(7) Disabling or bypassing the PLL will result in an improvement in noise measurements.

Electrical Characteristics DV_{DD} = 3V, AV_{DD} = 3V, R_{LHP} = 32Ω, R_{LHF} = 8Ω[1][2] (continued)

The following specifications apply for the circuit shown in Figure 62, unless otherwise specified. Limits apply for T_A = 25°C.

Symbol	Parameter	Conditions	LM4931		Units (Limits)
			Typical[3]	Limits[4]	
SNR (Voice)	Signal-to-Noise Ratio of Voice Channel (Headphone Amplifier)	Signal = V_O at 0dBFS, f = 1kHz and 1% THD+N, Noise = digital zero, A-weighted, 0dB gain setting[7]			
		f_{MCLK} = 12.288MHz, PLL disabled	75		dB
		f_{MCLK} = 12MHz, PLL active	73		dB
SNR (Music)	Signal-to-Noise Ratio of Music Channel (Headphone Amplifier)	Signal = V_O at 0dBFS, f = 1kHz and 1% THD+N, Noise = digital zero, A-weighted, 0dB gain setting[7]			
		f_{MCLK} = 12.288MHz, PLL disabled	86		dB
		f_{MCLK} = 12MHz, PLL active	82		dB
X_{TALK}	Stereo Channel-to-Channel Crosstalk	f_S = 48kHz, f_{IN} = 1kHz sinewave at –3dBFS	62		dB
ΔA_{CH-CH}	Stereo Channel-to-Channel Gain Mismatch		0.3		dB
e_N (Music)	Output Noise	A-weighted filter, Vin = digital zero[7]			
		f_{MCLK} = 12.288MHz, PLL disabled	45		µV
		f_{MCLK} = 12MHz, PLL active	65		µV
VCR	Volume Control Range (Headphone Amplifier)	Minimum Gain	–46.5		dB
		Maximum Gain	0		dB
SS	Volume Control Stepsize (Headphone Amplifier)		1.5		dB
Microphone Amplifier					
V_{BIAS}	Mic Bias Voltage		2		V
GCR	Gain Control Range (Microphone Amplifier)	Minimum Gain	6		dB
		Maximum Gain	36		dB
SS	Gain Control Stepsize (Microphone Amplifier)		2		dB
Voice Codec (Typical numbers are with 1.024MHz voice clock and 8kHz sampling frequency)					
R_{VDAC}	Voice DAC Ripple	300Hz-3.3kHz through headphone output.	+/- 0.15		dB
R_{VADC}	Voice ADC Ripple	300Hz-3.3kHz through headphone output.	+/- 0.25		dB
PB_{VDAC}	Voice DAC Passband	–3dB Point	3.46		kHz
SBA_{VDAC}	Voice DAC Stopband Attenuation	Above 4kHz	72		dB
UPB_{VDAC}	Upper Passband Cutoff Frequency	Upper – 3dB Point	3.47		kHz
LPB_{VDAC}	Lower Passband Cutoff Frequency	Lower – 3dB Point	0.230		kHz
SBA_{VADC}	Voice ADC Stopband Attenuation	Above 4kHz	65		dB
SBA_{NOTCH}	Voice ADC Notch Attenuation	Centered on 55Hz, figure gives worst case attenuation for 50Hz & 60Hz	58		dB
SNR (Voice)	Signal-to-Noice Ratio of Voice Channel (Voice ADC path)	Signal = V_O at 0dBFS, f = 1kHz and 1% THD+N, MIC_P, MIC_N Terminated to ground, A-weighted, 36dB MIC Preamp gain setting[8]			
		f_{MCLK} = 12.288MHz, PLL disabled	81		dB
		f_{MCLK} = 12MHz, PLL active	80		dB
STR	Side Tone Range	Minimum Gain	–30		dB
		Maximum Gain	0		dB

(8) Disabling or bypassing the PLL will result in an improvement in noise measurements.

Electrical Characteristics DV_{DD} = 3V, AV_{DD} = 3V, R_{LHP} = 32Ω, R_{LHF} = 8Ω[1][2] (continued)

The following specifications apply for the circuit shown in Figure 62, unless otherwise specified. Limits apply for T_A = 25°C.

Symbol	Parameter	Conditions	LM4931		Units (Limits)
			Typical[3]	Limits[4]	
SS	Side Tone Step Size		3		dB
Audio DAC (Typical numbers are with 6.144MHz audio clock and 48kHz sampling frequency)					
R_{DAC}	Audio DAC Ripple	20Hz–20kHz through headphone output	+/-0.1		dB
PB_{DAC}	Audio DAC Passband width	–3dB point	22.7		kHz
SBA_{DAC}	Audio DAC Stop band Attenuation	Above 24kHz	76		dB
DR_{DAC}	Audio DAC Dynamic Range	DC – 20kHz	97		dB
SNR_{DAC}	Audio DAC SNR Digital Filter Section	DC – 20kHz	97		dB
PLL					
f_{IN}	Input Frequency on MCLK pin		12	10 25	MHz (min) MHz (max)
SPI/I^2C					
f_{SPI}	Maximum SPI Frequency		400	4000	kHz (max)
$t_{SPISETD}$	SPI Data Setup Time			100	ns (min)
$t_{SPISETENB}$	SPI ENB Setup Time			100	ns (min)
$t_{SPIHOLDD}$	SPI Data Hold Time			100	ns (min)
$t_{SPIHOLDENB}$	SPI ENB Hold Time			100	ns (min)
t_{SPICL}	SPI Clock Low Time			500	ns (min)
t_{SPICH}	SPI Clock HighTime			500	ns (min)
t_{SPIT}	SPI Clock Transition Time			5	ns (min)
f_{CLKI2C}	I^2C_CLK Frequency		400	3400	kHz (max)
$t_{I2CHOLD}$	I^2C_DATA Hold Time			100	ns (min)
t_{I2CSET}	I^2C_DATA Setup Time			100	ns (min)
PCM/I^2S					
f_{CLKPCM}	PCM_CLK Frequency		128		kHz
	PCM_CLK Duty Cycle		50	40 60	% (min) % (max)
f_{CLKI2S}	I^2S_CLK Frequency	I^2S_RES = 0 I^2S_RES = 1	1536 3072		kHz kHz
	I^2S_WS Duty Cycle		50	40 60	% (min) % (max)

Electrical Characteristics DV_{DD} = 3.3V, AV_{DD} = 5V, R_{LHP} = 32Ω, R_{LHF} = 8Ω[1][2]

The following specifications apply for the circuit shown in Figure 1, unless otherwise specified. Limits apply for T_A= 25°C.

Symbol	Parameter	Conditions	LM4931		Units (Limits)
			Typical[3]	Limits[4]	
Power					
DI_{SD}	Digital Shutdown Current	Mode 0			
		f_{MCLK} = 12MHz[5]	500	600	µA (max)
		No MCLK	1		µA (max)
DI_{ST}	Digital Standby Current	Mode 1, f_{MCLK} = 12MHz	500	1600	µA (max)
DI_{DD}	Digital Power Supply Current	f_{MCLK} = 12MHz			
		Mode 2, 3, 4	1.6	3.5	mA (max)
		Mode 5, 6, 7	3.5	8	mA (max)
		Mode 8, 9, 10	4.0	8	mA (max)
$PLLI_{DD}$	PLL Quiescent Current	f_{MCLK} = 12MHz	3.3	4	mA (max)
AI_{DD}	Analog Shutdown Current	Mode 0, No Load	0.6	3	µA (max)
AI_{ST}	Analog Standby Current	Mode 1, No Load	220	450	µA (max)
AI_{DD}	Analog Power Supply Quiescent Current	No Load			
		Mode 2	18.5	32	mA (max)
		Mode 3	7.3	12	mA (max)
		Mode 4	19.6	29	mA (max)
		Mode 5	19.4	30	mA (max)
		Mode 6	8.4	26	mA (max)
		Mode 7	20.5	30	mA (max)
		Mode 8, 9, 10	22	32	mA (max)
Loudspeaker Amplifier					
V_{FS}	Full-Scale Output Voltage (Mono speaker amplifie)r	8Ω load, 0dB gain setting	2.6		V_{P-P}
THD+N	Total Harmonic Distortion + Noise	f_{OUT} = 1kHz, P_{OUT} = 400mW	0.16		%
P_{OLS}	Loudspeaker Amplifier Output Power	THD = 1%, f_{OUT} = 1kHz	1.1		W
PSRR	Power Supply Rejection Ratio (Loudspeaker Amplifier)	C_B = 1.0µF V_{RIPPLE} = 200mV_{PP} f_{RIPPLE} = 217Hz	56		dB
SNR (Voice)	Signal-to-Noise Ratio of Voice Channel (Loudspeaker Amplifier)	Signal = V_O at 0dBFS, f = 1kHz Noise = digital zero, A-weighted 0dB gain setting[6]			
		f_{MCLK} = 12.288MHz, PLL disabled	70		dB
		f_{MCLK} = 12MHz, PLL active	69		dB
SNR (Music)	Signal-to-Noise Ratio of Music Channel (Loudspeaker Amplifier)	Signal = V_O at 0dBFS, f = 1kHz Noise = digital zero, A-weighted 0dB gain setting[6]			
		f_{MCLK} = 12.288MHz, PLL disabled	74		dB
		f_{MCLK} = 12MHz, PLL active	73		dB

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional but do not guarantee specific performance limits. Electrical Characteristics state DC and AC electrical specifications under particular test conditions which guarantee specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not guaranteed for parameters where no limit is given, however, the typical value is a good indication of device performance.
(2) All voltages are measured with respect to the relevant GND pin unless otherwise specified. All grounds should be coupled as close as possible to the device.
(3) Typicals are measured at 25°C and represent the parametric norm.
(4) Limits are guaranteed to National's AOQL (Average Outgoing Quality Level).
(5) Digital shutdown current is measured with system clock set for PLL output while the PLL is disabled.
(6) Disabling or bypassing the PLL will result in an improvement in noise measurements.

Electrical Characteristics DV_{DD} = 3.3V, AV_{DD} = 5V, R_{LHP} = 32Ω, R_{LHF} = 8Ω[1][2] (continued)

The following specifications apply for the circuit shown in Figure 1, unless otherwise specified. Limits apply for T_A= 25°C.

Symbol	Parameter	Conditions	LM4931		Units (Limits)
			Typical[3]	Limits[4]	
e_N (Music)	Output Noise	A-Weighted filter, V_{IN}= digital zero[6]			
		f_{MCLK} = 12.288MHz, PLL disabled	250		µV
		f_{MCLK} = 12MHz, PLL active	320		µV
V_{OS}	Offset Voltage		10		mV
VCR	Volume Control Range (Loudspeaker Amplifier)	Minimum Gain	–34.5		dB
		Maximum Gain	12		dB
SS	Volume Control Step Size		1.5		dB
Headphone Amplifier					
V_{FS}	Full-Scale Output Voltage (Headphone Amplifier)	32Ω stereo load, 0dB gain setting	2.6		V_{P-P}
THD+N	Total Harmonic Distortion + Noise (Headphone Amplifier)	f_{IN} = 1kHz, P_{OUT} = 7.5mW 32Ω stereo load	0.05		%
P_{OHP}	Output Power (Headphone Amplifier)	THD = 0.5%, f_{OUT} = 1kHz	26	20	mW (min)
PSRR	Power Supply Rejection Ratio (Headphone Amplifier)	C_B = 1.0µF V_{RIPPLE} = 200mV_{PP} f_{RIPPLE} = 217Hz	70		dB
SNR (Voice)	Signal-to-Noise Ratio of Voice Channel (Headphone Amplifier)	Signal = V_O at f = 1kHz and 1% THD+N, Noise = digital zero, A-weighted 0dB gain setting[6]			
		f_{MCLK} = 12.288MHz, PLL disabled	75		dB
		f_{MCLK} = 12MHz, PLL active	73		dB
SNR (Music)	Signal-to-Noise Ratio of Music Channel (Headphone Amplifier)	Signal = V_O at f = 1kHz and 1% THD+N, Noise = digital zero, A-weighted 0dB gain setting[7]			
		f_{MCLK} = 12.288MHz, PLL disabled	86		dB
		f_{MCLK} = 12MHz, PLL active	82		dB
X_{TALK}	Stereo Channel-to-Channel Crosstalk	f_S = 48kHz f_{IN} = 1kHz sinewave at –3dBFS	62		dB
ΔA_{CH-CH}	Stereo Channel-to-Channel Gain Mismatch		0.3		dB
e_N (Music)	Output Noise	A-Weighted filter V_{IN} = digital zero[7]			
		f_{MCLK} = 12.288MHz, PLL disabled	45		µV
		f_{MCLK} = 12MHz, PLL active	70		µV
VCR	Volume Control Range (Headphone Amplifier)	Minimum Gain	-46.5		dB
		Maximum Gain	0		dB
SS	Volume Control Step Size (Headphone Amplifier)		1.5		dB
Microphone Amplifier					
V_{BIAS}	Mic Bias Voltage		2		V
GCR	Gain Control Range (Microphone Amplifier)	Minimum Gain	6		dB
		Maximum Gain	36		dB
SS	Gain Control Step Size		2		dB
Voice Codec (Typical numbers arew ith 1.024MHz voice clock and 8kHz sampling frequency					
R_{VDAC}	Voice DAC Ripple	300Hz - 3.3kHz through headphone output	+/-0.15		dB
R_{VADC}	Voice ADC Ripple	300Hz - 3.3kHz through headphone output	+/-0.25		dB
PB_{VDAC}	Voice DAC Passband	–3dB Point	3.46		kHz

(7) Disabling or bypassing the PLL will result in an improvement in noise measurements.

Electrical Characteristics DV_{DD} = 3.3V, AV_{DD} = 5V, R_{LHP} = 32Ω, R_{LHF} = 8Ω[1][2] (continued)

The following specifications apply for the circuit shown in Figure 1, unless otherwise specified. Limits apply for T_A= 25°C.

Symbol	Parameter	Conditions	LM4931		Units (Limits)
			Typical[3]	Limits[4]	
SBA_{VDAC}	Voice DAC Stopband Attenuation	Above 4kHz	72		dB
UPB_{VADC}	Upper Passband Cutoff Frequency	Upper – 3dB Point	3.47		kHz
LPB_{VADC}	Lower Passband Cutoff Frequency	Lower – 3dB Point	0.230		kHz
SBA_{VADC}	Voice ADC Stopband Attenuation	Above 4kHz	65		dB
SBA_{NOTCH}	Voice ADC Notch Attenuation	Centered on 55Hz, figure gives worst case attenuation for 50Hz & 60Hz	58		dB
SNR (Voice)	Signal-to-Noise Ratio of Voice Channel (Voice ADC path)	Signal = V_O at f = 1kHz and 1% THD+N, MIC_P, MIC_N terminated to ground, A-weighted, 36dB MIC Preamp gain setting[7]			
		f_{MCLK} = 12.288MHz, PLL disabled	83		dB
		f_{MCLK} = 12MHz, PLL active	81		dB
STR	Side Tone Range	Minimum	–30		dB
		Maximum	0		dB
SS	Side Tone Step Size		3		dB
Audio DAC (Typical numbers are with 6.144MHz audio clock and 48kHz sampling frequency)					
R_{DAC}	Audio DAC Ripple	20Hz – 20kHz through headphone output	+/- 0.1		dB
PB_{DAC}	Audio DAC Passband width	–3dB point	22.7		kHz
SBA_{DAC}	Audio DAC Stop band Attenuation	Above 24kHz	76		dB
DR_{DAC}	Audio DAC Dynamic Range	DC – 20kHz	97		dB
SNR_{DAC}	Audio DAC SNR Digital Filter Section	DC – 20kHz	97		dB
PLL					
f_{IN}	Input Frequency on MCLK pin		12	10 20	MHz (min) MHz (max)
SPI/I^2C					
f_{SPI}	Maximum SPI Frequency		400	4000	kHz (max)
$t_{SPISETD}$	SPI Data Setup Time			100	ns (min)
$t_{SPISETENB}$	SPI ENB Setup Time			100	ns (min)
$t_{SPISETHOLDD}$	SPI Data Hold Time			100	ns (min)
$t_{SPIHOLDENB}$	SPI ENB Hold Time			100	ns (min)
t_{SPICL}	SPI Clock Low Time			500	ns (min)
t_{SPICH}	SPI Clock High Time			500	ns (min)
t_{SPIT}	SPI Clock TransitionTime			5	ns (min)
t_{CLKI2C}	I^2C_CLK Frequency		400	3400	kHz (max)
$t_{I2CHOLD}$	I^2C_DATA Hold Time			100	ns (min)
t_{I2CSET}	I^2C_DATA Setup Time			100	ns (min)
PCM/I^2S					
f_{CLKPCM}	PCM_CLK Frequency		128		kHz
	PCM_CLK Duty Cycle		50	40 60	% (min) % (max)
f_{CLKI2S}	I^2S_CLK Frequency	I^2S_RES = 0 I^2S_RES = 1	1536 3072		kHz
	I^2S_WS Duty Cycle		50	40 60	% (min) % (max)

System Control

The LM4931 is controlled via either a three wire SPI or a two wire I^{2}C compatible interface, selectable with the MODE pin When MODE is cleared the device is in I^{2}C mode, when MODE is set the device is in SPI mode. This interface is used to configure the operating mode, interfaces, data converters, mixers and amplifiers. The LM4931 is controlled by writing 8 bit data into a series of write-only registers, the device is always a slave for both type of interfaces.

THREE WIRE, SPI INTERFACE (MODE = 1)

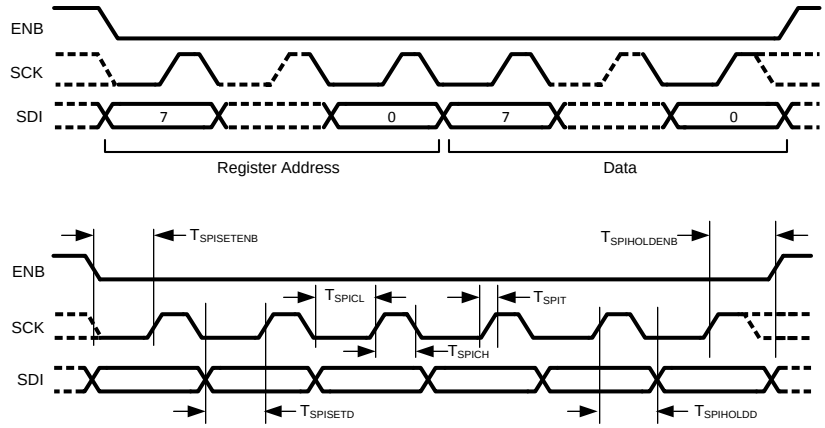


Figure 3.

When the part is configured as an SPI device and the enable (ENB) line is lowered the serial data on SDI is clocked in on the rising edge of the SCK line. The protocol used is 16bit, MSB first. The upper 8 bits (15:8) are used to select an address within the device, the lower 8 bits (7:0) contain the updated data for this register.

TWO WIRE I^{2}C COMPATIBLE INTERFACE (MODE = 0)

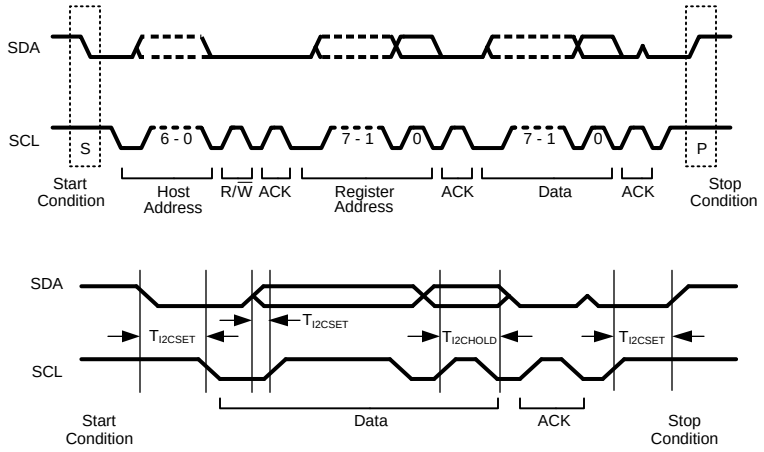


Figure 4.

When the part is configured as an I^{2}C device then the LM4931 will respond to one of two addresses, according to the ADDR input. If ADDR is low then the address portion of the I^{2}C transaction should be set to write to 0010000. When ADDR is high then the address input should be set to write to 1110000. The LM4931 uses the following 11 registers to store configuration information:

Table 1. SYSTEM CONTROL TABLE

Address	Register Name	Description
00000000	BASIC_CONFIG	Controls the output mode configuration
00000001	VOICE_CONFIG	Controls the settings for the voice codec
00000010	MIC_GAIN	Controls the gain and muting of the microphone pre-amplifier
00000011	HP_GAIN	Controls the gain and muting of the headphone amplifier
00000100	LS_GAIN	Controls the gain and muting of the loudspeaker amplifier
00000101	PLL_M	Sets the PLL input divider
00000110	PLL_N	Sets the PLL feedback divider
00000111	PLL_P	Sets the PLL output divider
00001000	CLK_MUX	Configures the clock divider
00001001	INTERFACES	Controls the format of the PCM, I^2S and GPIO interfaces
00001010	PMC_CONFIG	Controls the power management functions

Basic Configuration Register

This register used to configure the basic function of the chip.

Table 2. DEFAULT CHART FOR BASIC_CONFIG (00h)

DATA BIT	7	6	5	4	3	2	1	0
DEFAULT	0	0	0	0	0	0	0	0

Table 3. BASIC_CONFIG (00h) (SET = LOGIC 1, CLEAR = LOGIC 0)

Address	Register	Description				
3:0	MODE	The LM4931 can be placed in one of several modes that dictate the basic operation. When a new mode is selected the LM4931 will change operation silently and will reconfigure the power management profile automatically. The modes are described as follows(1):				
		3:0	**Mono Speaker Amplifier Source**	**Headphone Left Source**	**Headphone Right Source**	**Comment**
		0000	None	None	None	Powerdown mode
		0001	None	None	None	Standby mode
		0010	Voice	None	None	Mono speaker mode
		0011	None	Voice	Voice	Headphone call mode
		0100	Voice	Voice	Voice	Conference call mode
		0101	Audio (L+R)	None	None	L+R mixed to mono speaker
		0110	None	Audio (Left)	Audio (Right)	Headphone stereo audio
		0111	Audio (L+R)	Audio (Left)	Audio (Right)	L+R mixed to mono speaker + stereo headphone audio
		1000	Audio (Left)	Voice	Voice	Mixed mode
		1001	Voice + Audio (Left)	Voice	Voice	Mixed mode
		1010	Voice	Audio (Left)	Audio (Left)	Mixed mode

(1) Modes 8, 9, and 10 are only available if the sample rate of the I^2S is an integer multiple of the sample rate of the PCM. For example, 48kHz (I^2S) and 8kHz (PCM) would be acceptable.

Table 3. BASIC_CONFIG (00h) (SET = LOGIC 1, CLEAR = LOGIC 0) (continued)

4	SOFTRESET	If set, resets the LM4931, excluding the I^2C/SPI registers and PLL. SOFTRESET should be cleared to resume normal operation.
5	DAC_ DITHER_OFF	Disables the audio DAC dither.
6	BYPASS_BYPASS	If set the power management and control circuit will assume that bypass is at $V_{DD}/2$ even when such condition is false(2).
7	RSVD	RESERVED(3)

(2) It is recommended to alter this bit only while the part is in Powerdown mode.
(3) Reserved bits should be set to zero when programming the associated register.

Voice Codec Configuration Register

This register configures the voiceband codec, sidetone attenuation, and selected control functions.

Table 4. DEFAULT CHART FOR VOICE_CONFIG (01h)

DATA BIT	7	6	5	4	3	2	1	0
DEFAULT	0	0	0	0	0	0	0	0

Table 5. VOICE_CONFIG (01h) (SET = LOGIC 1, CLEAR = LOGIC 0)

Address	Register	Description			
3:0	SIDETONE_ATTEN	Programs the attenuation of the digital sidetone. Attenuation is set as follows:			
		3:0	**Sidetone Attenuation**	**3:0**	**Sidetone Attenuation**
		0000	Mute	**1000**	–9dB
		0001	–30dB	**1001**	–6dB
		0010	–27dB	**1010**	–3dB
		0011	–24dB	**1011**	0dB
		0100	–21dB	**1100**	0dB
		0101	–18dB	**1101**	0dB
		0110	–15dB	**1110**	0dB
		0111	–12dB	**1111**	0dB
4	AUTO_SIDE	This will automatically disable the sidetone when in a VOICE over loudspeaker mode except when the headphone is connected and the loudspeaker is muted by the HP_SENSE control.			
5	RSVD	RESERVED(1)			
6	VADC_DITHER_OFF	Disables the Voice ADC dither.			
7	VDAC_DITHER_OFF	Disables the Voice DAC dither.			

(1) Reserved bits should be set to zero when programming the associated register.

Microphone Gain Registers

This register is used to control the gain of the microphone preamplifier.

Table 6. DEFAULT CHART FOR MIC_GAIN (02h)

DATA BIT	7	6	5	4	3	2	1	0
DEFAULT	0	0	0	0	0	0	0	0

Table 7. MIC_GAIN (02h) (SET = LOGIC 1, CLEAR = LOGIC 0)

Address	Register	Description	
3:0	MIC_GAIN	Programs the gain of the microphone pre-amplifier. Gain is set as follows:	
		3:0	**Mic Gain**
		0000	6dB
		0001	8dB
		0010	10dB
		0011	12dB
		0100	14dB
		0101	16dB
		0110	18dB
		0111	20dB
		1000	22dB
		1001	24dB
		1010	26dB
		1011	28dB
		1100	30dB
		1101	32dB
		1110	34dB
		1111	36dB
4	MIC_MUTE	If set the microphone pre-amplifier and the ADC output are muted.	
5	RSVD	RESERVED(1)	
6	RSVD	RESERVED(1)	
7	HPF_DISABLE	If set the HPF is disabled, this is useful for wider bandwidth use of the ADC.	

(1) Reserved bits should be set to zero when programming the associated register.

Headphone Gain Registers

This register is used to control the gain of the headphone amplifier.

Table 8. DEFAULT CHART FOR HP_GAIN (03h)

DATA BIT	7	6	5	4	3	2	1	0
DEFAULT	0	0	0	0	0	0	0	0

Table 9. HP_GAIN (03h) (SET = LOGIC 1, CLEAR = LOGIC 0)

Address	Register	Description			
4:0	HP_GAIN	Programs the gain of the headphone amplifier. Gain is set as follows:			
		4:0	**Headphone Gain**	**4:0**	**Headphone Gain**
		00000	–46.5dB	**10000**	–22.5dB
		00001	–45dB	**10001**	–21dB
		00010	–43.5dB	**10010**	–19.5dB
		00011	–42dB	**10011**	–18dB
		00100	–40.5dB	**10100**	–16.5dB
		00101	–39dB	**10101**	–15dB
		00110	–37.5dB	**10110**	–13.5dB
		00111	–36dB	**10111**	–12dB
		01000	–34.5dB	**11000**	–10.5dB
		01001	–33dB	**11001**	–9dB
		01010	–31.5dB	**11010**	–7.5dB
		01011	–30dB	**11011**	–6dB
		01100	–28.5dB	**11100**	–4.5dB
		01101	–27dB	**11101**	–3dB
		01110	–25.5dB	**11110**	–1.5dB
		01111	–23dB	**11111**	0dB
5	HP_MUTE	If set the headphone amplifier is muted.			
6	HP_SENSE_TYPE	Defines if a high or low voltage at the HP_SENSE pin should indicate that a headphone is plugged in.			
		HP_SENSE_TYPE		**HP_SENSE_IN**	
		0		High = HP Plugged In	
		1		Low = HP Plugged In	
		The HP_SENSE_OUTPUT signal can be configured to appear on the GPIO pin.			
7	HP_SENSE_OUTPUT	If set, the polarity of the HP_CONNECTED output from the GPIO pin is reversed, so if the headphone is connected a 0 is reported on the GPIO rather than a 1. This does not alter the operation of the loudspeaker auto-muting function (as defined in Loudspeaker Gain Register)			

Loudspeaker Gain Register

This register configures the loudspeaker amplifier gain and muting conditions.

Table 10. DEFAULT CHART FOR LS_GAIN (04h)

DATA BIT	7	6	5	4	3	2	1	0
DEFAULT	0	0	0	0	0	0	0	0

Table 11. LS_GAIN (04h) (SET = LOGIC 1, CLEAR = LOGIC 0)

Address	Register	Description			
4:0	LS_GAIN	Programs the gain of the loudspeaker amplifier. Gain is set as follows:			
		4:0	**Loudspeaker Gain**	**4:0**	**Loudspeaker Gain**
		00000	–34.5dB	10000	–10.5dB
		00001	–33dB	10001	–9dB
		00010	–31.5dB	10010	–7.5dB
		00011	–30dB	10011	–6dB
		00100	–28.5dB	10100	–4.5dB
		00101	–27dB	10101	–3dB
		00110	–25.5dB	10110	–1.5dB
		00111	–24dB	10111	0dB
		01000	–22.5dB	11000	1.5dB
		01001	–21dB	11001	3dB
		01010	–19.5dB	11010	4.5dB
		01011	–18dB	11011	6dB
		01100	–16.5dB	11100	7.5dB
		01101	–15dB	11101	9dB
		01110	–13.5dB	11110	10.5dB
		01111	–12dB	11111	12dB
5	LS_MUTE	If set the loudspeaker amplifier is muted.			
6	LS_AUTO_MUTE	If set the loudspeaker amplifier is automatically muted when the headphone sense detects that the headphones have been connected. This uses the conditions set by HP_SENSE_TYPE to determine if the headphones are connected.			
7	LS_PWDN	If set the Class D amplifier is disabled. If an external amplifier is being used, an enable signal can be accessed on the GPIO.			

PLL Configuration Registers

This register is used to control the frequency divider (M divider) which sits before the PLL phase comparator, it also allows the 3 MSBs of the N_divider's modulus input to be programmed. See Figure 5 for further explanation.

Table 12. DEFAULT CHART FOR PLL_M (05h)

DATA BIT	7	6	5	4	3	2	1	0
DEFAULT	0	0	0	0	0	0	0	0

Table 13. PLL_M (05h) (SET = LOGIC 1, CLEAR = LOGIC 0)

Address	Register	Description
4:0	PLL_M	Programs the PLL input divider from divide by 4 to divide by 31. It is also possible to bypass the divider if PLL_M = 1 or divide by 2 if PLL_M = 2. Setting PLL_M = 3 will default to divide by 4.
7:5	PLL_N_MOD1	Programs the modulus bits [4:2] of the PLL feedback divider .

This register is used to control the integer of the PLL feedback divider (fractional N divider).

Table 14. DEFAULT CHART FOR PLL_N (06h)

DATA BIT	7	6	5	4	3	2	1	0
DEFAULT	0	0	0	0	0	0	0	0

Table 15. PLL_N (06n) (SET = LOGIC 1, CLEAR = LOGIC 0)

Address	Register	Description
6:0	PLL_N	Programs the PLL feedback divider from divide by 4 to divide by 127, PLL_N inputs from 0 to 3 are rounded to 4.
7	FAST_VCO	If set the VCO operates best at frequencies up to 100MHz, normally the VCO is tuned for outputs around 50MHz.

This register is used to control the PLL output divider (P divider), it also allows the 2 LSBs of the N divider's modulus input to be programmed.

Table 16. DEFAULT CHART FOR PLL_P (07h)

DATA BIT	7	6	5	4	3	2	1	0
DEFAULT	0	0	0	0	0	0	0	0

Table 17. PLL_P (07h) (SET = LOGIC 1, CLEAR = LOGIC 0)

Address	Register	Description	
3:0	PLL_P	Programs the PLL output divider from divide by 4 to divide by 15, PLL_P inputs from 0 to 3 are rounded to 4. It is recommended that P = 4 to keep the VCO around its nominal frequency of 50MHz.	
5:4	PLL_N_MOD2	Programs the PLL feedback divider modulus bits [1:0].	
7:6	DITHER_LEVEL	Programs the magnitude of the PLL dither level.	
		7:6	**PLL Dither Level**
		00	32
		01	16
		10	48
		11	0

The N divider is a fractional divider as such:

N = PLL_N + (PLL _NMOD/32)

If the Modulus input is zero then the N divider is simpler an integer N divider. The output from the PLL is determined by the following formula:

Fout = (Fin*N)/(PLL_M*PLL_P)

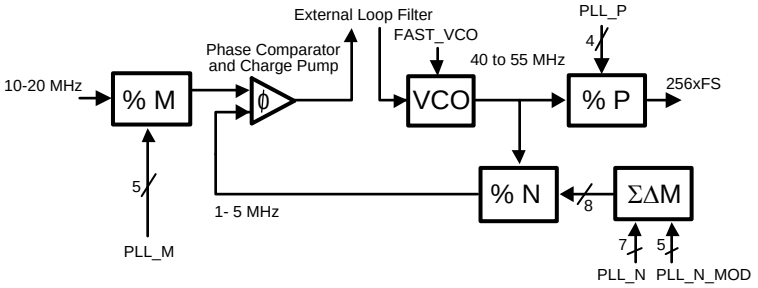


Figure 5.

Table 18. AUDIO CLOCK REQUIREMENTS

Input Clock	Sample Rate	Required Clock	M	N	N_MOD	P	Output Clock	Error (Hz)
12.000MHz	48kHz	12.288MHz	14	57	11	4	12.288MHz	0.2Hz
13.000MHz	48kHz	12.288MHz	4	15	4	4	12.288MHz	4.1Hz
14.400MHz	48kHz	12.288MHz	9	30	23	4	12.288MHz	1.9Hz

Table 18. AUDIO CLOCK REQUIREMENTS (continued)

Input Clock	Sample Rate	Required Clock	M	N	N_MOD	P	Output Clock	Error (Hz)
16.200MHz	48kHz	12.288MHz	11	33	12	4	12.288MHz	0.3Hz
16.800MHz	48kHz	12.288MHz	8	23	13	4	12.288MHz	1.1Hz
19.200MHz	48kHz	12.288MHz	13	33	9	4	12.288MHz	1.8Hz
19.440MHz	48kHz	12.288MHz	11	27	26	4	12.288MHz	0.3Hz
19.680MHz	48kHz	12.288MHz	13	32	15	4	12.288MHz	0.7Hz
19.800MHz	48kHz	12.288MHz	16	39	23	4	12.287MHz	0.1Hz
12.000MHz	44.1kHz	11.2896MHz	8	32	27	4	11.290MHz	1.7Hz
13.000MHz	44.1kHz	11.2896MHz	6	20	27	4	11.290MHz	2.9Hz
14.400MHz	44.1kHz	11.2896MHz	14	43	29	4	11.290MHz	2.3Hz
16.200MHz	44.1kHz	11.2896MHz	15	41	26	4	11.289MHz	0.9Hz
16.800MHz	44.1kHz	11.2896MHz	17	57	4	5	11.290MHz	1.6Hz
19.200MHz	44.1kHz	11.2896MHz	15	35	9	4	11.290MHz	0.8Hz
19.440MHz	44.1kHz	11.2896MHz	15	34	27	4	11.289MHz	1.6Hz
19.680MHz	44.1kHz	11.2896MHz	7	16	2	4	11.290MHz	0.2Hz
19.800MHz	44.1kHz	11.2896MHz	17	48	15	5	11.289MHz	3.0Hz
I^2S Inputs:								
1.536MHz	48kHz	12.288MHz	1	32	0	4	12.288MHz	0Hz
1.4112MHz	44.1kHz	11.2896MHz	1	32	0	4	11.2896MHz	0Hz
Other examples:								
19.44MHz	32kHz	8.192MHz	17	50	5	4	8.193MHz	6Hz
24.576MHz	44.1kHz	11.2896MHz	14	26	11	4	11.2868MHz	2.3Hz
66MHz	48kHz	12.288MHz	12	17	28	4	12.288MHz	4.1Hz
100MHz	48kHz	12.288MHz	24	23	19	4	12.288MHz	1.6Hz
100MHz	44.1kHz	11.2896MHz	31	28	0	4	11.2899MHz	2.8Hz

Please note that the Error (Hz) column is relative to sample rate. For instance:

If the Sample Rate is 48kHz and the input clock is 12.000MHz, then the solution shown in the table is:

Output Clock = 12.000MHz * (57 + 11/32) / (14 * 4) = 12.287946MHz. = 47.99979kHz * 256

Error = 48kHz – 47.99979kHz = 0.2Hz

Clock Divider Configuration Registers

This register is used to control the multiplexers in the clock module.

Table 19. DEFAULT CHART FOR CLK_MUX (08h)

DATA BIT	7	6	5	4	3	2	1	0
DEFAULT	0	0	0	0	0	0	0	0

Table 20. CLK_MUX (08h) (SET = LOGIC 1, CLEAR = LOGIC 0)

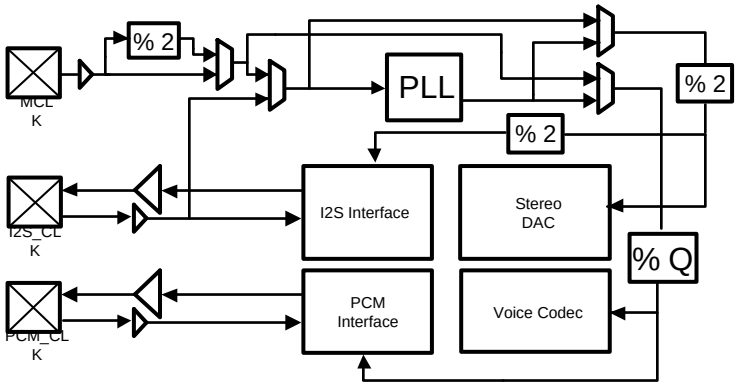
Address	Register	Description	
0	PLL_INPUT	Programs the PLL input multiplexer to select(1).	
		PLL_INPUT	**PLL Input Source**
		0	MCLK
		1	I^2S Input Clock

(1) It is recommended to alter this bit only while the part is in Powerdown mode.

Table 20. CLK_MUX (08h) (SET = LOGIC 1, CLEAR = LOGIC 0) (continued)

Address	Register	Description	
1	FAST_CLOCK	If set the master clock is divided by two, for example allowing for a 24.576MHz or PCI clock to be used(1)(2).	
		FAST_CLOCK	**MCLK Frequency**
		0	Normal
		1	Divided by 2
2	AUDIO_CLK_SEL	Selects which clock is passed to the audio sub-system(1):	
		AUDIO_CLK_SEL	**Audio Sub-system Input Source**
		0	PLL Output
		1	MCLK / MCLK/2
3	VOICE_CLK_SEL	Selects which clock is passed to the voice sub-system(1):	
		VOICE_CLK_SEL	**Audio Sub-system Input Source**
		0	PLL Output
		1	MCLK / MCLK/2
4	PLL_DISABLE	Powers down the PLL if it is not required.	
6:5	Q_DIV	Programs the Q divider (divides from the PLL output frequency of 12.288MHz).	
		6:5	**Divide Value**
		00	12 (1.024MHz/8kHz)
		01	8 (1.536MHz/12kHz)
		10	6 (2.048MHz/16kHz)
		11	4 (3.072MHz/24kHz)
7	RSVD	RESERVED(3)	

(2) For inputs greater than 50Mhz, the input clock divider FAST_CLOCK should be set.
(3) Reserved bits should be set to zero when programming the associated register.



The voice codec operates at 128*fs, so it requires a 1.024MHz clock to operate on 8kHz data. The Audio DAC also operates at 128*fs, i.e. 6.144MHz for 48kHz data, 5.6448MHz for 44.1kHz data etc. It is expected that the PLL is used to drive the audio system unless a 12.288MHz or 24.576MHz (AC'97) master clock is supplied and the sample rate is always 48kHz, in which case the PLL can be bypassed to reduce power.

The voice codec is always driven from the divided down clock from the PLL output or a divided down version of the master clock. When using the voice codec for 8kHz operation, program the PLL as you would for 48kHz operation and use Q to divide by (2*FSaudio/FSvoice).

The PLL can also use the I2S clock input as a source. In this case, the audio DAC uses the clock from the output of the PLL and the voice codec either uses a divided by 6 clock or a divided version of the MCLK pin.

MCLK must be less than or equal to 50MHz if the input divider is to be used, otherwise MCLK can be any frequency up to 25MHz. The comparison frequency after the M divider should be less than 5MHz

Digital Interface Configuration Registers

This register is used to control the format of the PCM, I2S, and GPIO interfaces.

Table 21. DEFAULT CHART FOR INTERFACES (09h)

DATA BIT	7	6	5	4	3	2	1	0
DEFAULT	0	0	0	0	0	0	0	0

Table 22. INTERFACES (09h) (SET = LOGIC 1, CLEAR = LOGIC 0)

Address	Register	Description	
0	PCM_COMPANDED	If set the data is assumed to be in either A-law or u-law 8-bit companded form, otherwise it is assumed to be up to 16 bits of MSB first linear 2's complement PCM format(1).	
1	PCM_ALAW_ULAW	If set the data is assumed to be A-law, otherwise it is u-law companded(1).	
2	PCM_MS	When set the PCM operates in a master mode.	
3	PCM_LONG	When set the PCM operates in long mode(1).	
4	I^2S_MS	When set the I^2S operates in a master mode.	
5	I^2S_RES	This selects if each word is 16 or 32 bits long(2):	
		I^2S_RES	**Word Length**
		0	16
		1	32
		In 32 bit mode the 18 MSBs are passed to the DAC. In 16 bit mode all 16 bits are passed to the DAC.	
6	RSVD	RESERVED(3)	
7	RSVD	RESERVED(3)	

(1) It is recommended to alter this bit only while the part is in Powerdown mode.
(2) Always operate the digital IO at the lowest frequency possible to save power and reduce noise. Obviously this can limit the resolution of the I^2S interface from 18 bits to 16 bits, but if only 16 bit data is available use the 16 bit mode to reduce I/O power.
(3) Reserved bits should be set to zero when programming the associated register.

Power Management Configuration Registers

This register is used to control the power management settings.

Table 23. DEFAULT CHART FOR PMC_CONFIG (0Ah)

DATA BIT	7	6	5	4	3	2	1	0
DEFAULT	0	0	0	0	0	0	0	0

Table 24. PMC_CONFIG (0Ah) (SET = LOGIC 1, CLEAR = LOGIC 0)

Address	Register	Description		
0	ZXD_DISABLE	If set then zero cross detection is ignored when changing modes or gains(1).		
2:1	CAP_SIZE	Set to accommodate a selected bypass capacitor value to give correct turn-on delay and click/pop performance. Value is set as follows(2):		
		2:1	**Delay**	**Capacitor Size/Time**
		00	short	0.1µF/25ms
		01	medium	1µF/100ms
		10	long	2.2µF/200ms
		11	test	Test Mode/1ms

(1) To ensure a successful transition into Powerdown Mode, ZXD_DISABLE must be set whenever there is no audio input signal present.
(2) The effect of CAP_SIZE will vary with the audio clock frequency. The delays quoted are for a 12.288MHz MCLK. These will scale inversely to the MCLK frequency. For example if used in a 44.1kHz application where the PLL output is 11.2896MHz, "01" or 100ms will be 100ms*11.2896/12.288 = 108.8ms. It is suggested that to save power earlier during the shutdown cycle, the PLL can be disabled and the MCLK or MCLK/2 can be used to bypass the PLL and also provide longer shutdown times for further reduced click and pop.

Table 24. PMC_CONFIG (0Ah) (SET = LOGIC 1, CLEAR = LOGIC 0) (continued)

Address	Register	Description	
5:3	GPIO_SETUP	Set the GPIO port function(3):	
		5:3	**GPIO**
		000	HP_CONNECTED
		001	VC_CLOCK
		010	GPIO_DATA
		011	EXT_LS_ENABLE
		100	VOICE_ADC_SD
		101	VOICE_DAC_SD
		110	DAC_LEFT_SD
		111	DAC_RIGHT_SD
6	RSVD	RESERVED(4)	
7	CLASS_D_DITHER	When set enables dither in the class D amplifier	

(3) VC_CLOCK is only supplied over the GPIO port if the voice codec is enabled.
(4) Reserved bits should be set to zero when programming the associated register.

Audio Interfaces

I²S

The LM4931 supports both master and slave I2S transmission at either 16 or 32 bits per word at clock rates up to 3.072MHz (48kHz stereo, 32bit). The basic format is shown below:

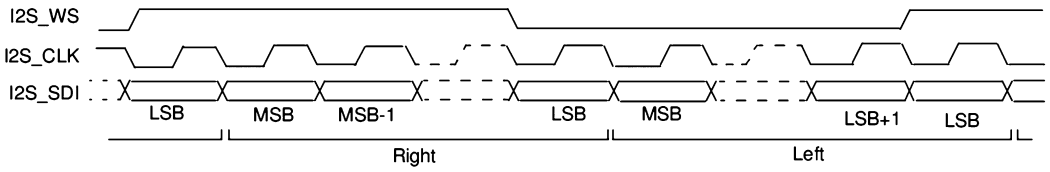


Figure 6.

PCM

The PCM interface is both master and slave and is compatible with National Semiconductor's AAI, Motorola's SSI, and Texas Instrument's McBSP audio codec interfaces. The protocol is short frame sync MSB first 2's complement 16 bit linear. The MSB always follows the sync pulse. In the case of companded data the first 8 bits are used and the interface can be slowed to 8 clock cycles per sync. In PCM_LONG mode the PCM_SYNC signal is inverted relative to that shown below.

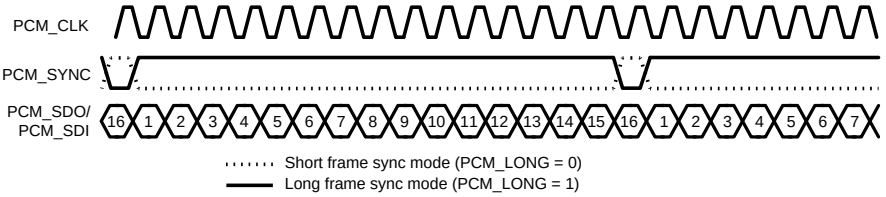


Figure 7.

Typical Performance Characteristics

MIC PreAmp + ADC Frequency Response (MIC Gain = 6dB)

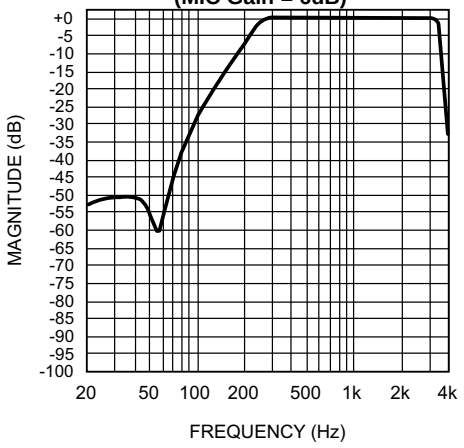


Figure 8.

MIC PreAmp + ADC Frequency Response Zoom (MIC Gain = 6dB)

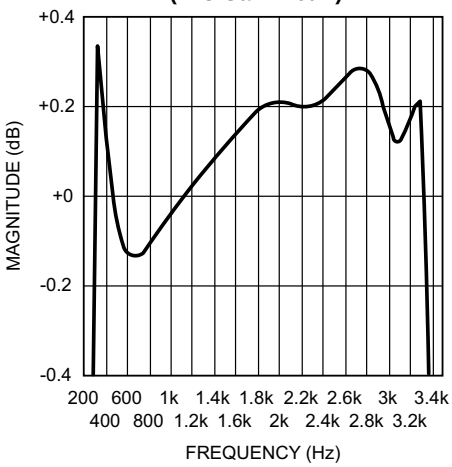


Figure 9.

MIC PreAmp + ADC Frequency Response (MIC Gain = 36dB)

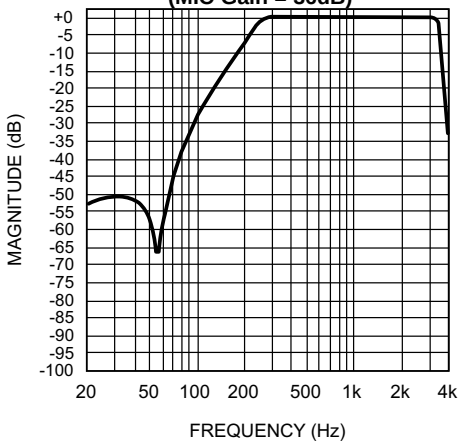


Figure 10.

MIC PreAmp + ADC Frequency Response Zoom (MIC Gain = 36dB)

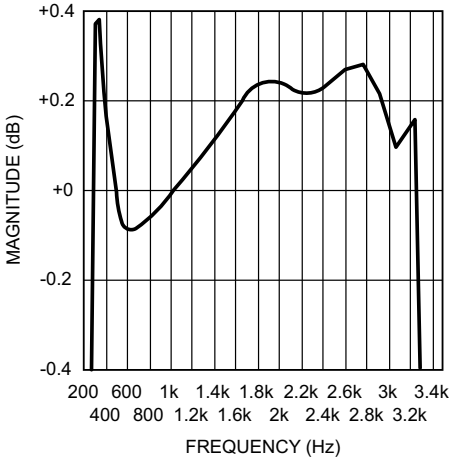


Figure 11.

MIC PreAmp + ADC Frequency Response High Cutoff (MIC Gain = 6dB)

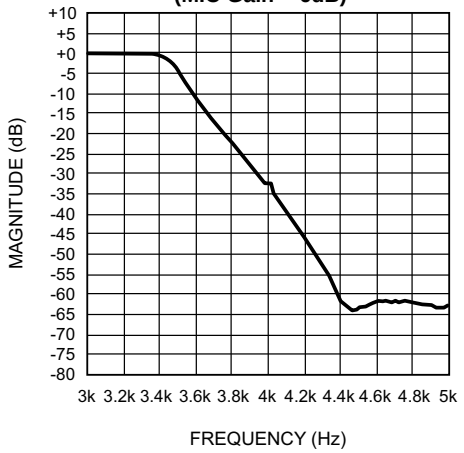


Figure 12.

MIC PreAmp + ADC Frequency Response High Cutoff (MIC Gain = 36dB)

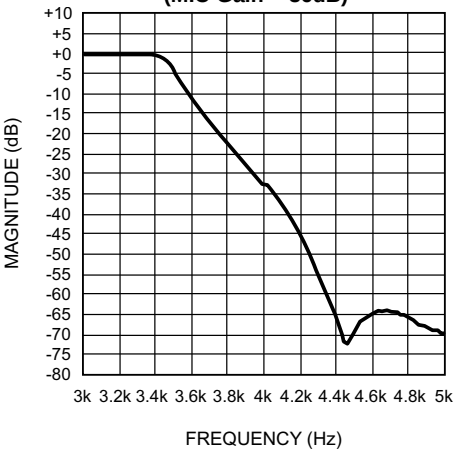


Figure 13.

Typical Performance Characteristics (continued)

MIC PreAmp + ADC Frequency Response Low Cutoff (MIC Gain = 6dB)

Figure 14.

MIC PreAmp + ADC Frequency Response Low Cutoff (MIC Gain = 36dB)

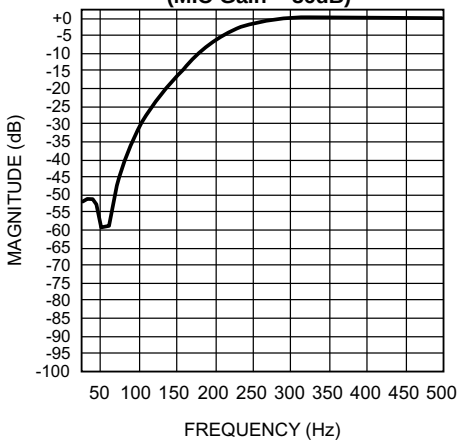


Figure 15.

ADC THD+N vs MIC Input Voltage (MIC Gain = 6dB), AV_{DD} = 5V

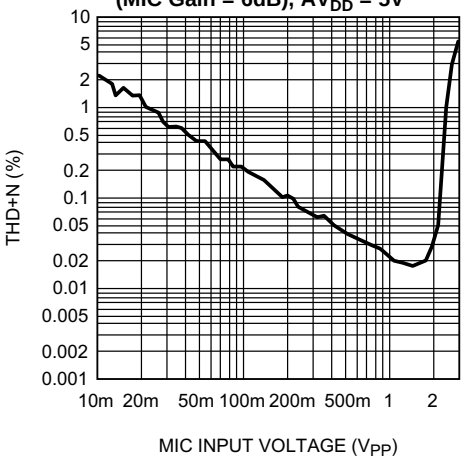


Figure 16.

ADC THD+N vs MIC Input Voltage (MIC Gain = 6dB), AV_{DD} = 3V

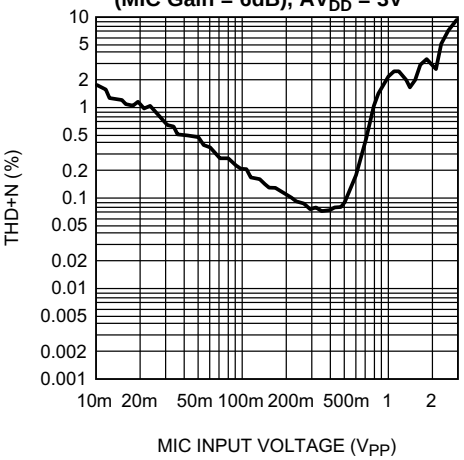


Figure 17.

ADC THD+N vs MIC Input Voltage (MIC Gain = 36dB, AV_{DD} = 5V)

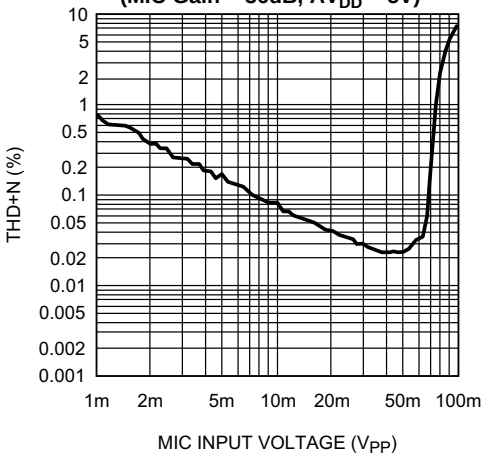


Figure 18.

ADC THD+N vs MIC Input Voltage (MIC Gain = 36dB, AV_{DD} = 3V)

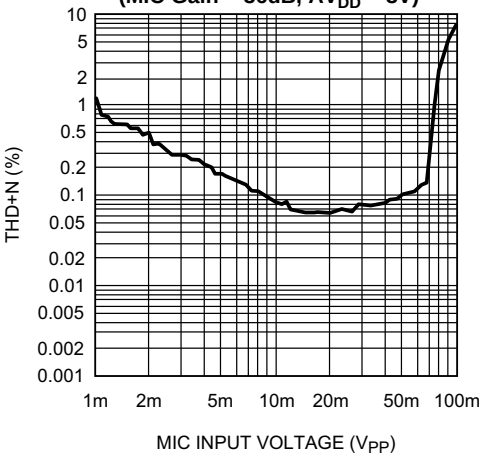


Figure 19.

Typical Performance Characteristics (continued)

MIC PreAmp + ADC PSRR vs Frequency
Top Trace = 36dB MIC Gain, Bottom Trace = 6dB MIC Gain, AV_{DD} = 5V

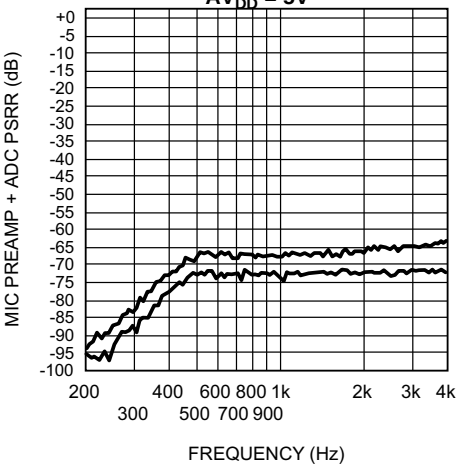


Figure 20.

MIC PreAmp + ADC PSRR vs Frequency
Top Trace = 36dB MIC Gain, Bottom Trace = 6dB MIC Gain, AV_{DD} = 3V

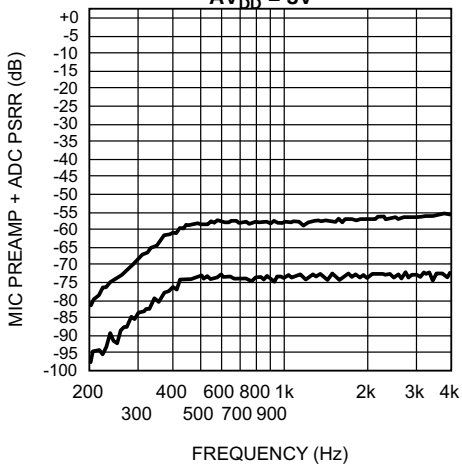


Figure 21.

Headphone Sense In Hysteresis Loop (AV_{DD} = 3V)

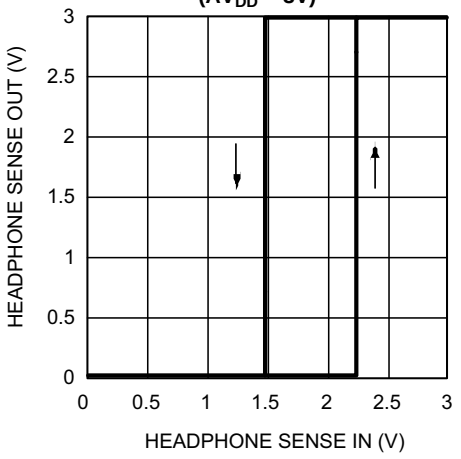


Figure 22.

Headphone Sense In Hysteresis Loop (AV_{DD} = 5V)

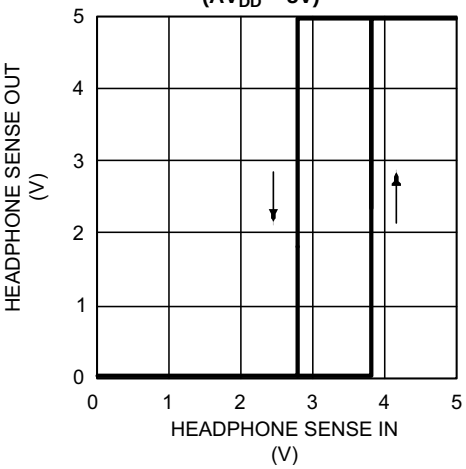


Figure 23.

I^2S DAC Frequency Response (Handsfree Output)

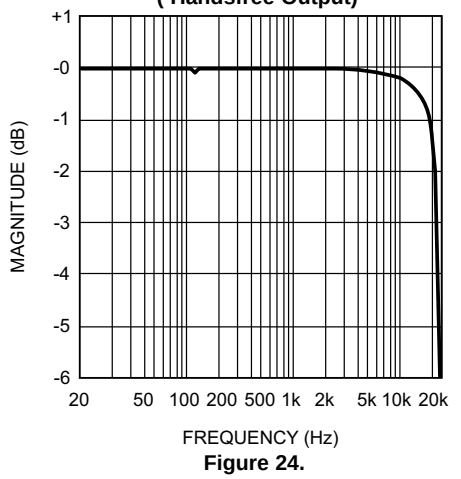


Figure 24.

I^2S DAC Frequency Response Zoom (Handsfree Output)

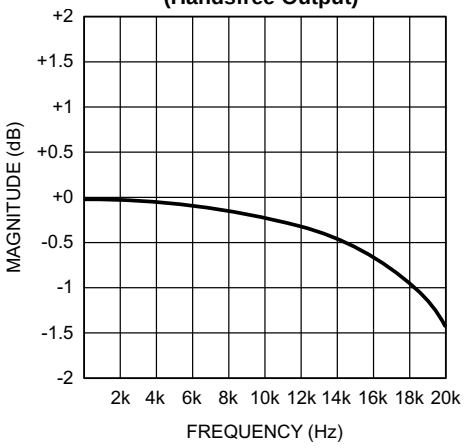


Figure 25.

Typical Performance Characteristics (continued)

I^2S DAC Frequency Response Zoom (Headphone Output)

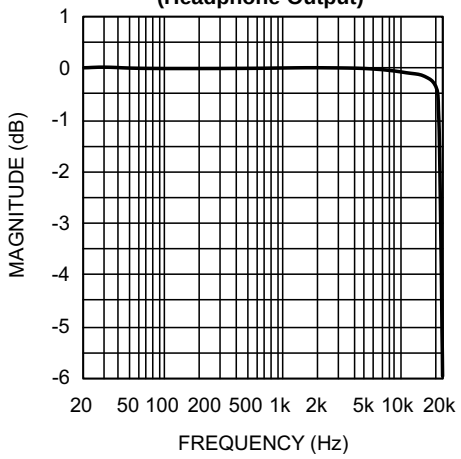


Figure 26.

I^2S DAC Frequency Response Zoom (Headphone Output)

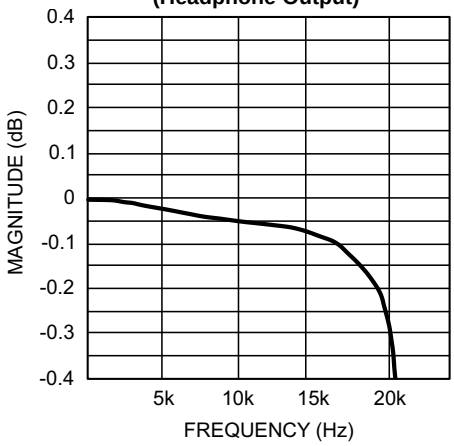


Figure 27.

THD+N vs I^2S Input Voltage (Handsfree Output, 0dB Handsfree Gain, AV_{DD} = 5V)

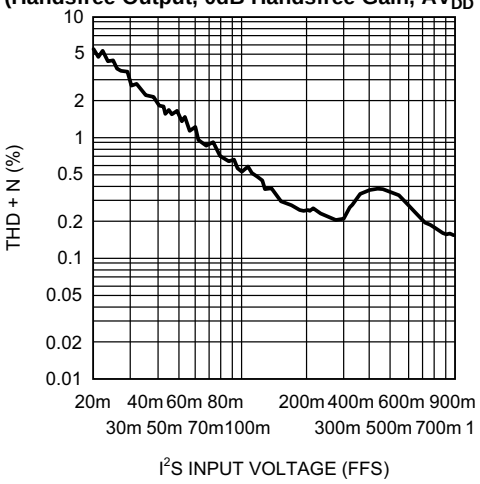


Figure 28.

THD+N vs I^2S Input Voltage (Handsfree Output, 0dB Handsfree Gain, AV_{DD} = 3V)

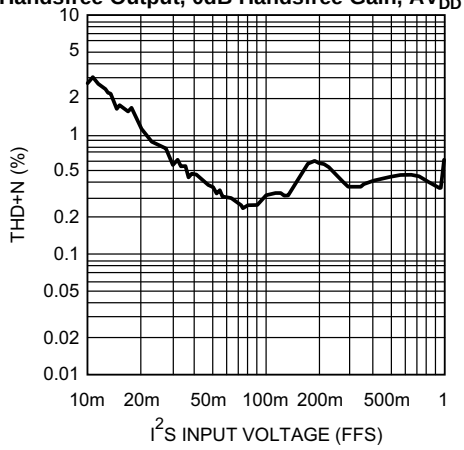


Figure 29.

THD+N vs I^2S Input Voltage (Headphone Output, 0dB Headphone Gain, AV_{DD} = 5V)

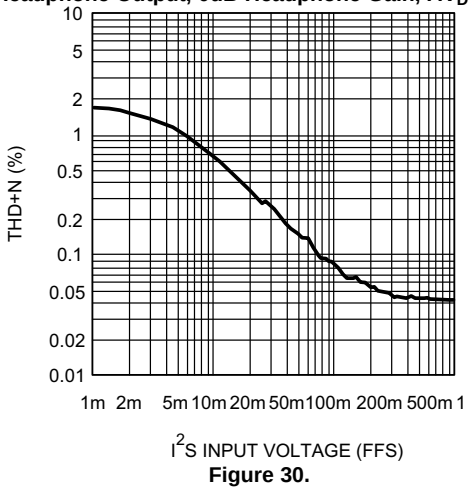


Figure 30.

THD+N vs I^2S Input Voltage (Headphone Output, 0dB Headphone Gain, AV_{DD} = 3V)

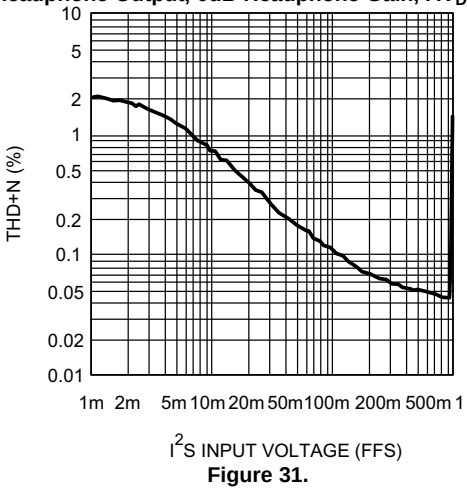


Figure 31.

Typical Performance Characteristics (continued)

I^2S DAC Crosstalk
(Top Trace = Left to Right, Bottom Trace = Right to Left)

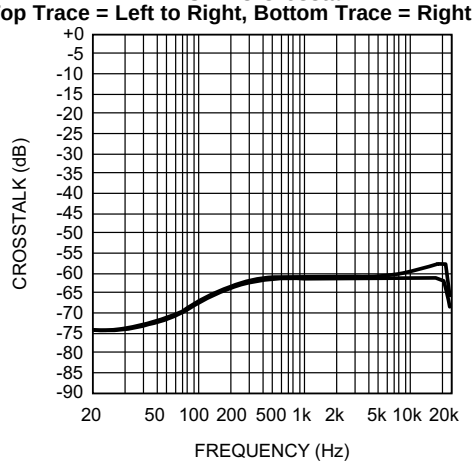


Figure 32.

MIC Bias Dropout Voltage vs MIC Bias Current

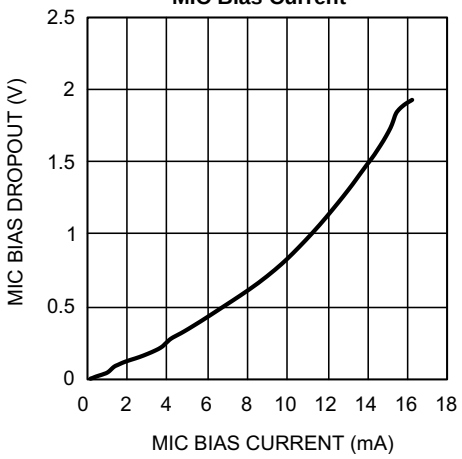


Figure 33.

PCM DAC Frequency Response (Handsfree Output)

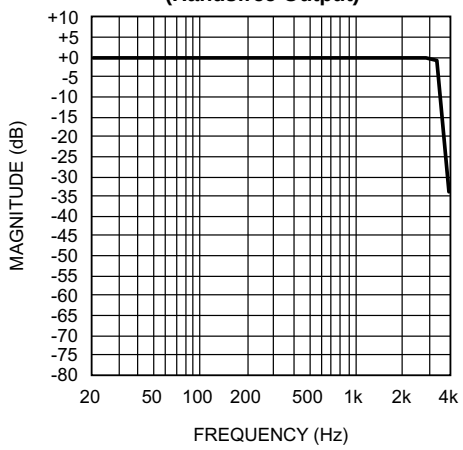


Figure 34.

PCM DAC Frequency Response Zoom (Handsfree Output)

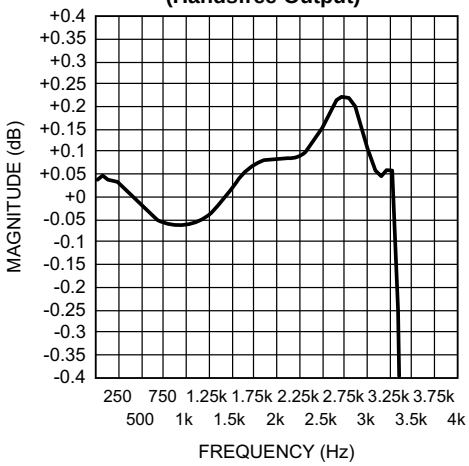


Figure 35.

PCM DAC Frequency Response (Headphone Output)

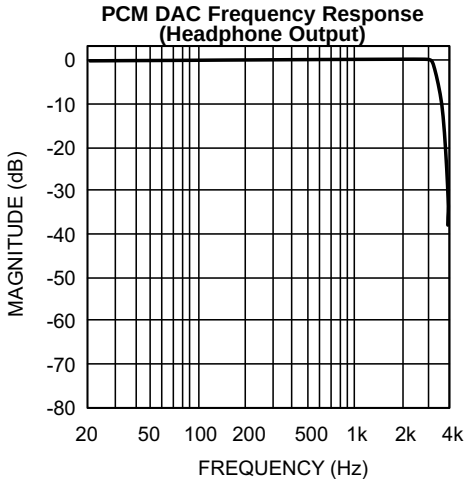


Figure 36.

PCM DAC Frequency Response Zoom (Headphone Output)

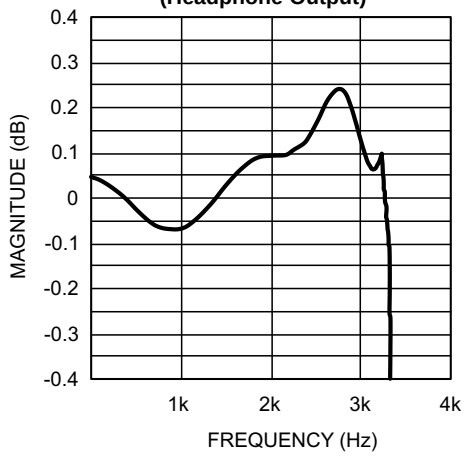


Figure 37.

Typical Performance Characteristics (continued)

THD+N vs PCM Input Voltage (Handsfree Output, 0dB Handsfree Gain, AV_{DD} = 5V)

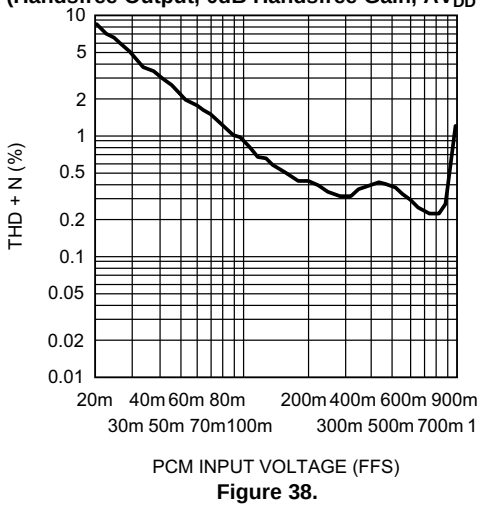


Figure 38.

THD+N vs PCM Input Voltage (Handsfree Output, 0dB Handsfree Gain, AV_{DD} = 3V)

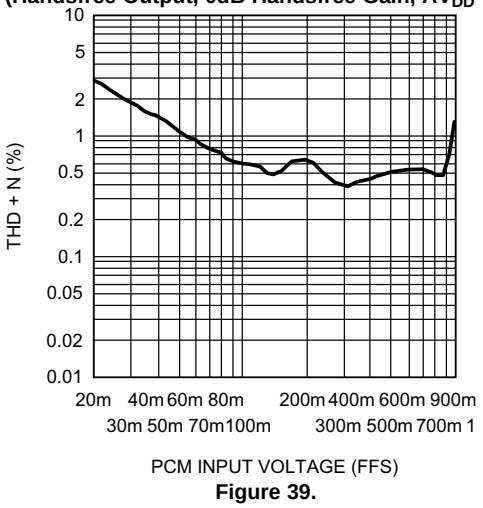


Figure 39.

THD+N vs PCM Input Voltage (Headphone Output, 0dB Headphone Gain, AV_{DD} = 5V)

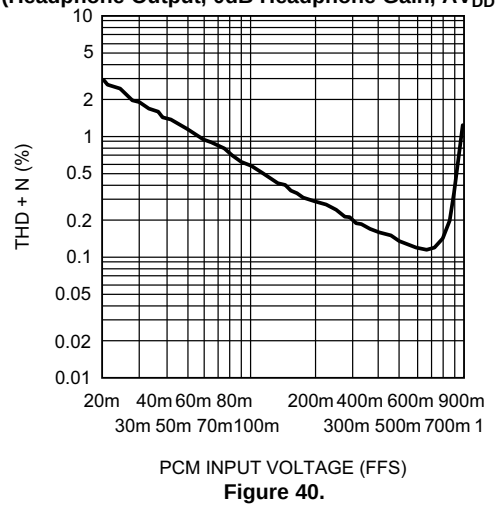


Figure 40.

THD+N vs PCM Input Voltage (Headphone Output, 0dB Headphone Gain, AV_{DD} = 3V)

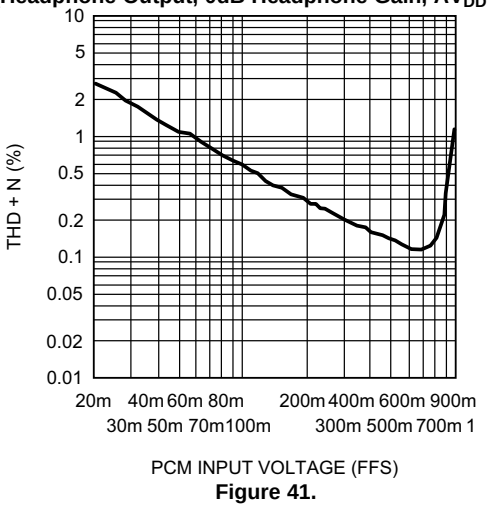


Figure 41.

PSRR vs Frequency (AV_{DD} = 5V, R_L = 32Ω, Headphone Output, Mode 6)

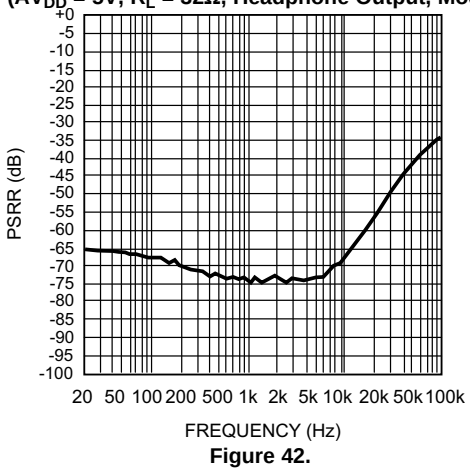


Figure 42.

PSRR vs Frequency (AV_{DD} = 3V, R_L = 32Ω, Headphone Output, Mode 6)

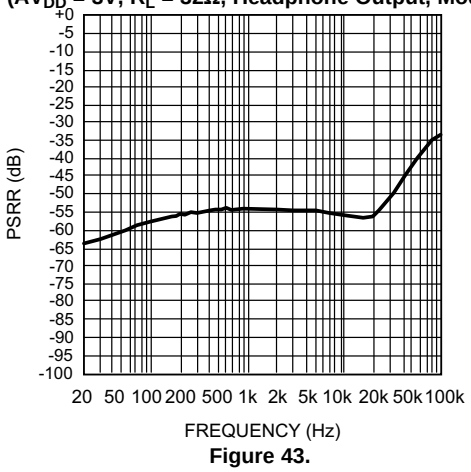


Figure 43.

Typical Performance Characteristics (continued)

PSRR vs Frequency
(AV_{DD} = 5V, R_L = 32Ω, Headphone Output, Mode 7)

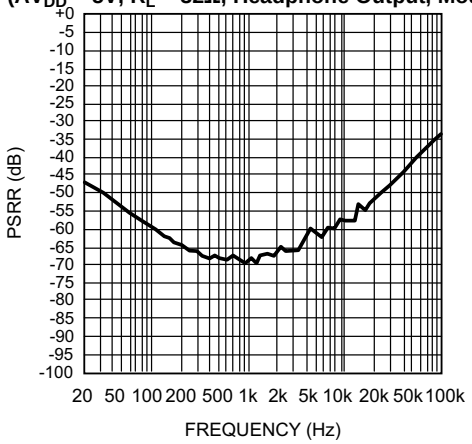


Figure 44.

PSRR vs Frequency
(AV_{DD} = 3V, R_L = 32Ω, Headphone Output, Mode 7)

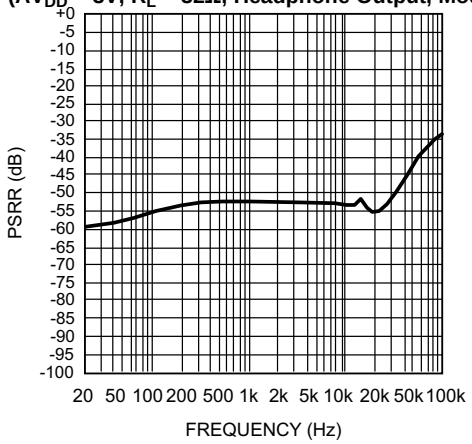


Figure 45.

PSRR vs Frequency
(AV_{DD} = 5V, R_L = 8Ω, Handsfree Output)

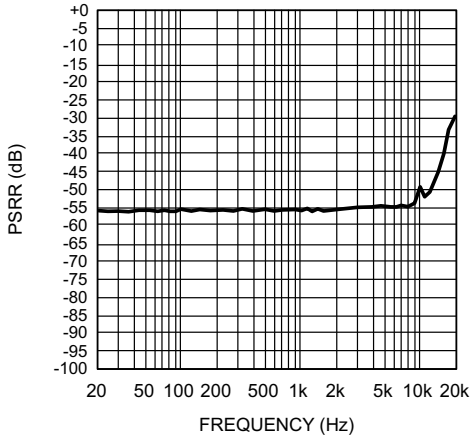


Figure 46.

PSRR vs Frequency
(AV_{DD} = 3V, R_L = 8Ω, Handsfree Output)

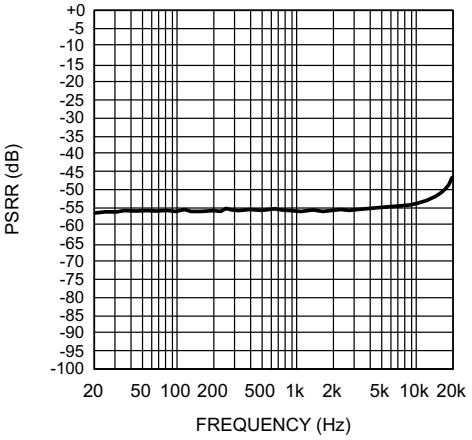


Figure 47.

THD+N vs Frequency
(AV_{DD} = 5V, R_L = 8Ω, P_O = 400mW, Handsfree Output)

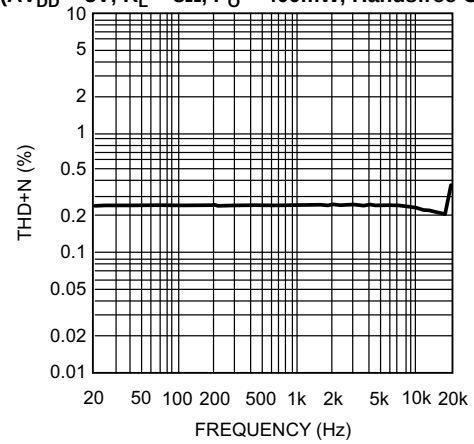


Figure 48.

THD+N vs Frequency
(AV_{DD} = 3V, R_L = 32Ω, P_O = 200mW, Handsfree Output)

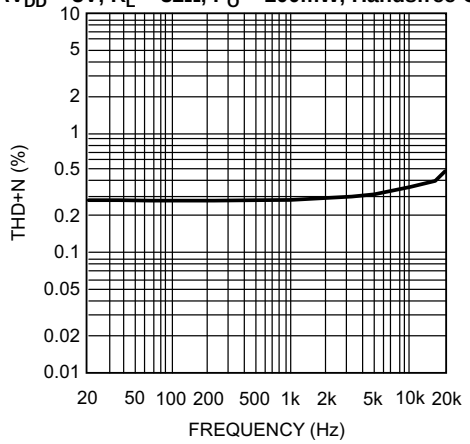


Figure 49.

Typical Performance Characteristics (continued)

THD+N vs Frequency
(AV_{DD} = 5V, R_L = 32Ω, P_O = 7.5mW, Headphone Output)

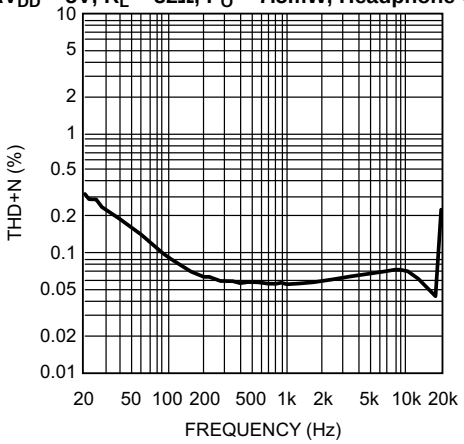


Figure 50.

THD+N vs Frequency
(AV_{DD} = 3V, R_L = 8Ω, P_O = 7.5mW, Headphone Output)

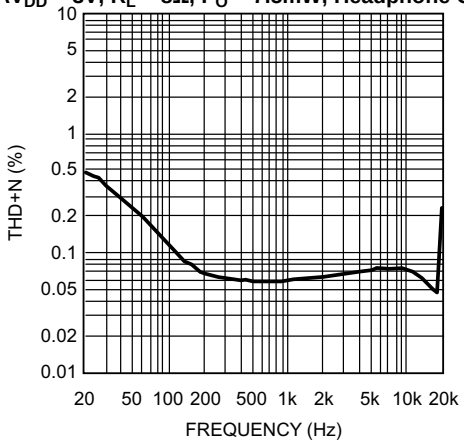


Figure 51.

THD+N vs Output Power
(AV_{DD} = 5V, R_L = 8Ω, f = 1kHz, Handsfree Output)

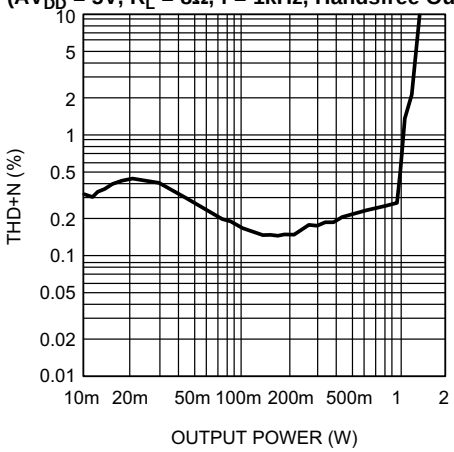


Figure 52.

THD+N vs Output Power
(AV_{DD} = 3V, R_L = 8Ω, f = 1kHz, Handsfree Output)

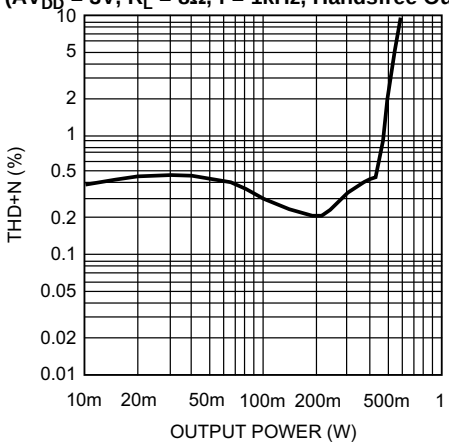


Figure 53.

THD+N vs Output Power
(AV_{DD} = 5V, R_L = 32Ω, f = 1kHz, Headphone Output)

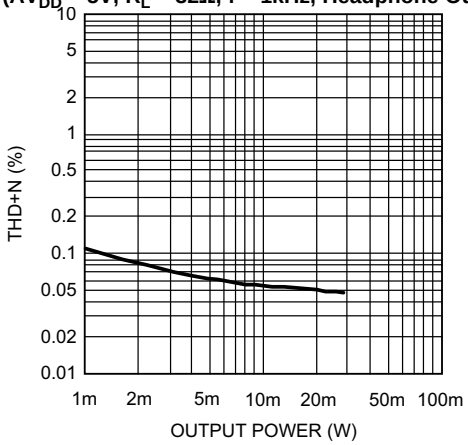


Figure 54.

THD+N vs Output Power
(AV_{DD} = 3V, R_L = 32Ω, f = 1kHz, Headphone Output)

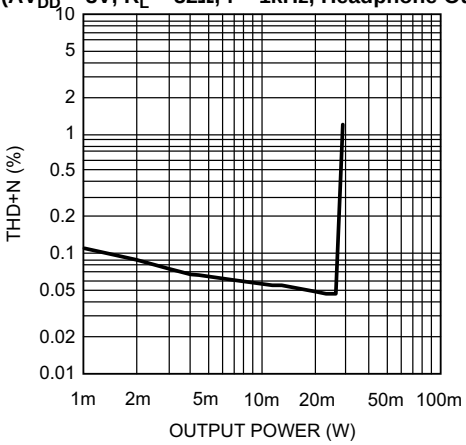


Figure 55.

Typical Performance Characteristics (continued)

THD+N vs Frequency
(AV_{DD} = 3.3V, R_L = 8Ω, P_O = 200mW, Handsfree Output)

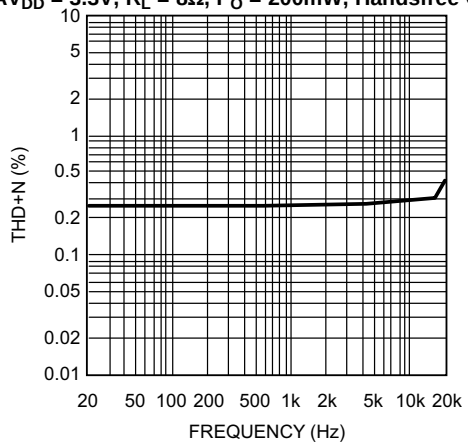


Figure 56.

THD+N vs Frequency
(AV_{DD} = 3.3V, R_L = 32Ω, P_O = 7.5mW, Headphone Output)

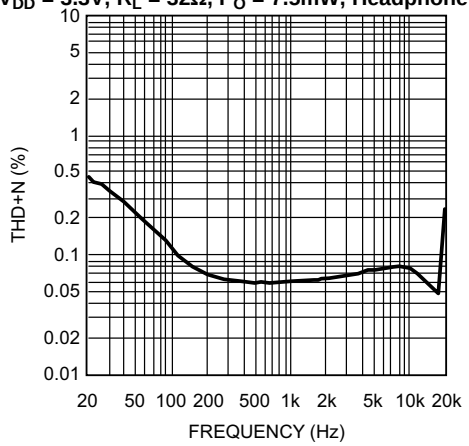


Figure 57.

THD+N vs Output Power
(AV_{DD} = 3.3V, R_L = 8Ω, f = 1kHz, Handsfree Output)

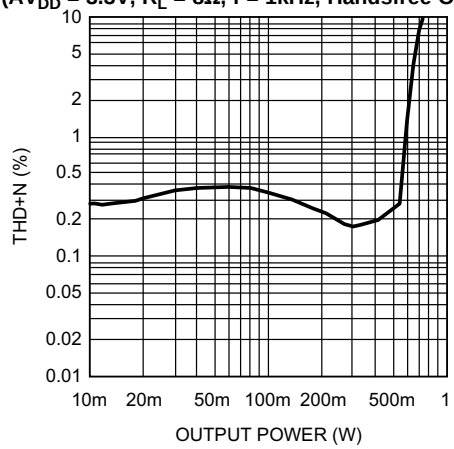


Figure 58.

THD+N vs Output Power
(AV_{DD} = 3.3V, R_L = 32Ω, f = 1kHz, Headphone Output)

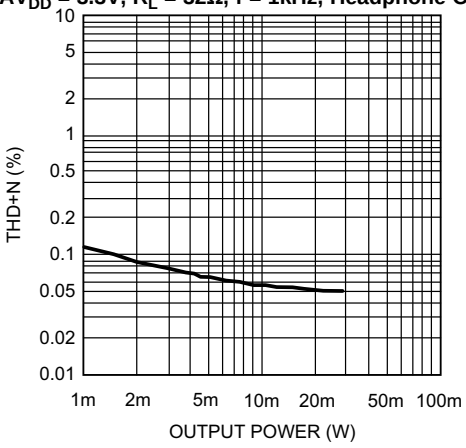


Figure 59.

APPLICATION INFORMATION

REFERENCE DESIGN BOARD AND LAYOUT

LM4931ITL Board Layout

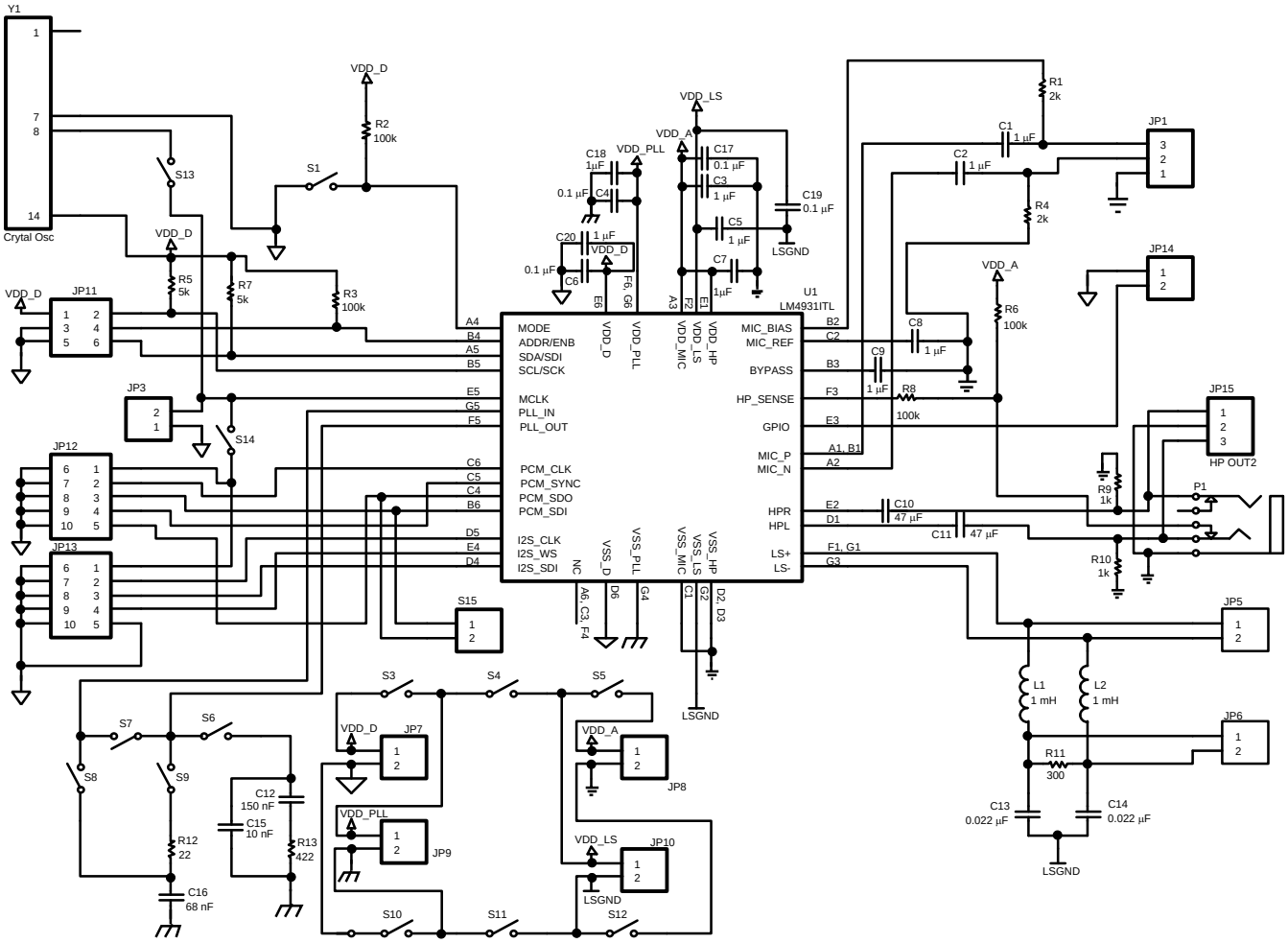


Figure 60. LM4931ITL Demo Board Schematic

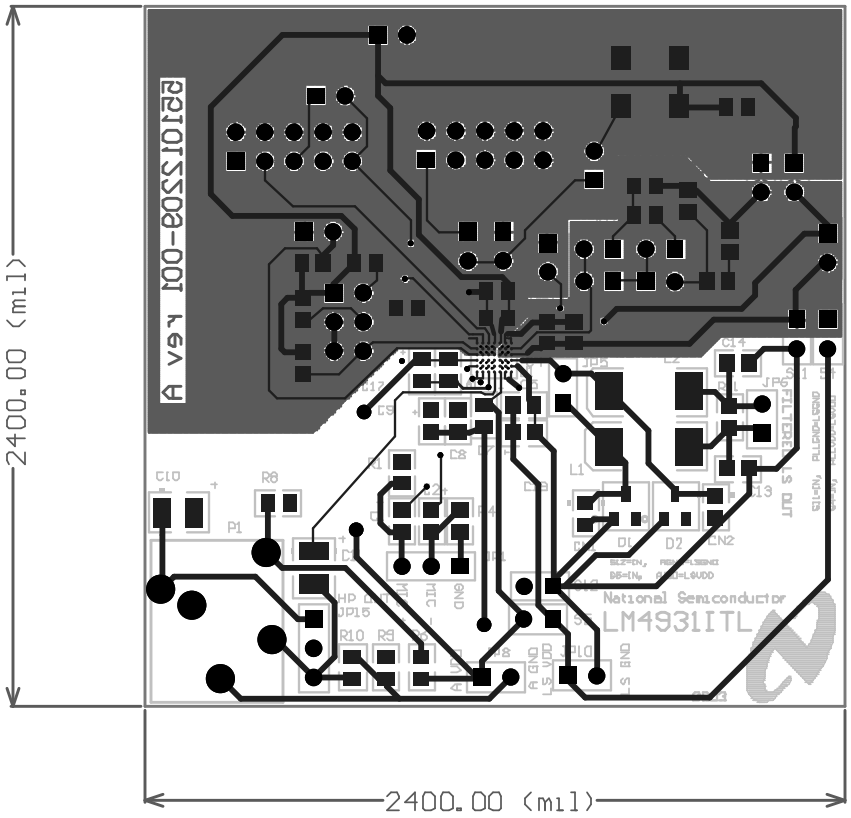


Figure 61. LM4931ITL Demo Board Composite View

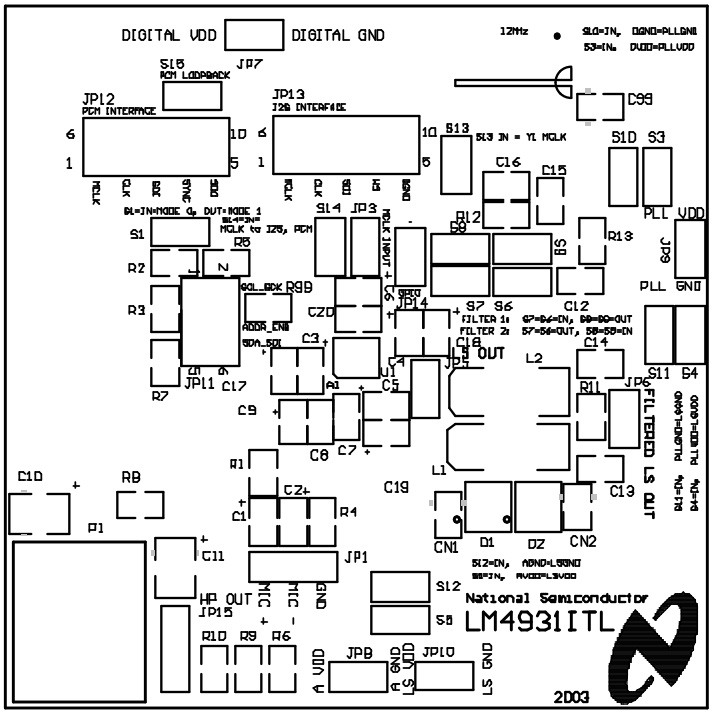


Figure 62. LM4931ITL Demo Board Silkscreen

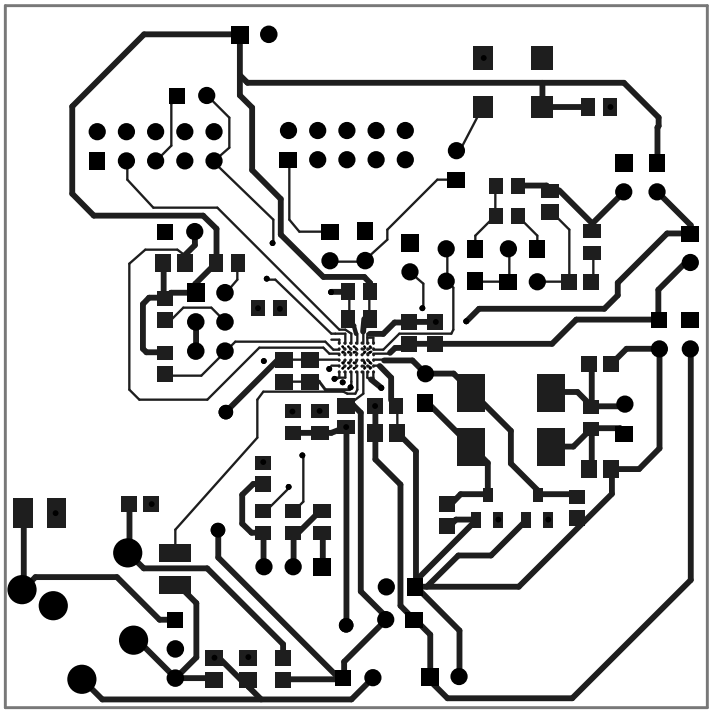


Figure 63. LM4931ITL Demo Board Top Layer

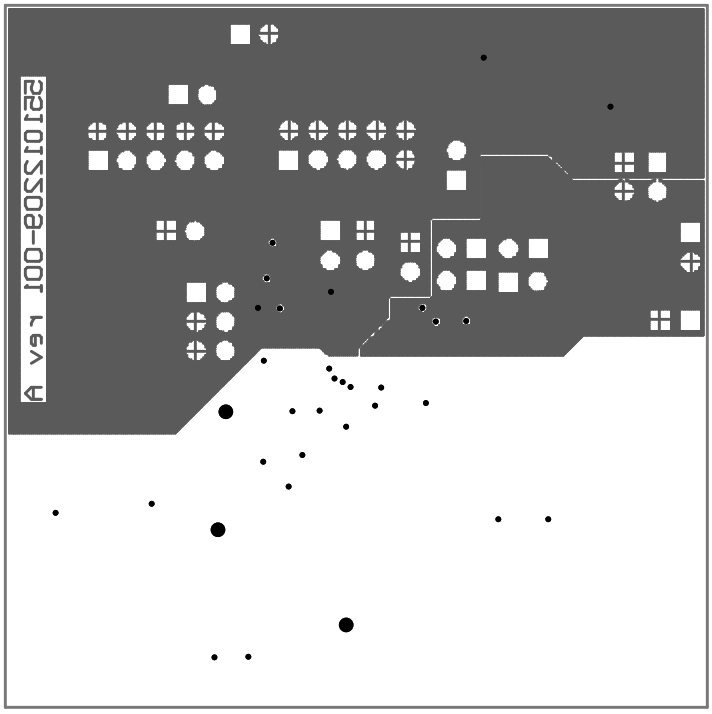


Figure 64. LM4931ITL Demo Board Bottom Layer

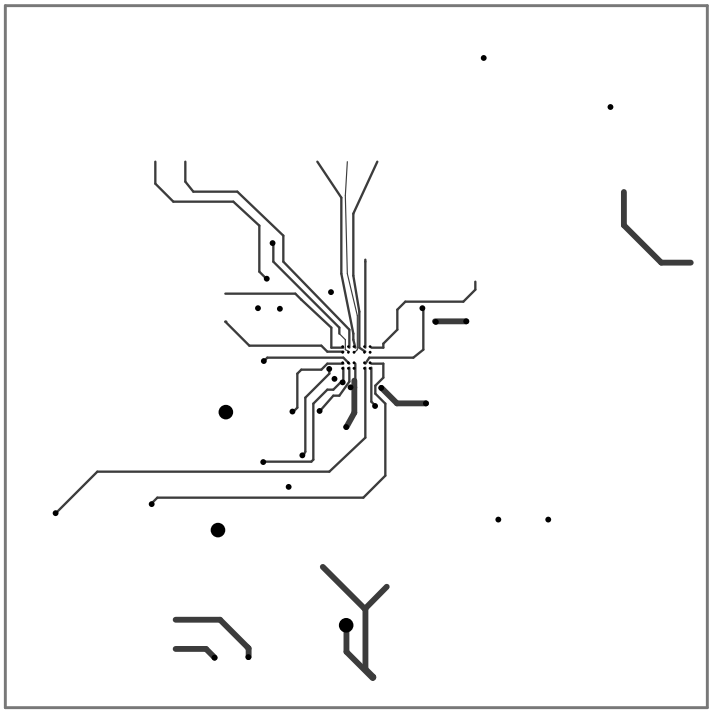


Figure 65. LM4931ITL Demo Board Inner Layer 1

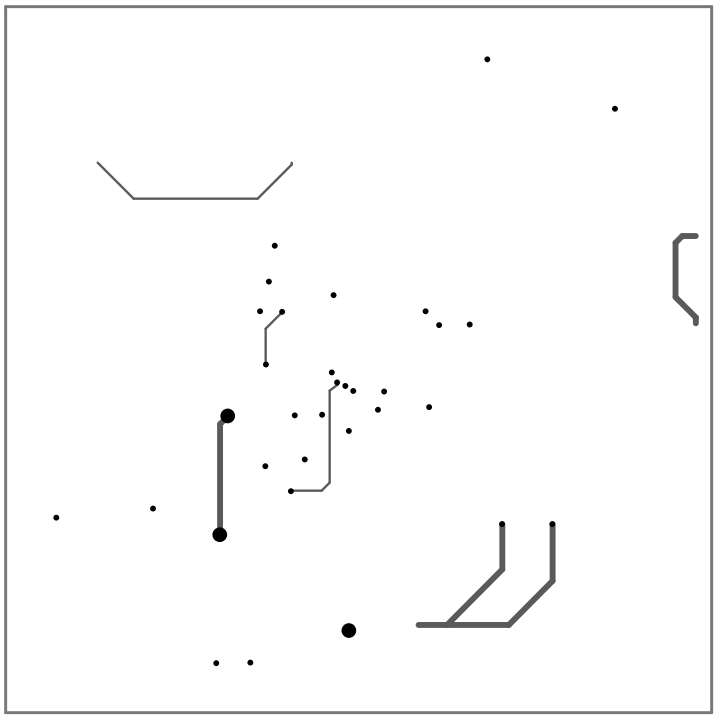


Figure 66. LM4931ITL Demo Board Inner Layer 2

Table 25. LM4931 DEMO BOARD BILL OF MATERIALS

Part Description	QTY	Reference Designator
Cer Cap 10nF 50V 10% 0805	1	C15
Cer Cap 150nF 50V 10% 0805	1	C12
Cer Cap 68pF 50V 10% 0805	1	C16
Cer Cap 0.022uF 50V 10% 0805	2	C13, C14
Cer Cap 0.1uF 50V 10% 0805	4	C4, C6, C17, C19
Tant Cap 1uF 16V 10% Case=A 3216	9	C1–C3, C5, C7–C9, C18, C20
Tant Cap 47uF 16V 10% Case=C 6032	2	C10–C11
Res 22.6 ohm 1/10W 1% 0805	1	R12
Res 300 ohm 1/10W 1% 0805	1	R11
Res 422 ohm 1/10W 1% 0805	1	R13
Res 1K Ohm 1/10W 1% 0805	2	R9, R10
Res 2K Ohm 1/10W 1% 0805	2	R1, R4
Res 5K Ohm 1/10W 1% 0805	4	R2, R6, R8, R99
Inductor 1mH	2	L1, L2
Stereo Headphone Jack	1	P1
Header 1 X 2	22	JP3, JP5–JP10, Jp14, S1, S3–S15
Header 1 X 3	4	
Header 1 X 5	4	

Table 26. I^2C/SPI CONTROL INTERFACE (JP11)

Pin	Function
1	VDD_D
2	SCL/SCK
3	VSS_D
4	ADDR/ENB
5	VSS_D
6	SDA/SDI

Table 27. PCM INTERFACE (JP12)

Pin	Function
1	MCLK
2	PCM_CLK
3	PCM_SDI
4	PCM_SYNC
5	PCM_SDO
6	VSS_D
7	VSS_D
8	VSS_D
9	VSS_D
10	VSS_D

Table 28. I^2S INTERFACE (JP13)

Pin	Function
1	MCLK
2	I2S_CLK
3	I2S_SDI
4	I2S_WS

Table 28. I²S INTERFACE (JP13) (continued)

5	VSS_D
6	VSS_D
7	VSS_D
8	VSS_D
9	VSS_D
10	VSS_D

Table 29. MIC JACK (JP1)

Pin	Function
1	VSS_HP
2	MIC_N
3	MIC_P

Table 30. EXTERNAL MASTER CLOCK INPUT MCLK/XTAL (JP3)

Pin	Function
1	VSS_D
2	MCLK

Table 31. DIGITAL SUPPLY VOLTAGE AND (JP7)

Pin	Function
1	VDD_D
2	VSS_D

Table 32. PLL SUPPLY VOLTAGE AND GND (JP9)

Pin	Function
1	VDD_PLL
2	VSS_PLL

Table 33. ANALOG SUPPLY VOLTAGE AND GND MIC AND HEADPHONE (JP8)

Pin	Function
1	VDD_A
2	VSS_A

Table 34. ANALOG SUPPLY VOLTAGE AND GND FOR LOUDSPEAKER (JP10)

Pin	Function
1	VDD_LS
2	VSS_LS

Table 35. ALTERNATE STEREO HEADPHONE OUTPUT (JP15)

Pin	Function
1	HPR
2	VSS_HP
3	HPL

Table 36. LOUDSPEAKER DIRECT OUTPUT (JP5)

Pin	Function
1	LS+
2	LS-

Table 37. LOUDSPEAKER FILTERED OUTPUT — FOR MEASUREMENT PURPOSES (JP6)

Pin	Function
1	Filtered LS+
2	Filtered LS-

Table 38. MULTI-USE PORT GPIO (JP14)

Pin	Function
1	VSS_D
2	GPIO

Table 39. PCM LOOPBACK JUMPER

Pin	Function
1	PCM_SDI
2	PCM_SDO

MODE Select Jumper (S1)

Jumper IN = LOW

Jumper OUT = HIGH

Crystal MCLK Jumper (S13)

Jumper IN = MCLK Supplied by on-board crystal oscillator

Jumper OUT = MCLK supplied by other source, crystal oscillator isolated

MCLK to PCM Bus and I^2S Bus Jumper (S14)

Jumper IN = MCLK connected to PCM bus and I^2S bus

Jumper OUT = MCLK isolated from PCM bus and I^2S bus

Table 40. PLL FILTER SELECT JUMPERS (S6–S9)

Jumper	IN/OUT	Function
S6 + S7	IN	2nd Order Filter Select
S8 + S9	OUT	
S6 + S7	OUT	3rd Order Filter Select
S8 + S9	IN	

Table 41. POWER SUPPLY JUMPERS (S3–S5, S10–S12)

Jumper	Function
S3	connects VDD_D and VDD_PLL
S4	connects VDD_PLL and VDD_LS
S5	connects VDD_A and VDD_LS
S10	connects VSS_D and VSS_PLL
S11	connects VSS_PLL and LSGND
S12	connects VSS_A and LSGND

LM4931ITL DEMO BOARD OPERATION

The LM4931ITL demo board is a complete evaluation platform, designed to give easy access to the control pins of the part and comprises all the necessary external passive components. Besides the separate analog (JP8), digital (JP7), PLL (JP9) and Loudspeaker (JP10) supply connectors, the board features seven other major input and control blocks: an SPI/I^2C compatible selectable interface bus (JP11) for the control lines, a PCM interface bus (JP12) for voiceband digital audio, an I^2S interface bus (JP13) for full-range digital audio, an analog mic jack input (JP1) for connection to an external microphone, a high efficiency class D BTL mono output (JP5) for connection to an external speaker, a stereo headphone output (JP15 or P1), and an external MCLK input (JP3) for use in place of the crystal on the demoboard.

SPI/I^2C Interface Bus (JP11)

This is the main control bus for the LM4931. This interface may either be configured as a two-wire, I^2C compatible interface by setting MODE = 0 (S1 = IN) or a three-wire SPI interface by setting MODE = 1 (S1 = OUT).

I^2C Compatible Mode (MODE = 0)

The two-wire I^2C compatible interface consists of an SDA line (data) and SCL line (clock). Each transmission from the baseband controller to the LM4931 is given MSB first and must follow the timing intervals given in the **Electrical Characteristics** section of the datasheet to create the start and stop conditions for a proper transmission. The start condition is detected if SCL is high on the falling edge of SDA. The stop condition is detected if SCL is high on the rising edge of SDA. Repeated start signals are handled correctly. Data is then transmitted as shown in Figure 4 for the **Two Wire I^2C Compatible Interface**. After the start condition has been achieved the chip address is sent, followed by a set write bit, wait for ack (SDA will be pulled low by LM4931), data bits 15-8, wait for ACK (SDA will be pulled low by LM4931), data bits 7-0, wait for ACK (SDA will be pulled low by LM4931) and finally the stop condition is given.

This same sequence follows for any I^2C control bus transmission to the LM4931. The chip address is hardwire selected by the ADDR Select pin (JP11, pin 4) which may be software enabled high or low with the LM4931 demonstration control software. If ADDR is low, then the chip address is set to 0010000b. If ADDR is high, the address is set to 1110000b. The 11 control registers are shown on page 13 in the **System Control Table**. Data is sampled only if the address is in range and the R/W bit is clear. Data for each register is given in the **System Control** section of the datasheet.

Pull-up resistors are required to achieve reliable operation. 10kΩ pull-up resistors on the SDA and SCL lines achieves best results when used with National's parallel-to-serial interface board. Lower value pull-up resistors will decrease the rise and fall times on the bus which will in turn decrease susceptibility to bus noise that may cause a false trigger. The cost comes at extra current use. Control bus reliability will thus depend largely on bus noise and may vary from design to design. Low noise is critical for reliable operation.

SPI Mode (MODE = 1)

The SPI interface consists of three lines: the serial data input pin (SDI), the clock input pin (SCK), and the SPI enable pin (ENB).The serial data bits are organized into two fields of 8 bit data as shown on Figure 3 in the **Three Wire, SPI Interface** timing diagram. The first 8 bits corresponds to the register address given on the **System Control Table** on page 13. The second 8 bits contains the data to write to the desired control register. These fields are transmitted subsequently to form a 16 bit word. For each SPI transfer, ENB is lowered and the data bits are written to the SDI pin with the most significant bit (MSB) first. All serial data are sampled at the rising edge of the SCK signal. Once all the data bits have been sampled, ENB transitions from logic-high to logic-low to complete the SPI sequence. All 16 bits must be received before any data latch can occur. Any excess CLK and DATA transitions will be ignored after the sixteenth rising clock edge has occurred. For any data sequence longer than 16 bits, only the first 16 bits will get loaded into the shift register and the rest of the bits will be disregarded.

SPI Operational Requirements

1. The data bits are transmitted with the MSB first.

2. The maximum clock rate is 4MHz for the SCK pin.

3. SCK must remain logic-high for at least 500ns (t_{SPICH}) after the rising edge of SCK, and SCK must remain logic-low for at least 500ns (t_{SPICL}) after the falling edge of SCK.

4. The serial data bits are sampled at the rising edge of SCK. Any transition on SDI must occur at least 100ns ($t_{SPISETHOLDD}$) before the rising edge of SCK. Also, any transition on SDI must occur at least 100ns ($t_{SPISETD}$) after the rising edge of SCK and stabilize before the next rising edge of SCK.

5. ENB should be logic-low only during serial data transmission.

6. ENB must be logic-low at least 100ns ($t_{SPISETENB}$) before the first rising edge of SCK, and ENB has to remain logic-low at least 100ns ($t_{SPIHOLDENB}$) after the sixteenth rising edge of SCK.

7. If ENB remains logic-high for mtore than 10ns before all 16 bits are transmitted then the data latch will be aborted.

8. If ENB is logic-low for more than 16 SCK pulses then only the first 16 data bits will be latched and activated when ENB transitions to logic-high.

9. ENB must remain logic-low for at least 100ns ($t_{SPIHOLDENB}$) to latch in the data.

10. Coincidental rising or falling edges of SCK and ENB are not allowed. If SCK is to be held logic-high after the data transmission, the falling edge of SCK must occur at least 100ns before ENB transitions to logic-low for the next set of data.

LM4931 Evaluation Software

The LM4931 demoboard can be easily evaluated with the accompanying **LM4931 Evaluation Software**. The Windows 95/98/2000/NT/XP compatible software is a GUI that allows easy access to all the I^2C/SPI internal registers of the device. The GUI controls the PC parallel port to deliver the appropriate I^2C/SPI commands via the National Semiconductor I^2C/SPI Interface Card, in order to properly program the LM4931.

PCM Bus Interface (JP12)

PCM_SDO, PCM_SYNC, PCM_SDI, and PCM_CLK form the PCM interface bus for simple communication with most baseband ICs with voiceband communications and follow the PCM-1900 communications standard. The PCM interface features a frame length of 16 bits, A-law and u-law companded, linear mode, short or long frame sync, an energy-saving power down mode, and master or slave operation. PCM_SYNC is the word sync line for the bus. It may be set in the **INTERFACES (09h)** register (bit 3 PCM_LONG) for short or long frame sync. A short frame sync is 1 PCM_CLK cycle (PCM_LONG=0), a long frame sync is an inverted version of short sync (PCM_LONG=1). This is illustrated by Figure 7 in the **PCM** timing diagram under the **Audio Interfaces** section. PCM_CLK is the bit clock for the bus. Its frequency is fixed at 128kHz and may be generated by the LM4931 when the PCM section is set to operate in master mode by setting bit 2 of the **INTERFACES (09h)** register. Clearing this same bit (bit 2) places the PCM section into slave mode where an external clock must be provided.

The other two lines, PCM_SDO and PCM_SDI, are for serial data out and serial data in, respectively. The type of data may also be set in the **INTERFACES (09h)** register by bits 0 and 1. Bit 0 controls whether the data is linear or companded. If set to 1, the 8 MSBs are presumed to be companded data and the 8 LSBs are ignored. If cleared to 0, the data is treated as 2's complement PCM data. Bit 1 controls which PCM law is used if Bit 0 is set for companded (G711) data. If set to 1, the companded data is assumed to be A-law. If cleared to 0, the companded data is treated as µ-law.

I^2S Interface Bus (JP13)

The I^2S standard provides a uni-directional serial interface designed specifically for digital audio. For the LM4931, the interface provides access to a 48kHz, 18 bit full-range stereo audio DAC. This interface uses a three port system of clock (I^2S_CLK), data (I^2S_SDI), and word (I^2S_WS). The clock and word lines can be either master or slave as set by bit 4 in the **INTERFACES (09h)** register.

A bit clock (I^2S_CLK) at 32 or 64 times the sample frequency is generated by the I^2S system master (unless set as a slave) and a word select (I^2S_WS) line is driven at a frequency equal to the sampling rate of the audio data, up to 48kHz. The word length is set by bit 5 of the **INTERFACES (09h)** register. When bit 5 is cleared, a word length of 16 bits is selected. When set, the word length is set to 32 bits. All 18MSBs are passed to the DAC when the I^2S interface is set to 32 bit word mode. In 16 bit mode, all 16 bits are sent to the DAC. The word line is registered to change on the negative edge of the bit clock. The serial data (I^2S_SDI) is sent MSB first, again registered on the negative edge of the bit clock, delayed by 1 bit clock cycle relative to the changing of the word line (see Figure 6).

MCLK/XTAL_IN (JP3)

This is the input for an external Master Clock. The jumper at S13 must be removed (disconnecting the onboard crystal from the circuit) when using an external Master Clock. Additionally, the jumper S14 may be used to connect the MCLK with the PCM and I^2S interface buses.

High-Efficiency Class D BTL Mono Out (JP5)

This is the high-efficiency mono speaker output, designed for use with an 8Ω speaker. The outputs are driven in bridge-tied-load (BTL) mode, so both sides have signal. Outputs are normally biased at one half AV_{DD} when the LM4931 is in active mode. The class D amplifier provides exceptional power use savings versus standard class AB amplifiers. A measurement output (JP6) is also provided, since the switching characteristics of an unfiltered Class D output often render conventional audio measurement techniques useless. This output band-limits the output to 20kHz, filtering out the switching noise for measurement purposes. This measurement output is not intended to provide power to a load.

Stereo Headphone Out (JP15 or P1)

This is the stereo headphone output. Each channel is single-ended, with 47uF DC blocking capacitors mounted on the demo board. The jack (P1) features a typical stereo headphone pinout. An alternate, pinned connection is also provided (JP15).

Headphone sense is incorporated into the jack on the demo board. In this application HP_SENSE is pulled low by the 1kΩ resistor when no headphone is present. This gives a corresponding logic low output on the HP_SENSE pin. When a headphone is placed in the jack the 1kΩ pull-down is disconnected and a 100kΩ pull-up resistor creates a high voltage condition on HP_SENSE. This information may be placed on the GPIO pin to reliably drive an external microcontroller with headphone status.

It is important to note that if using the alternate connection (JP15) for stereo headphone operation, HP sense is still tied to the mini-jack, requiring a physical plug to break the connection. HP sensing will then require a plug be placed in the jack (dummy plug).

MIC Jack (JP1)

This jack is for connection to an external microphone like the kind typically found in mobile phones. Pin 1 is GND, pin 2 is the negative input pin, and pin 3 is the positive pin, with phantom voltage supplied by MIC_BIAS on the LM4931.

GPIO (JP14)

This pin provides simple status updates from the LM4931 to an external microcontroller if desired. The GPIO output may be configured in the **PMC_CONFIG (0Ah)** register. Bits of the **PMC_CONFIG (0Ah)** register may be used to set the GPIO to output information regarding whether the headphone is connected, the voice-codec clock, an external LS enable signal, and shutdown status for the voiceband ADC, voiceband DAC, and the Left and Right channels of the full range-audio DAC. The voice-codec clock is only provided over the GPIO port if the voice codec is enabled. These outputs can be useful for simple software/driver development to monitor mode changes, or as a simple debugging tool.

BASIC OPERATION

The LM4931 is a highly integrated audio subsystem with many different operating modes available. These modes may be controlled in the **BASIC_CONFIG (00h)** register by bits 3:0. These mode settings are shown in the **BASIC_CONFIG (00h)** register table and are described here below:

Powerdown Mode (0000b)

Part is powered down, analog outputs are not biased. This is a minimum current mode. All part features are shut down.

Standby Mode (0001b)

The LM4931 is powered down, but outputs are still biased at one half AV_{DD}. This comes at some current cost, but provides a much faster turn-on time with zero "click and pop" transients on the headphone out. Standby mode can be toggled into and out of rapidly and is ideal for saving power whenever continuous audio is not a requirement. All other part functions are suspended.

Mono Speaker Mode (0010b)

Part is active. All analog outputs are biased. Audio from the voiceband codec is routed to the mono speaker out. Stereo headphone out is muted.

Headphone Call Mode (0011b)

Part is active. All analog outputs are biased. Audio from voiceband codec is routed to the stereo headphones. Both left and right channels are the same. Mono speaker out is muted.

Conference Call Mode (0100b)

Part is active. All analog outputs are biased. Audio from the voiceband codec is routed to the mono speaker out and to the stereo headphones.

L+R Mixed to Mono Speaker (0101b)

Part is active. All analog outputs are biased. Full-range audio from the 18bit/48kHz audio DAC is mixed together and routed to the mono speaker out. Stereo headphones are muted.

Headphone Stereo Audio (0110b)

Part is active. All analog outputs are biased. Full-range audio from the 18bit/48kHz audio DAC is sent to the stereo headphone jack. Each channel is heard discretely. The mono speaker is muted.

L+R Mixed to Mono Speaker + Stereo Headphone Audio (0111b)

Part is active. All analog outputs are biased. Full-range audio from the 18bit/48kHz audio DAC is sent discretely to the stereo headphone jack and also mixed together and sent to the mono speaker out.

Mixed Mode (1000b)

Part is active. All analog outputs are biased. This provides one channel (the left channel) of full range audio to the mono speaker out. Audio from the voiceband codec is then sent to the stereo headphones, the same on each channel.

Mixed Mode (1001b)

Part is active. All analog outputs are biased. Mixed voiceband and full-range audio (left channel only) is sent to the mono speaker out. Audio from the voiceband codec only is sent to the stereo headphones, the same on each channel.

Mixed Mode (1010b)

Part is active. All analog outputs are biased. Audio from the voiceband codec is sent to the mono speaker out. The left channel only of the full range audio is then sent to both the left and right channels of the stereo headphone out.

REGISTERS

The LM4931 starts on power-up with all registers cleared in Powerdown mode. Powerdown mode is the recommended time to make setup changes to the digital interfaces (PCM bus, I^2S bus). Although the configuration registers can be changed in any mode, changes made during Standby or Powerdown prevent unwanted audio artifacts that may occur during rapid mode changes with the outputs active. The LM4931 also features a soft reset. This reset is enabled by setting bit 4 of the **BASIC_CONFIG (00h)** register. DAC dither may also be controlled in this register (bit 5).

The **VOICE_CONFIG (01h)** register is used to set various configuration parameters on the voiceband and full-range audio codecs. SIDETONE_ATTEN (bits 3:0) refers to the level of signal from the MIC input that is fed back into the analog audio output path (commonly used in headphone applications and killed in hands-free applications). Setting the AUTOSIDE bit (bit 4) automatically mutes the sidetone in voice over mono speaker modes so feedback isn't an issue. Dither for the voice ADC and DAC may be disabled by setting bits 6 or 7, respectively. Bit 5 is reserved.

The **MIC_GAIN (02h)** register provides for microphone preamplifier gains of 6dB to 36dB in 2dB steps (bits 3:0). A quick mute bit is provided for the mic (bit 4) as well as a bit to disable the high-pass filter on the voice ADC, allowing wider bandwidth usage through the microphone input.

The **HP_GAIN (03h)** register provides settings for headphone control. Bits 4:0 set the gain of the headphone output from –46.5dB to 0dB in 1.5dB steps. A quick mute bit is also provided (bit 5). Additionally, the LM4931 may be configured to react to a high or low HP_SENSE voltage (bit 6) and may also provide this output on the GPIO pin in either positive or negative form (bit 7). This will only be seen on the GPIO output if it is configured to show HP_CONNECTED as described in the GPIO section.

The **LS_GAIN (04h)** register is used to set the mono class D loudspeaker gain. Bits 4:0 set this from –34.5dB to +12dB in 1.5dB steps. A quick mute (bit 5) is provided as well as an auto-mute bit (bit 6) that, if set, automatically mutes the loudspeaker when headphone sense detects that headphones have been connected. A powerdown bit (bit 7) is also provided to independently shutdown just the class D amplifier.

CLK_MUX (08h) is the clock divider register. Bit 0 sets the PLL input source. When clear, MCLK is used, when set, the I^2S input clock is used. Bit 1 gives a divide by 2 for usage with a faster MCLK (like 24.576MHz). Bit 2 selects which clock is passed to the full range audio subsystem. If clear, the PLL output is used. If set, MCLK (or MCLK/2 if set) is used directly. Bit 3 does the same for the voice codec subsystem. If clear, the PLL output is used. If set, MCLK or MCLK/2 is used. Bit 4 powers down the PLL (if not needed). Bits 6:5 program the Q divider, that can be further used to divide down the PLL output frequency. Bit 7 is reserved.

The **INTERFACES (09h)** register controls all the digital interface configurations. This may be used to set the PCM configuration and I^2S configuration as stated above in the PCM Bus Interface and **I^2S Bus Interface** sections. Bits 6 is reserved for test modes.

The **PMC_CONFIG (0Ah)** register controls various power management responsibilities including bypass capacitor size (bits 2:1). Zero crossing disable (bit 0) is also provided to allow the LM4931 to change modes regardless of zero crossing detect status. If set, the LM4931 will change modes immediately without waiting for the outputs to cross zero. Bits 6 is reserved.

PLL Registers

The PLL will accept incoming clock frequencies from 10MHz to 25MHz. However, since the control clocks, PCM clocks, and I^2S clocks all operate at fixed, defined frequencies the PLL must also be configured to match the incoming frequency and provide the correct output for all the parts of the subsystem.

The first register, **PLL_M (05h)**, sets the PLL input divider. Bits 4:0 of this register are used to set the divider from 4 to 31. It is also possible to bypass the divider (M =1) by setting PLL_M to 0001b. Setting PLL_M to 0010b gives a divide by 2. Setting PLL_M to 0011b gives a default divider of 4 (as does setting to 0100b). Values above that are identical to their base 10 integer values. Bits 7:5 programs the modulus bits of the PLL feedback divider.

The second PLL register, **PLL_N (06h)**, sets the PLL feedback divider. Bits 6:0 are used to set the PLL feedback divider from divide by 4 to divide by 127. Values set from 0 to 3 are rounded to 4. This register also may be used to alter the speed of the VCO. Setting bit 7 (FAST_VCO) tunes the VCO operation for frequencies up to 100MHz. Normally it is tuned for outputs around 50MHz.

The final PLL register, **PLL_P (07h)**, sets the PLL output divider. Bits 3:0 set this from divide by 4 to divide by 15. Inputs of 0 to 3 are rounded to 4. It is also recommended that P = 4 to keep the VCO around its nominal operating frequency (50MHz if PLL_N bit 7 is clear). The divider modulus may be set by bits 5:4. Additionally, the dither level for the PLL is controlled in this register in bits 7:6.

The **Audio Clock Requirements** table details how different clock values may be generated for a given input clock.

PLL Loop Filter

The LM4931 demoboard features an onboard second and third order PLL loop filter. Jumpers (S6-S9) configure the demoboard to select between the second and third order PLL loop filters. Reference values for the loop filters are given in the Table 25 section. For a more detailed discussion on how to optimize a second and third order PLL loop filter.

ANALOG INPUTS AND OUTPUTS

The LM4931 features a high-efficiency class D mono BTL output for connection to an 8Ω external speaker. This output can provide up to 1.1W of power into an 8 ohms load with a 5V analog supply. A single-ended stereo headphone output is also featured, providing up to 26mW of power per channel into 32Ω with a 5V analog supply. The MIC Jack input (JP1) provides for a low level analog input. Pin 3 provides the power to the MIC and the positive input of the LM4931. Gain for the MIC preamp is set in the **MIC_GAIN (02h)** register.

HIGH EFFICIENCY CLASS D AMPLIFIER FUNCTION

The class D mono output signals generated by the LM4931 consist of two, BTL connected, output signals that pulse momentarily from near ground potential to VDD. The two outputs can pulse independently with the exception that they both may never pulse simultaneously as this would result in zero volts across the BTL load. The minimum width of each pulse is approximately 160ns. However, pulses on the same output can occur sequentially, in which case they are concatenated and appear as a single wider pulse to achieve an effective 100% duty cycle. This results in maximum audio output power for a given supply voltage and load impedance. The LM4931 can achieve much higher efficiencies than class AB amplifiers while maintaining acceptable THD performance. The short (160ns) drive pulses emitted at the LM4931 outputs means that good efficiency can be obtained with minimal load inductance. The typical transducer load on an audio amplifier is quite reactive (inductive). For this reason, the load can act as it's own filter, so to speak. This "filter-less" switching amplifier/transducer load combination is much more attractive economically due to savings in board space and external component cost by eliminating the need for a filter.

CLASS D POWER DISSIPATION AND EFFICIENCY

In general terms, efficiency is considered to be the ratio of useful work output divided by the total energy required to produce it with the difference being the power dissipated, typically, in the IC. The key here is "useful" work. For audio systems, the energy delivered in the audible bands is considered useful including the distortion products of the input signal. Sub-sonic (DC) and super-sonic components (>22kHz) are not useful. The difference between the power flowing from the power supply and the audio band power being transduced is dissipated in the LM4931 and in the transducer load. The amount of power dissipation in the LM4931 is very low. This is because the ON resistance of the switches used to form the output waveforms is typically less than 0.25Ω. This leaves only the transducer load as a potential "sink" for the small excess of input power over audio band output power. The LM4931 dissipates only a fraction of the excess power requiring no additional PCB area or copper plane to act as a heat sink.

DUAL MICROPHONE SUPPORT

The LM4931 can be configured to accept two separate microphone inputs when used in conjunction with the LMS4684. The LMS4684 is a dual SPDT analog switch that will allow the MIC_P and MIC_N inputs of the LM4931 to switch between a differential handset microphone and a single-ended handsfree microphone. The MIC DETECT block shown in Figure 67 can be implemented with a microphone jack's mechanical control pin to set the voltage at the IN1 and IN2 pins of the LMS4684. The voltage applied at the IN1 and IN2 pins sets the position of the switch. For a more detailed discussion on the operation of the analog switch, please refer to the LMS4684 datasheet.

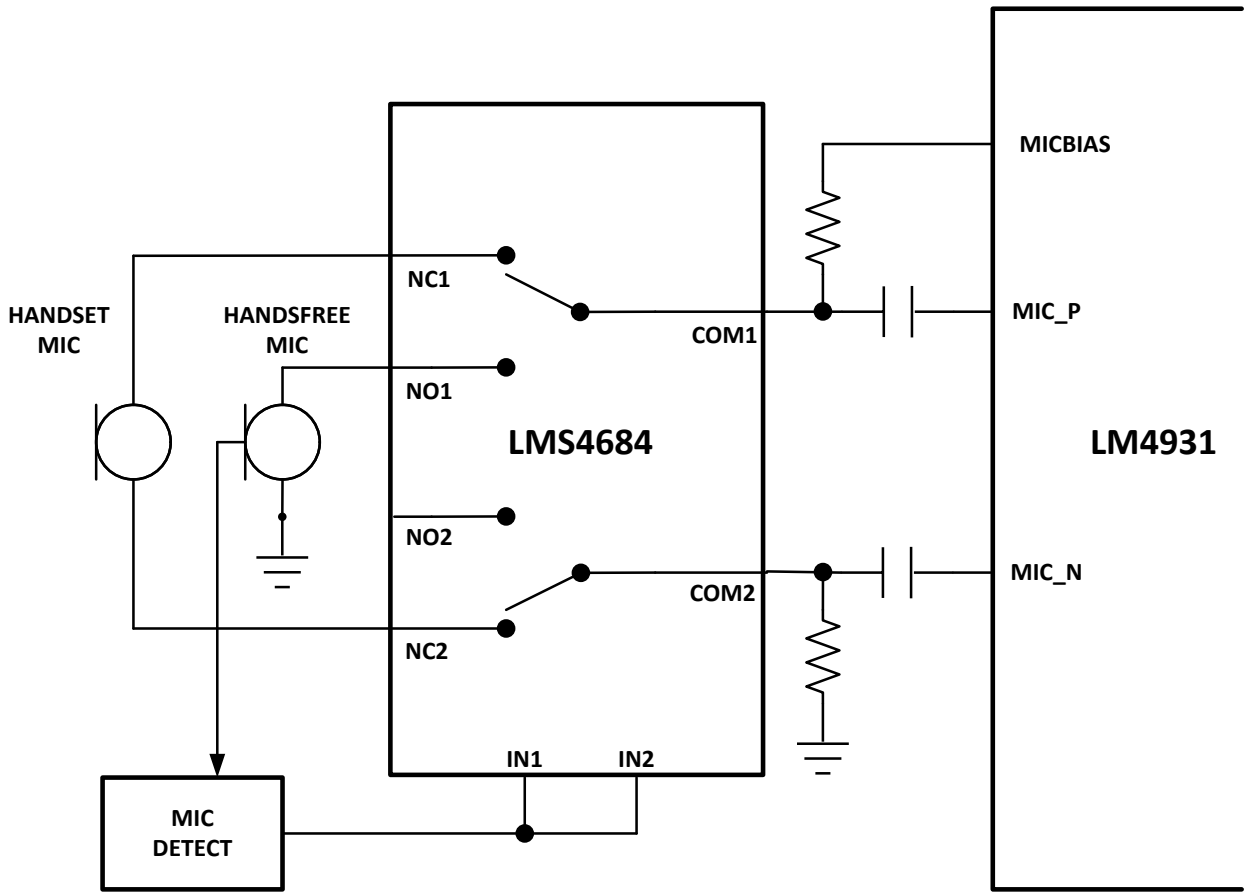


Figure 67. Dual Microphone Setup

Revision History

Rev	Date	Description
1.0	6/30/04	Re-webd.
1.1	7/24/06	Input a couple of text edits on table (LS-GAIN 04h).... per Alvin Fok, then re-released D/S to the WEB.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
LM4931ITL/NOPB	ACTIVE	DSBGA	YZR	42	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	GC9	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

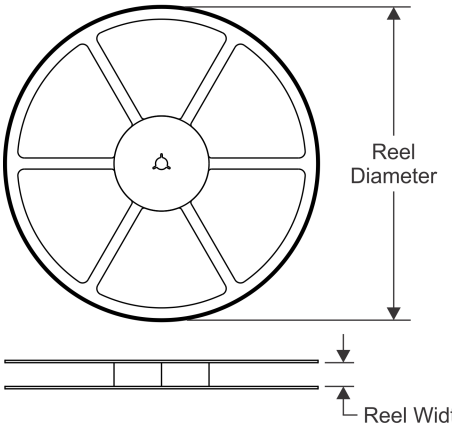
(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

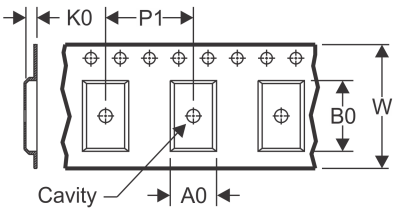
(4) Only one of markings shown within the brackets will appear on the physical device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

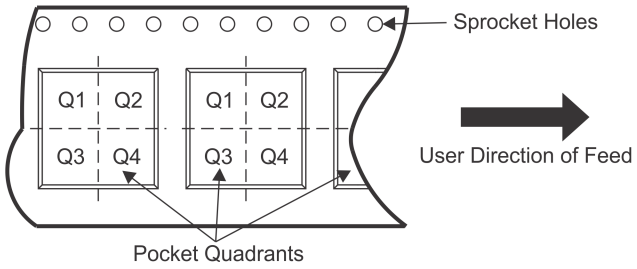


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

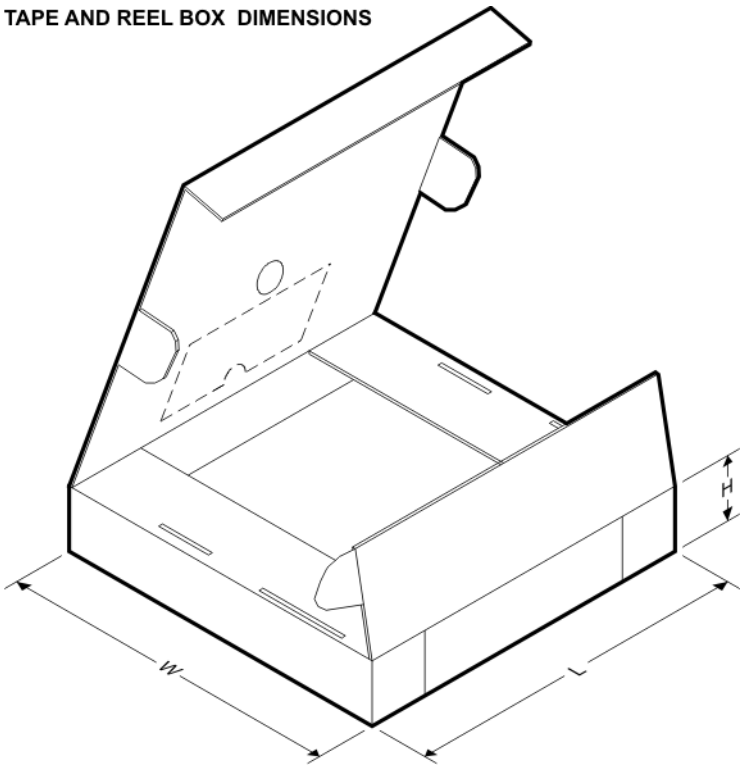
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM4931ITL/NOPB	DSBGA	YZR	42	250	178.0	12.4	3.71	4.12	0.76	8.0	12.0	Q1

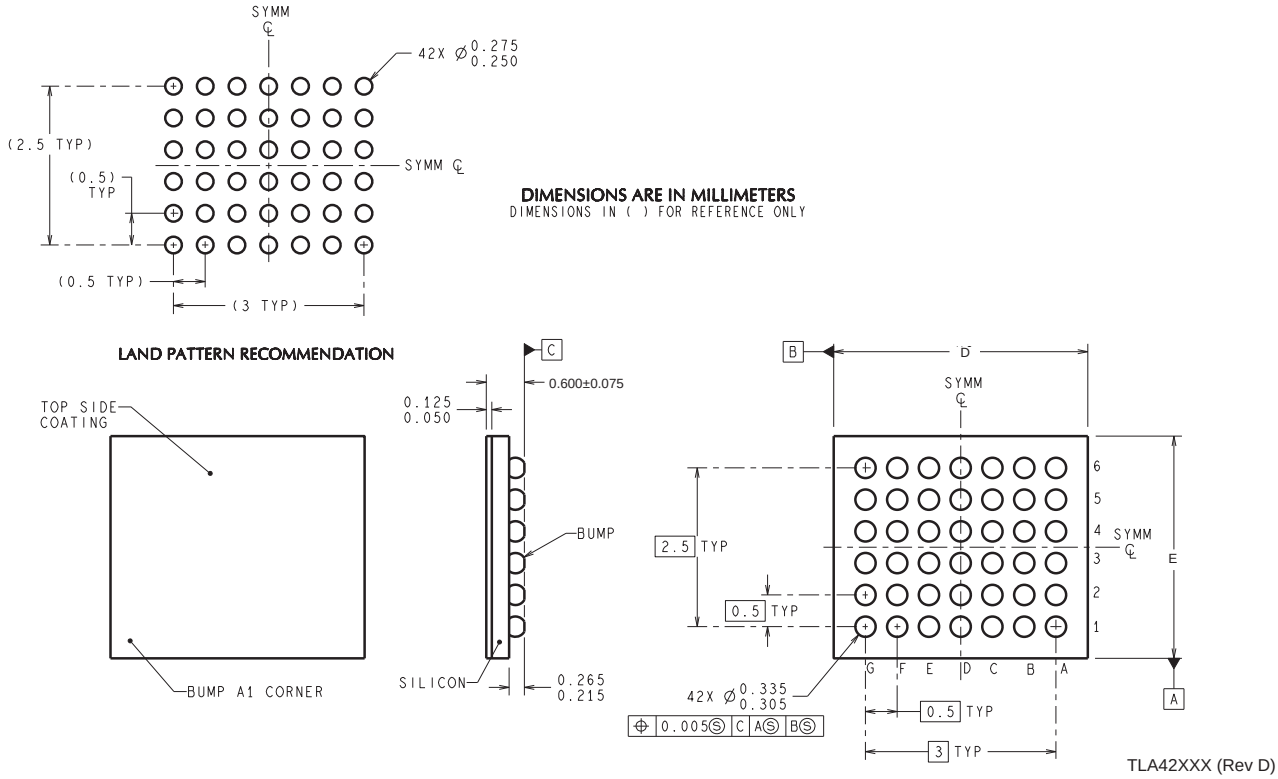
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM4931ITL/NOPB	DSBGA	YZR	42	250	203.0	190.0	41.0

YZR0042



D: Max = 3.986 mm, Min =3.885 mm

E: Max = 3.579 mm, Min =3.478 mm

4215060/A 12/12

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.

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