LM49321 Boomer® Audio Power Amplifier Series Audio Sub-System with Stereo DAC, Mono Class AB Loudspeaker Amplifier, OCL/SE Stereo Headphone Output and RF Suppression

Check for Samples: LM49321, LM49321RLEVAL

FEATURES

- **18-bit stereo DAC with up to 192kHz sampling rate**
- **Multiple distinct output modes**
- **Mono class AB speaker amplifier**
- **Stereo OCL/SE headphone amplifier**
- **Mono earpiece amplifier**
- **Differential mono analog input**
- **Single-ended analog inputs**
- **Independent loudspeaker, headphone and mono earpiece volume controls**
- **I^2C/SPI (selectable) compatible interface**
- **Ultra low shutdown current**
- **Click and Pop Suppression circuit**

APPLICATIONS

- **Cell Phones**
- **PDAs**
- **Laptop computers**
- **Portable devices**

DESCRIPTION

The LM49321 is an integrated audio sub-system designed for mono voice, stereo music cell phones connecting to base band processors with mono differential analog voice paths. Operating on a 3.3V supply, it combines a mono speaker amplifier delivering 520mW into an 8Ω load, a stereo headphone amplifier delivering 36mW per channel into a 32Ω load, and a mono earpiece amplifier delivering 55mW into a 32Ω load. The headphone amplifier can be configured for output capacitor-less (OCL) or single-ended (SE) mode. It integrates the audio amplifiers, volume control, mixer, and power management control all into a single package. In addition, the LM49321 routes and mixes the single-ended stereo and differential mono inputs into multiple distinct output modes. The LM49321 features an I^2S serial interface for full range audio and an I^2C or SPI compatible interface for control. The full range music path features an SNR of 85dB with up to 192kHz playback.

Boomer audio power amplifiers are designed specifically to provide high quality output power with a minimal amount of external components.

Table 1. Key Specifications

	VALUE	UNIT
P_{OUT} LS, 8Ω, 3.3V, 1% THD+N	520	mW (typ)
P_{OUT} HP, 32Ω, 3.3V, 1% THD+N	36	mW (typ)
P_{OUT} Mono Earpiece, 32Ω 1% THD+N	55	mW (typ)
Shutdown current	0.6	µA (typ)
SNR (DAC + Amplifier)	85	dB (typ)

Block Diagram

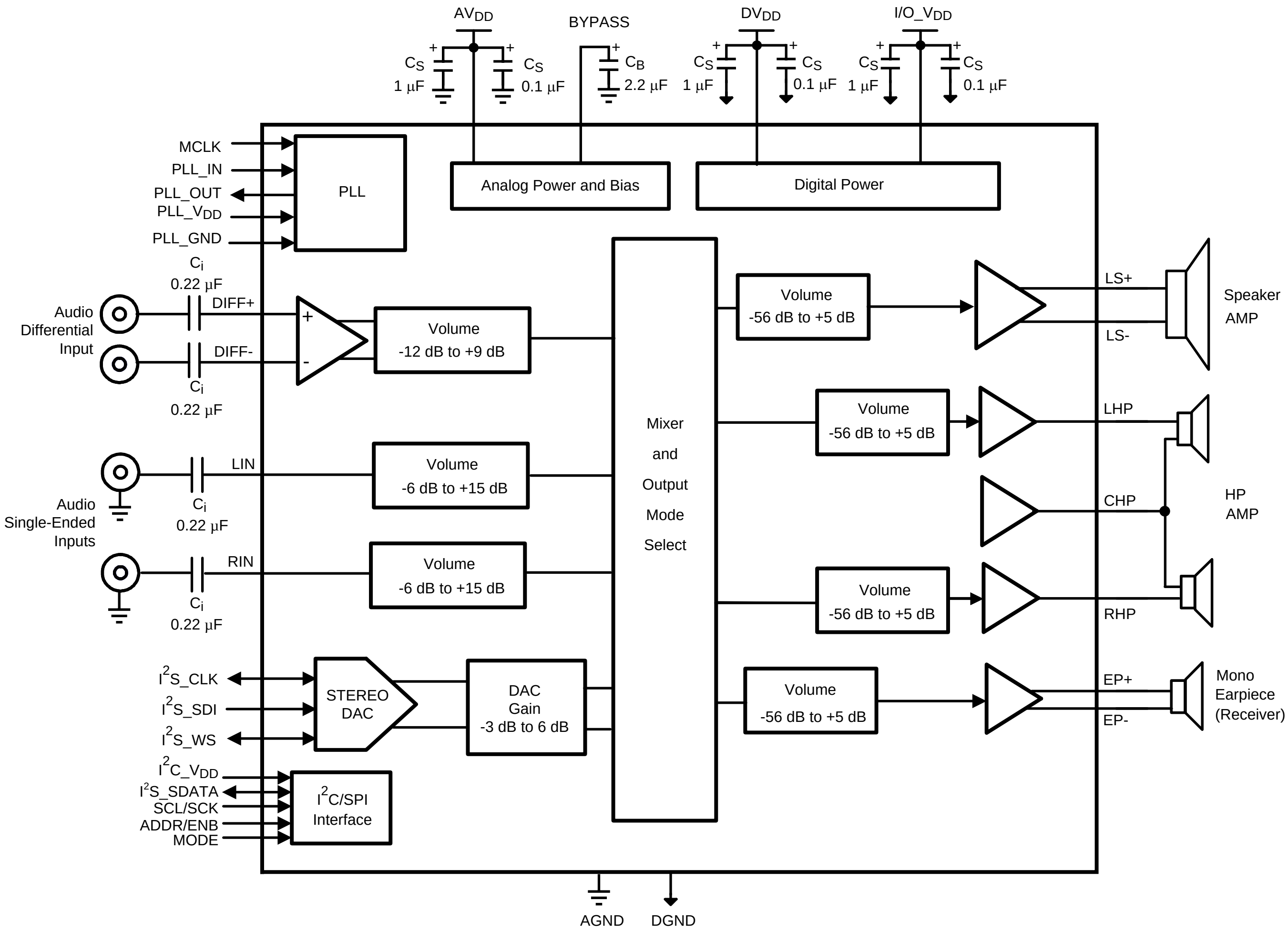

Figure 1. Typical Audio Amplifier Subsystem Application circuit with Output Capacitor-less (OCL) Headphone configuration

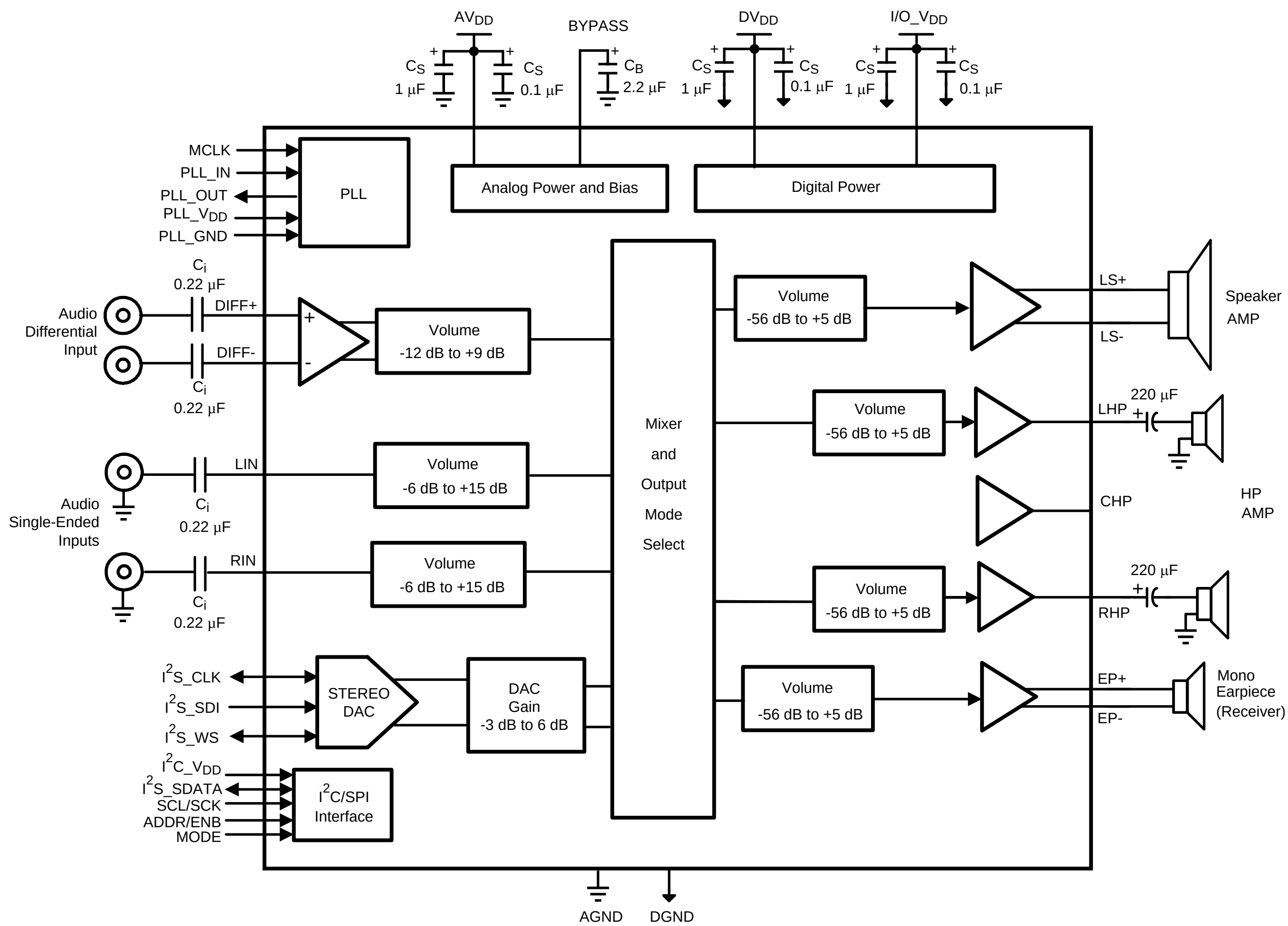

Figure 2. Typical Audio Amplifier Subsystem Application circuit with Cap-C`oupled single-ended (SE) Headphone configuration

Connection Diagram

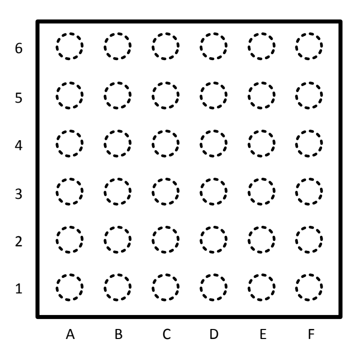

Figure 3. Top View (Bump Side Down)
36 – Bump Micro SMD

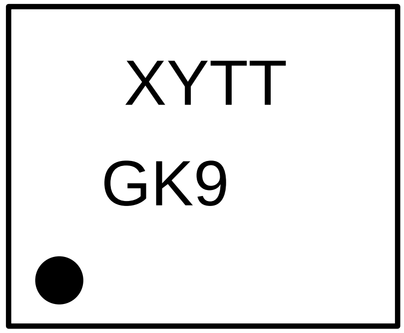

Figure 4. 36 – Bump Micro SMD - Top View
XY — 2 Digit Date Code
TT — Die Traceability
G — Boomer Family
K9 — LM49321RL

Pin Functions

Pin Descriptions

Pin	Pin Name	Digital/Analog	I/O, Power	Description
A1	DGND	D	P	DIGITAL GND
A2	MCLK	D	I	MASTER CLOCK
A3	I^2S_WS	D	I/O	I^2S WORD SELECT
A4	SDA/SDI	D	I/O	I^2C SDA OR SPI SDI
A5	DV_{DD}	D	P	DIGITAL SUPPLY VOLTAGE
A6	I/O_V_{DD}	D	P	I/O SUPPLY VOLTAGE
B1	PLL_VDD	D	P	PLL SUPPLY VOLTAGE
B2	I^2S_SDATA	D	I	I^2S SERIAL DATA INPUT
B3	I^2S_CLK	D	I/O	I^2S CLOCK SIGNAL
B4	GPIO	D	O	TEST PIN (MUST BE LEFT FLOATING)
B5	I^2C_V_{DD}	D	P	I^2C SUPPLY VOLTAGE
B6	SDL/SCK	D	I	I^2C_SCL OR SPI_SCK
C1	PLL_GND	D	P	PHASE LOCK LOOP GROUND
C2	PLL_OUT	D	O	PHASE LOCK LOOP FILTER OUTPUT
C3	PLL_IN	D	I	PLL FILTER INPUT
C4	ADDR/ENB	D	I	I^2C ADDRESS OR SPI ENB DEPENDING ON MODE
C5	BYPASS	A	I	HALF-SUPPLY BYPASS
C6	AV_{DD}	A	P	ANALOG SUPPLY VOLTAGE
D1	AGND	A	P	ANALOG GROUND
D2	AGND	A	P	ANALOG GROUND
D3	NC			NO CONNECT (MUST BE LEFT FLOATING)
D4	MODE	D	I	SELECTS BETWEEN I^2C OR SPI CONTROL
D5	RHP	A	O	RIGHT HEADPHONE OUTPUT
D6	CHP	A	O	HEADPHONE CENTER PIN OUTPUT (1/2 VDD or GND)
E1	DIFF-	A	I	ANALOG NEGATIVE DIFFERENTIAL INPUT
E2	LIN	A	I	ANALOG LEFT CHANNEL INPUT
E3	RIN	A	I	ANALOG RIGHT CHANNEL INPUT
E4	NC			NO CONNECT (MUST BE LEFT FLOATING)
E5	LHP	A	O	LEFT HEADPHONE OUTPUT

Pin Descriptions (continued)

E6	AGND	A	P	ANALOG GROUND
F1	DIFF+	A	I	ANALOG POSITIVE DIFFERENTIAL INPUT
F2	EP-	A	O	MONO EARPIECE- OUTPUT
F3	EP+	A	O	MONO EARPIECE+ OUTPUT
F4	LS-	A	O	LOUDSPEAKER OUTPUT-
F5	AV_{DD}	A	P	ANALOG SUPPLY VOLTAGE
F6	LS+	A	O	LOUDSPEAKER OUTPUT+

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings (1) (2)

Analog Supply Voltage (Note 1)	6.0V
Digital Supply Voltage (Note 1)	6.0V
Storage Temperature	-65°C to +150°C
Input Voltage	-0.3V to V_{DD} +0.3V
Power Dissipation (3)	Internally Limited
ESD Ratings (Note 4)	2000V
ESD Ratings (Note 5)	200V
Junction Temperature (T_{JMAX})	150°C
Thermal Resistance	
θ_{JA} (RLA36)	100°C/W
Soldering Information	
See AN-1279 “Microfill Wafer Level Underfilled Chip Scale package.”	

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(2) The *Electrical Characteristics* tables list guaranteed specifications under the listed *Recommended Operating Conditions* except as otherwise modified or specified by the *Electrical Characteristics Conditions* and/or Notes. Typical specifications are estimations only and are not guaranteed.
(3) Maximum allowable power dissipation is $P_{DMAX} = (T_{JMAX} - T_A) / \theta_{JA}$ or the number given in *Absolute Maximum Ratings*, whichever is lower.

Operating Ratings (1) (2)

Temperature Range	
$T_{MIN} \le T_A \le T_{MAX}$	$-40°C \le T_A \le +85°C$
Supply Voltage	
	$2.7V \le AV_{DD} \le 5.5V$
	$2.7V \le DV_{DD} \le 4.0V$
	$1.7V \le I^2C\_V_{DD} \le 4.0V$
	$1.7V \le I/O\_V_{DD} \le 4.0V$

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Audio Amplifier Electrical Characteristics AV_{DD} = 3.0V, DV_{DD} = 3.0V (1) (2)

The following specifications apply for the circuit shown in Figure 1 with all programmable gain set at 0dB, unless otherwise specified. Limits apply for T_A = 25°C.

Symbol	Parameter	Conditions	LM49321		Units (Limits)
			Typical (3)	Limits (4)	
I_{DD}	Supply Current	V_{IN} = 0, No Load All Amps On + DAC, OCL (Note 10)	13	18	mA (max)
		Headphone Mode Only, OCL, DAC off	4.6	6.25	mA (max)
		Headphone Mode Only, OCL, DAC Off STEREO_OUTPUT_ONLY = 1, STEREO_INPUT_ONLY = 1	4	5.5	mA
		Headphone Mode only OCL, DAC On, OSR = 64, DAC_INPUT_ONLY = 1 STEREO_OUTPUT_ONLY = 1	7.5	10	mA (max)
		Mono Loudspeaker Mode Only (Note 11)	6.5	11.5	mA (max)
		Mono Earpiece Speaker Mode Only MONO_ONLY = 1 (register 01h) MONO_ONLY = 0	3.7 3.3	5	mA (max) mA
		DAC Off, All Amps On (OCL) (Note 10)	10	13.5	mA (max)
I_{SD}	Shutdown Current	(Note 8)	0.6	1	μA (max)
P_O	Output Power	Speaker; THD = 1%; f = 1kHz, 8Ω BTL	420	370	mW (min)
		Headphone; THD = 1%; f = 1kHz, 32Ω SE	27	24	mW (min)
		Earpiece; THD = 1%; f = 1kHz, 32Ω BTL	45	40	mW (min)
$V_{FS\ DAC}$	Full Scale DAC Output		2.4		V_{RMS}
THD+N	Total Harmonic Distortion+Noise	Speaker; P_O = 200mW; f = 1kHz, 8Ω BTL	0.04		%
		Headphone; P_O = 10mW; f = 1kHz, 32Ω SE	0.01		%
		Earpiece; P_O = 20mW; f = 1kHz, 32Ω BTL	0.04		%
V_{OS}	Offset Voltage	Speaker	10	55	mV (max)
		Earpiece	8	50	mV (max)
		Headphone (OCL)	8	15	mV (max)
ϵ_O	Output Noise	A-weighted; 0dB gain	Table 1		
PSRR	Power Supply Rejection Ratio	f = 217Hz; V_{RIPPLE} = 200mV_{P-P} C_B = 2.2µF	Table 2		
X_{TALK}	Crosstalk	Headphone; P_O = 10mW, f = 1kHz; OCL	–60		dB
T_{WU}	Wake-Up Time	C_B = 2.2µF, CD_6 = 0	35		ms
		C_B = 2.2µF, CD_6 = 1	85		ms
CMRR	Common-Mode Rejection Ratio	f = 217Hz, V_{RMS} = 200mV_{PP}	56		dB

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(2) The *Electrical Characteristics* tables list guaranteed specifications under the listed *Recommended Operating Conditions* except as otherwise modified or specified by the *Electrical Characteristics Conditions* and/or Notes. Typical specifications are estimations only and are not guaranteed.
(3) Typical values represent most likely parametric norms at T_A = +25ºC, and at the *Recommended Operation Conditions* at the time of product characterization and are not guaranteed.
(4) Datasheet min/max specification limits are guaranteed by test or statistical analysis.

Audio Amplifier Electrical Characteristics AV_{DD} = 5.0V, DV_{DD} = 3.3V (1) (2)

The following specifications apply for the circuit shown in Figure 1 with all programmable gain set at 0dB, unless otherwise specified. Limits apply for T_A = 25°C.

Symbol	Parameter	Conditions	LM49321		Units (Limits)
			Typical (3)	Limits (4)	
I_{DD}	Supply Current	V_{IN} = 0, No Load All Amps On + DAC, OCL (Note 10)	17.5		mA (max)
		Headphone Mode Only, OCL, DAC Off	5.8		mA (max)
		Headphone Mode Only, OCL, DAC Off STEREO_OUTPUT_ONLY = 1, STEREO_INPUT_ONLY = 1	5.5		mA
		Headphone Mode Only, OCL, DAC On, OSR = 64, DAC_INPUT_ONLY = 1 STEREO_OUTPUT_ONLY = 1	9.5		mA
		Mono Loudspeaker Mode Only (Note 10)	11.6		mA
		Mono Earpiece Mode Only (Note 10)	5		mA
		DAC Off, All Amps On (OCL) (Note 10)	12.9		mA
I_{SD}	Shutdown Current	(Note 8)	1.6		µA
P_O	Output Power	Speaker; THD = 1%; f = 1kHz, 8Ω BTL	1.25		mW
		Headphone; THD = 1%; f = 1kHz, 32Ω SE	80		mW
		Earpiece; THD = 1%; f = 1kHz, 32Ω BTL	175		mW
$V_{FS\ DAC}$	Full Scale DAC Output		2.4		V_{RMS}
THD+N	Total Harmonic Distortion + Noise	Speaker; P_O = 500mW; f = 1kHz, 8Ω BTL	0.03		%
		Headphone; P_O = 30mW; f = 1kHz, 32Ω SE	0.01		%
		Earpiece; P_O = 40mW; f = 1kHz, 32Ω BTL	0.04		%
V_{OS}	Offset Voltage	Speaker	10		mV
		Earpiece	8		mV
		HP (OCL)	8		mV
ϵ_O	Output Noise	A-weighted; 0dB gain;	Table 1		
PSRR	Power Supply Rejection Ratio	f = 217Hz; V_{ripple} = 200mV$_{P-P}$ C_B = 2.2µF	Table 3		
X_{TALK}	Crosstalk	Headphone; P_O= 15mW, f = 1kHz; OCL	–56		dB
T_{WU}	Wake-Up Time	C_B = 2.2µF, CD_6 = 0	45		ms
		C_B = 2.2µF, CD_6 = 1	130		ms

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(3) Typical values represent most likely parametric norms at T_A = +25ºC, and at the *Recommended Operation Conditions* at the time of product characterization and are not guaranteed.
(4) Datasheet min/max specification limits are guaranteed by test or statistical analysis.

Volume Control Electrical Characteristics (1) (2)

The following specifications apply for 3.0V ≤ AV_{DD} ≤ 5.0V and 2.7V ≤ DV_{DD} ≤ 4.0V, unless otherwise specified. Limits apply for T_A = 25°C.

Symbol	Parameter	Conditions	LM49321 Typical (3)	LM49321 Limits (4)	Units (Limits)
PGR	Stereo Analog Inputs Pre-Amp Gain Setting Range	minimum gain setting	–6	–7	dB (min)
				–5	dB (max)
		maximum gain setting	15	15.5	dB (max)
				14.5	dB (min)
	Differential Mono Analog Input Pre-Amp Gain Setting Range	minimum gain setting	–12	–13	dB (min)
				–11	dB (max)
		maximum gain setting	9	9.5	dB (max)
				8.5	dB (min)
VCR	Output Volume Control for Loudspeaker, Headphone Output, or Earpiece Output	minimum gain setting	–56	–59	dB (min)
				–53	dB (max)
		maximum gain setting	+5	4.5	dB (min)
				5.5	dB (max)
ΔA_{CH-CH}	Stereo Channel to Channel Gain Mismatch		0.3		dB
A_{MUTE}	Mute Attenuation	V_{IN} = 1V_{RMS}, Gain = 0dB with load, Headphone	–90		dB
R_{INPUT}	DIFF+, DIFF-, L_{IN} and R_{IN} Input Impedance		23	18	kΩ (min)
				28	kΩ (max)

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(4) Datasheet min/max specification limits are guaranteed by test or statistical analysis.

Digital Section Electrical Characteristics (1) (2)

The following specifications apply for 3.0V ≤ AV_{DD} ≤ 5.0V and 2.7V ≤ DV_{DD} ≤ 4.0V, unless otherwise specified. Limits apply for T_A = 25°C.

Symbol	Parameter	Conditions	LM49321		Units (Limits)
			Typical (3)	Limits (4)	
DI_{SD}	Digital Shutdown Current	Mode 0, DV_{DD} = 3.0V			
		No MCLK	0.01		µA
DI_{DD}	Digital Power Supply Current	f_{MCLK} = 12MHz, DV_{DD} = 3.0V ALL MODES EXCEPT 0	5.3	6.5	mA (max)
$PLLI_{DD}$	PLL Quiescent Current	f_{MCLK} = 12MHz, DV_{DD} = 3.0V	4.8	6	mA (max)
Audio DAC (Typical numbers are with 6.144MHz audio clock and 48kHz sampling frequency					
R_{DAC}	Audio DAC Ripple	20Hz - 20kHz through headphone output	+/-0.1		dB
PB_{DAC}	Audio DAC Passband width	-3dB point	22.6		kHz
SBA_{DAC}	Audio DAC Stop band Attenuation	Above 24kHz	76		dB
DR_{DAC}	Audio DAC Dynamic Range	DC - 20kHz, –60dBFS; AES17 Standard	Table 4		dB
SNR	Audio DAC-AMP Signal to Noise Ratio	A-Weighted, Signal = V_O at 0dBFS, f = 1kHz Noise = digital zero, A-weighted	Table 4		dB
SNR_{DAC}	Internal DAC SNR	A-weighted (Note 9)	95		dB
PLL					
f_{IN}	Input Frequency on MCLK pin		12	10	MHz
				26	
SPI/I²C (1.7V ≤ $I^2C\_V_{DD}$ ≤ 2.2V)					
f_{SPI}	Maximum SPI Frequency			1000	kHz (max)
$t_{SPISETD}$	SPI Data Setup Time			250	ns (max)
$t_{SPISETENB}$	SPI ENB Setup Time			250	ns (max)
$t_{SPIHOLDD}$	SPI Data Hold Time			250	ns (max)
$t_{SPIHOLDENB}$	SPI ENB Hold Time			250	ns (max)
t_{SPICL}	SPI Clock Low Time			500	ns (max)
t_{SPICH}	SPI Clock High Time			500	ns (max)
f_{CLKI2C}	I^2C_CLK Frequency			400	kHz (max)
$t_{I2CHOLD}$	I^2C_DATA Hold Time			250	ns (max)
t_{I2CSET}	I^2C_DATA Setup Time			250	ns (max)
V_{IH}	I^2C/SPI Input High Voltage		$I^2C\_V_{DD}$	0.7 x $I^2C\_V_{DD}$	V (min)
V_{IL}	I^2C/SPI Input Low Voltage		0	0.25 x $I^2C\_V_{DD}$	V (max)
SPI/I²C (2.2V ≤ $I^2C\_V_{DD}$ ≤ 4.0V)					
f_{SPI}	Maximum SPI Frequency			4000	kHz (max)
$t_{SPISETD}$	SPI Data Setup Time			100	ns (max)
$t_{SPISETENB}$	SPI ENB Setup Time			100	ns (max)
$t_{SPIHOLDD}$	SPI Data Hold Time			100	ns (max)
$t_{SPIHOLENB}$	SPI ENB Hold Time			100	ns (max)

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(3) Typical values represent most likely parametric norms at T_A = +25ºC, and at the *Recommended Operation Conditions* at the time of product characterization and are not guaranteed.
(4) Datasheet min/max specification limits are guaranteed by test or statistical analysis.

Digital Section Electrical Characteristics [(1)] [(2)] (continued)

The following specifications apply for 3.0V ≤ AV_{DD} ≤ 5.0V and 2.7V ≤ DV_{DD} ≤ 4.0V, unless otherwise specified. Limits apply for T_A = 25°C.

Symbol	Parameter	Conditions	LM49321		Units (Limits)
			Typical [(3)]	Limits [(4)]	
t_{SPICL}	SPI Clock Low Time			125	ns (max)
t_{SPICH}	SPI Clock High Time			125	ns (max)
f_{CLKI2C}	I^2C_CLK Frequency			400	kHz (max)
$t_{I2CHOLD}$	I^2C_DATA Hold Time			100	ns (max)
t_{I2CSET}	I^2C_DATA Setup Time			100	ns (max)
V_{IH}	I^2C/SPI Input High Voltage		$I^2C\_V_{DD}$	0.7 x $I^2C\_V_{DD}$	V (min)
V_{IL}	I^2C/SPI Input Low Voltage		0	0.3 x $I^2C\_V_{DD}$	V (max)
I^2S(1.7V ≤ I/O_V_{DD} ≤ 2.7V)					
f_{CLKI^2S}	I^2S_CLK Frequency	I^2S_RESOLUTION = 1 I^2S_RESOLUTION = 0	1536 3072	6144 12288	kHz (max) kHz (max)
	I^2S_WS Duty Cycle		50	40 60	% (min) % (max)
V_{IH}	Digital Input High Voltage			0.75 x I/O_V_{DD}	V (min)
V_{IL}	Digital Input Low Voltage			0.25 x I/O_V_{DD}	V (max)
I^2S(2.7V ≤ I/O_V_{DD} ≤ 4.0V)					
f_{CLKI^2S}	I^2S_CLK Frequency	I^2S_RESOLUTION = 0	1536 3072	6144 12288	kHz (max) kHz (max)
	I^2S_WS Duty Cycle	I^2S_RESOLUTION = 1	50	40 60	% %
V_{IH}	Digital Input High Voltage			0.7 x I/O_V_{DD}	V (min)
V_{IL}	Digital Input Low Voltage			0.3 x I/O_V_{DD}	V (max)

Table 2. Output NoiseOutput Noise AV_{DD} = 5.0V and AV_{DD} = 3.0V. All gains set to 0dB. Units in µV, A-weighted, Inputs terminated to ground.

MODE	EP	LS	HP OCL	Units
1	22	22	8	µV
2	22	22	8	µV
3	22	22	8	µV
4	68	88	46	µV
5	38	48	24	µV
6	29	34	18	µV
7	38	48	24	µV

Table 3. PSRR AV_{DD} = 3.0VPSRR AV_{DD} = 3.0V, f_{RIPPLE} = 217Hz; $V_{RIPPLEe}$ = 200mV_{P-P}; C_B = 2.2µF; All gains set to 0dB..

MODE	EP(Typ)	LS (Typ)	LS (Limit)	HP (Typ)	HP (Limit)	Units
1	69	76		72		dB
2	69	76	67	72	68	dB
3	69	76		72		dB
4	63	62		55		dB
5	69	68		61		dB

Table 3. PSRR AV_{DD} = 3.0VPSRR AV_{DD} = 3.0V, f_{RIPPLE} = 217Hz; $V_{RIPPLEe}$ = 200mV$_{P-P}$; C_B = 2.2µF; All gains set to 0dB..

(continued)

MODE	EP(Typ)	LS (Typ)	LS (Limit)	HP (Typ)	HP (Limit)	Units
6	69	70		64		dB
7	69	68		61		dB

Table 4. PSRR AV_{DD} = 5.0VPSRR AV_{DD} = 5.0V, f_{RIPPLE} = 217Hz; V_{RIPPLE} = 200mV$_{P-P}$; C_B = 2.2µF; All gains set to 0dB,

MODE	EP (Typ)	LS (Typ)	HP (Typ)	Units
1	68	72	71	dB
2	68	72	71	dB
3	68	72	71	dB
4	68	66	69	dB
5	68	69	70	dB
6	69	72	71	dB
7	68	69	70	dB

Table 5. Dynamic Range and SNRDynamic Range and SNR. 3.0V ≤ AV_{DD} ≤ 5.0V. All programmable gain set to 0dB. Units in dB.

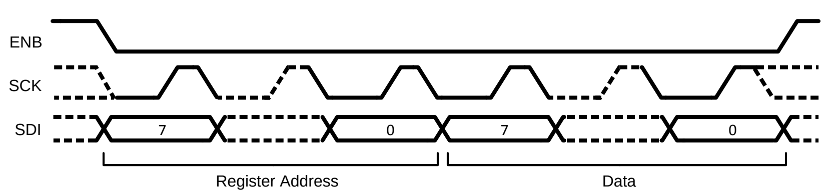
	DR (Typ)	SNR (Typ)	Units
LS	95	85	dB
HP	95	85	dB
EP	97	85	dB

System Control

The LM49321 is controlled via either a two wire I^{2}C compatible interface or three wire SPI interface, selectable with the MODE pin. This interface is used to configure the operating mode, interfaces, data converters, mixers and amplifiers. The LM49321 is controlled by writing 8 bit data into a series of write-only registers, the device is always a slave for both type of interfaces.

THREE WIRE, SPI INTERFACE (MODE = 1)

Three Wire Mode Write Bus Transaction



Three Wire Mode Write Bus Timing

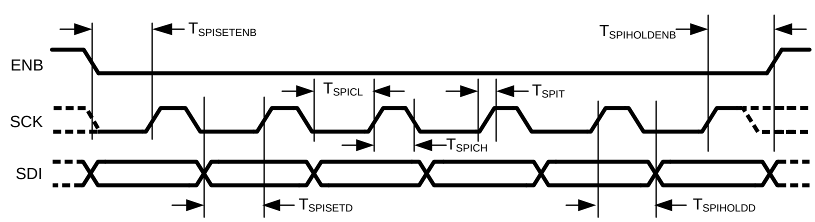
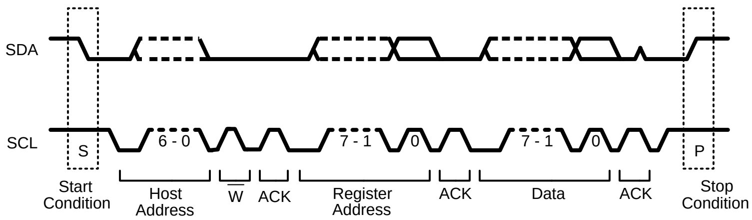


Figure 5. Three Wire Mode Write Bus

When the part is configured as an SPI device and the enable (ENB) line is lowered the serial data on SDI is clocked in on the rising edge of the SCK line. The protocol used is 16bit, MSB first. The upper 8 bits (15:8) are used to select an address within the device, the lower 8 bits (7:0) contain the updated data for this register.

TWO WIRE I^{2}C COMPATIBLE INTERFACE (MODE = 0)

Two Wire Mode Write Bus Transaction



Two Wire Mode Write Bus Timing

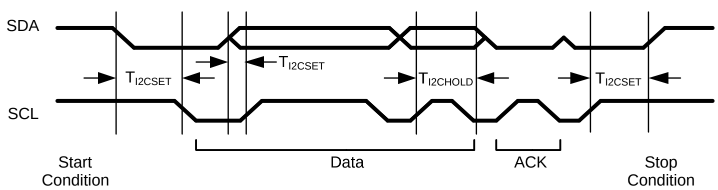


Figure 6. Two Wire Mode Write Bus

When the part is configured as an I^{2}C device then the LM49321 will respond to one of two addresses, according to the ADDR input. If ADDR is low then the address portion of the I^{2}C transaction should be set to write to 0010000. When ADDR is high then the address input should be set to write to 1110000.

Table 6. Chip Address

	A7	A6	A5	A4	A3	A2	A1	A0
Chip Address	0	EC	EC	1	0	0	0	0
ADR = 0	0	0	0	1	0	0	0	0
ADR = 1	0	1	1	1	0	0	0	0

Table 7. Control Registers

Address	Register	D7	D6	D5	D4	D3	D2	D1	D0
00h	MODE_CONTROL	0	CD_6	0	OCL	MODE_CONTROL			
01h	OUTPUT_ CONTROL	STEREO_ OUT_ONLY	MONO_ONLY	DAC_INPUT _ONLY	STEREO_INPUT_ ONLY	HP_R_ OUTPUT	HP_L_ OUTPUT	LS_ OUTPUT	MONO_ OUTPUT
02h	EP_VOL	0	0	0	EP_VOL				
03h	LS_VOL	0	0	0	LS_VOL				
04h	RESERVED	0	0	0	0	0	0	0	0
05h	HP_L_VOL	0	0	0	HP_L_VOL				
06h	HP_R_VOL	0	0	0	HP_R_VOL				
07h	ANALOG_INPUT _GAIN	0	0	ANA_R_GAIN			ANA_L_GAIN		
08h	ANALOG_DAC _GAIN	0	DAC_R_GAIN		DAC_L_GAIN		MONO_L_GAIN		

Table 7. Control Registers (continued)

Address	Register	D7	D6	D5	D4	D3	D2	D1	D0
09h	CLOCKS	R_DIV				PLL_ ENABLE	AUDIO _CLK_SEL	PLL_INPUT	FAST_ CLOCK
0Ah	PLL_M	0	PLL_M						
0Bh	PLL_N								
0Ch	PLL_N_MOD	VCO_F AST	DITHER_LE VEL	DITHER_LEV EL	PLL_N_MOD				
0Dh	PLL_P	0	0	0	0	PLL_P			
0Eh	DAC_SET UP	0	CUST_CO MP	DITHER_AL W_ON	DITHER_OFF	MUTE_R	MUTE_L	DAC_MODE	
0Fh	INTERFACE	0	0	0	0	I^2C_FAST	I^2S_MODE	I^2S_ RESOLUTI ON	I^2S_MASTE R_ SLAVE
10h	COMPENSATION _C OEFF0_LSB								
11h	COMPENSATION _C OEFF0_MSB								
12h	COMPENSATION _C OEFF1_LSB								
13h	COMPENSATION _C OEFF1_MSB								
14h	COMPENSATION _C OEFF2_LSB								
15h	COMPENSATION _C OEFF2_MSB								

Mixer Control Registers

This register is used to control the different mixer modes that the LM49321 supports.

Table 8. Mode Control Register (00h)

Bits	Field	Description					
3:0	MODE _CONTROL	This sets the different mixer output modes.					
		MODE_CONTROL	Mode	Mono Earpiece	Loudspeaker	Headphone Left	Headphone Right
		0000	0	SD	SD	SD	SD
		1001	1	M	M	M	M
		1010	2	AL+AR	AL+AR	AL	AR
		1011	3	M+AL+AR	M+AL+AR	M+AL	M+AR
		1100	4	DL+DR	DL+DR	DL	DR
		1101	5	DL+DR+AL+AR	DL+DR+AL+AR	DL+AL	DR+AR
		1110	6	M+DL+DR+AL+AR	M+DL+DR+AL+A R	M+DL+AL	M+DR+AR
		1111	7	M+DL+DR	M+DL+DR	M+DL	M+DR
4	OCL	This sets the headphone output to use output capacitor-less configuration.					
		OCL	Headphone output configuration				
		0	Cap-coupled Single-ended Mode (SE)				
		1	Output capacitor-less (OCL)				

This register is used to control the different output configurations.

Table 9. Output Control (01h)

Bits	Field	Description	
0	EP_OUTPUT	This enables the Mono Earpiece output.	
		EP_OUTPUT	Status
		0	Mono earpice output off
		1	Mono earpice output on

Table 9. Output Control (01h) (continued)

<table>
<tr><th>Bits</th><th>Field</th><th colspan="2">Description</th></tr>
<tr><td rowspan="4">1</td><td rowspan="4">LS_OUTPUT</td><td colspan="2">This enables the Mono Loudspeaker output.</td></tr>
<tr><td>LS_OUTPUT</td><td>Status</td></tr>
<tr><td>0</td><td>Loudspeaker output off</td></tr>
<tr><td>1</td><td>Loudspeaker output on</td></tr>
<tr><td rowspan="4">2</td><td rowspan="4">HP_L_OUTPUT</td><td colspan="2">This enables the Headphone left output.</td></tr>
<tr><td>HP_L_OUTPUT</td><td>Status</td></tr>
<tr><td>0</td><td>Headphone left output off. If OCL=1, output is in mute.</td></tr>
<tr><td>1</td><td>Headphone left output on</td></tr>
<tr><td rowspan="4">3</td><td rowspan="4">HP_R_OUTPUT</td><td colspan="2">This enables the Headphone right output.</td></tr>
<tr><td>HP_R_OUTPUT</td><td>Status</td></tr>
<tr><td>0</td><td>Headphone right output off. If OCL=1, output is in mute.</td></tr>
<tr><td>1</td><td>Headphone right output on</td></tr>
<tr><td rowspan="4">4</td><td rowspan="4">STEREO_INPUT_ONLY</td><td colspan="2">This enables the analog left (AL) and analog right (AR) and disables all other inputs.</td></tr>
<tr><td>STEREO_INPUT_ONLY</td><td>Status</td></tr>
<tr><td>0</td><td>Normal</td></tr>
<tr><td>1</td><td>Enables AL and AR inputs only</td></tr>
<tr><td rowspan="4">5</td><td rowspan="4">DAC_INPUT_ONLY</td><td colspan="2">This enables the DAC left (DL) and analog right (DR) and disables all other inputs.</td></tr>
<tr><td>DAC_INPUT_ONLY</td><td>Status</td></tr>
<tr><td>0</td><td>Normal</td></tr>
<tr><td>1</td><td>Enables DL and DR inputs only</td></tr>
<tr><td rowspan="4">6</td><td rowspan="4">MONO_ONLY</td><td colspan="2">This enables mono earpiece (EP) and loudspeaker (LS) outputs MUX and disables the headphone outputs MUX. Enabling this mode can save up to 400µA of current.</td></tr>
<tr><td>MONO_ONLY</td><td>Status</td></tr>
<tr><td>0</td><td>Normal</td></tr>
<tr><td>1</td><td>Enable mono earpiece and loudspeaker outputs MUX</td></tr>
<tr><td rowspan="4">7</td><td rowspan="4">STEREO_OUTPUT_ONLY</td><td colspan="2">This enables the headphone output MUX only and disables all other output MUX's. Enabling this mode can save up to 200µA of current.</td></tr>
<tr><td>STEREO_OUTPUT_ONLY</td><td>Status</td></tr>
<tr><td>0</td><td>Normal</td></tr>
<tr><td>1</td><td>Enables the headphone output MUX</td></tr>
</table>

Volume Control Registers

These registers are used to control output volume control levels for Earpiece, Loudspeaker and Headphone.

Table 10. Volume Control Register

Table 10. Volume Control Register EP_VOL (02h), LS_VOL (03h), HP_L_VOL (05h), HP_R_VOL (06h) (continued)

EP_VOL (02h), LS_VOL (03h), HP_L_VOL (05h), HP_R_VOL (06h)

Bits	Field	Description	
4:0	EP_VOL LS_VOL HP_L_VOL HP_R_VOL	This programs the Earpiece, Loudspeaker and Headphone volume level.	
		VOL	Level (dB)
		00000	MUTE
		00001	–56
		00010	–52
		00011	–48
		00100	–45
		00101	–42
		00110	–39
		00111	–36
		01000	–33
		01001	–30
		01010	–28
		01011	–26
		01100	–24
		01101	–22
		01110	–20
		01111	–18
		10000	–16
		10001	–14
		10010	–12
		10011	–10
		10100	–8
		10101	–6
		10110	–4
		10111	–3
		11000	–2
		11001	–1
		11010	0
		11011	1
		11100	2
		11101	3
		11110	4
		11111	5

This register is used to control input gain for left and right analog inputs.

Table 11. Analog Left and Right Input Control (07h)

Bits	Field	Description	
2:0	ANA_L_GAIN	This program the analog left input gain.	
		ANA_L_GAIN	Level (dB)
		000	–6
		001	–3
		010	0
		011	3
		100	6
		101	9
		110	12
		111	15
5:3	ANA_R_GAIN	This program the analog Right input gain.	
		ANA_R_GAIN	Level (dB)
		000	–6
		001	–3
		010	0
		011	3
		100	6
		101	9
		110	12
		111	15

This register is sued to control input gain for Mono, DAC left and right inputs.

Table 12. Mono and DAC Input Gain Control (08h)

Bits	Field	Description	
2:0	MONO_IN_GAIN	This program the mono input gain.	
		MONO_IN_GAIN	Level (dB)
		000	–12
		001	–9
		010	–6
		011	–3
		100	0
		101	3
		110	6
		111	9
4:3	DAC_L_GAIN	This program the DAC left input gain.	
		DAC_L_GAIN	Level (dB)
		00	–3
		01	0
		10	3
		11	6

Table 12. Mono and DAC Input Gain Control (08h) (continued)

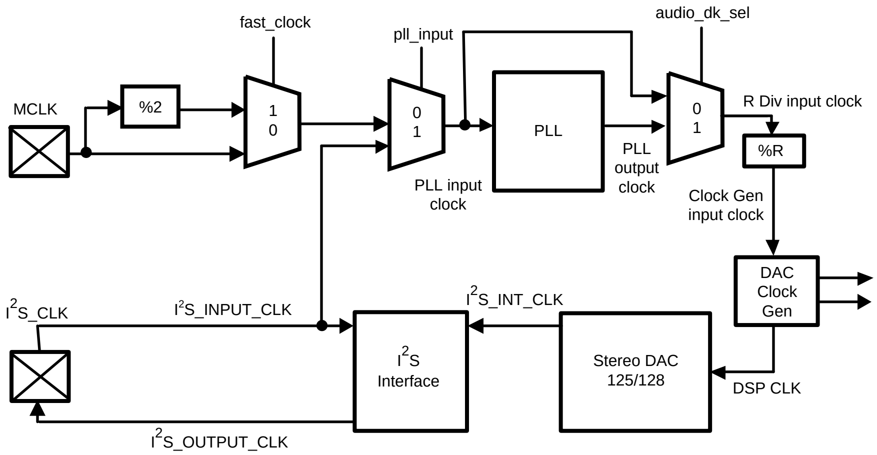
Bits	Field	Description	
6:5	DAC_R_GAIN	This program the DAC Right input gain.	
		DAC_R_GAIN	Level (dB)
		00	–3
		01	0
		10	3
		11	6

Clock Configuration Register

This register is used to control the multiplexers and clock R divider in the clock module.

Table 13. CLOCK (09h)

Bits	Register	Description	
0	FAST_CLOCK	If set master clock is divided by two.	
		FAST_CLOCK	MCLK Frequency
		0	Normal
		1	Divided by 2
1	PLL_INPUT	Programs the PLL input multiplexer to select:	
		PLL_INPUT	PLL Input Source
		0	MCLK
		1	I^2S Input Clock
2	AUDIO_CLK_SEL	Selects which clock is passed to the audio sub-system	
		DAC_CLK_SEL	DAC Sub-system Input Source
		0	PLL Input
		1	PLL Output
3	PLL_ENABLE	If set enables the PLL. (MODES 4–7 only)	
7:4	R_DIV	Programs the R divider	
		R_DIV	Divide Value
		0000	1
		0001	1
		0010	1.5
		0011	2
		0100	2.5
		0101	3
		0110	3.5
		0111	4
		1000	4.5
		1001	5
		1010	5.5
		1011	6
		1100	6.5
		1101	7
		1110	7.5
		1111	8



By default the stereo DAC operates at 250*fs, i.e. 12.000MHz (at the clock generator input clock) for 48kHz data. It is expected that the PLL be used to drive the audio system unless a 12.000MHz master clock is supplied. The PLL can also use the I2S clock input as a source. In this case, the audio DAC uses the clock from the output of the PLL.

Common Clock Settings for the DAC

The DAC can work in 4 modes, each with different oversampling rates, 125,128,64 & 32. In normal operation 125x oversampling provides for the simplest clocking solution as it will work from 12.000MHz (common in most systems with Bluetooth or USB) at 48kHz exactly. The other modes are useful if data is being provided to the DAC from an uncontrollable isochronous source (such as a CD player, DAB, or other external digital source) rather than being decoded from memory. In this case the PLL can be used to derive a clock for the DAC from the I2S clock.

The DAC oversampling rate can be changed to allow simpler clocking strategies, this is controlled in the DAC SETUP register but the oversampling rates are as follows:

DAC MODE	Over sampling Ratio Used
00	125
01	128
10	64
11	32

The following table describes the clock required at the clock generator input for various clock sample rates in the different DAC modes:

Fs (kHz)	DAC Oversampling Ratio	Required CLock at DAC Clock Generator Input (MHz)
8	125	2
8	128	2.048
11.025	125	2.75625
11.025	128	2.8224
12	125	3
12	128	3.072
16	125	4
16	128	4.096

Fs (kHz)	DAC Oversampling Ratio	Required CLock at DAC Clock Generator Input (MHz)
22.05	125	5.5125
22.05	128	5.6448
24	125	6
24	128	6.144
32	125	8
32	128	8.192
44.1	125	11.025
44.1	128	11.2896
48	125	12
48	128	12.288
88.2	64	11.2896
96	64	12.288
176.4	32	22.5792
192	32	24.576

Methods for producing these clock frequencies are described in the PLL section.

The R divider can be used when the master clock is exactly 12.00 MHz in order to generate different sample rates. The Table below shows different sample rates supported from 12.00MHz by using only the R divider and disabling the PLL. In this way we can save power and the clock jitter will be low.

R_DIV	Divide Value	DAC Clock Generator Input Frequency <MHz>	Sample Rate Supported <KHz>
11	6	2	8
9	5	2.4	9.6
7	4	3	12
5	3	4	16
4	2.5	4.8	19.2
3	2	6	24
2	1.5	8	32
0	1	12	48

The R divider can also be used along with the P divider in order to create the clock needed to support low sample rates.

PLL Configuration Registers

PLL M DIVIDER CONFIGURATION REGISTER

This register is used to control the input divider of the PLL.

Table 14. PLL_M (0Ah)

Bits	Register	Description	
6:0	PLL_M	Programs the PLL input divider to select:	
		PLL_M	Divide Ratio
		0000000	Divider Off
		0000001	1
		0000010	1.5
		0000011	2
		0000100	2.5
		...	...
		1111110	63.5

PLL N DIVIDER CONFIGURATION REGISTER

This register is used to control PLL N divider.

Table 15. PLL_N (0Bh)

Bits	Register	Description	
7:0	PLL_N	Programs the PLL feedback divider:	
		PLL_N	Divide Ratio
		00000000	Divider Off
		00000001 →00001010	10
		00001011	11
		00001100	12
		...	...
		11111000	248
		11111001	249

PLL P DIVIDER CONFIGURATION REGISTER

This register is used to control the PLL's P divider.

Table 16. PLL_P

Bits	Register	Description	
3:0	PLL_P	Programs the PLL input divider to select:	
		0000	Divider Off
		0001	1
		0010	1.5
		0011	2
		...	–> 2.5
		1101	7
		1110	7.5
		1111	8

PLL N MODULATOR AND DITHER SELECT CONFIGURATION REGISTER

This register is used to control the Fractional component of the PLL.

Table 17. PLL_N_MOD (0Ch)

Bits	Register	Description	
4:0	PLL_N_MOD	This programs the PLL N Modulator's fractional component:	
		PLL_N_MOD	Fractional Addition
		00000	0/32
		00001	1/32
		00010 → 11110	2/32 → 30/32
6:5	DITHER_LEVEL	Allows control over the dither used by the N Modulator	
		DITHER_LEVEL	DAC Sub-system Input Source
		00	Medium (32)
		01	Small (16)
		10	Large (48)
7	VCO_FAST	If set the VCO maximum and minimum frequencies are raised:	
		VCO_FAST	Maximum F_{VCO}
		0	40–55MHz

Further Notes on PLL Programming

The sigma-delta PLL is designed to drive audio circuits requiring accurate clock frequencies of up to 25MHz with frequency errors noise-shaped away from the audio band. The 5 bits of modulus control provide exact synchronization of 48kHz and 44.1kHz sample rates from any common clock source when the oversampling rate of the audio system is 125fs. In systems where 128x oversampling must be used (for example with an isochronous I^{2}S data stream) a clock synchronous to the sample rate should be used as input to the PLL (typically the I^{2}S clock). If no isochronous source is available then the PLL can be used to obtain a clock that is accurate to within typical crystal tolerances of the real sample rate.

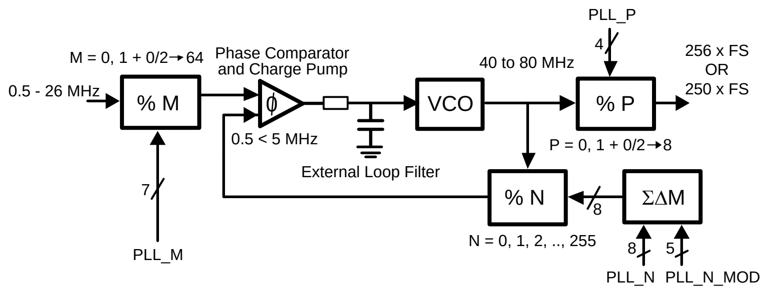


Table 18. Example Of PLL Settings For 48Khz Sample Rates

f_in (MHz)	fsamp (kHz)	M	N	P	PLL_M	PLL_N	PLL_N_MOD	PLL_P	f_out (MHz)
11	48	11	60	5	21	60	0	9	12
12	48	5	25	5	9	25	0	9	12
12.288	48	4	19.53125	5	7	19	17	9	12
13	48	13	60	5	25	60	0	9	12
14.4	48	9	37.5	5	17	37	16	9	12
16.2	48	27	100	5	53	100	0	9	12
16.8	48	14	50	5	27	50	0	9	12
19.2	48	13	40.625	5	25	40	20	9	12
19.44	48	27	100	6	53	100	0	11	12
19.68	48	20.5	62.5	5	40	62	16	9	12
19.8	48	16.5	50	5	32	50	0	9	12

Table 19. Example PLL Settings For 44.1Khz Sample Rates

f_in (MHz)	fsamp (kHz)	M	N	P	PLL_M	PLL_N	PLL_N_MOD	PLL_P	f_out (MHz)
11	44.1	11	55.125	5	21	55	4	9	11.025000
11.2896	44.1	8	39.0625	5	15	39	2	9	11.025000
12	44.1	5	22.96875	5	9	22	31	9	11.025000
13	44.1	13	55.125	5	25	55	4	9	11.025000
14.4	44.1	12	45.9375	5	23	45	30	9	11.025000
16.2	44.1	9	30.625	5	17	30	20	9	11.025000
16.8	44.1	17	55.78125	5	33	55	25	9	11.025000
19.2	44.1	16	45.9375	5	31	45	30	9	11.025000
19.44	44.1	13.5	38.28125	5	26	38	9	9	11.025000
19.68	44.1	20.5	45.9375	4	40	45	30	7	11.025000
19.8	44.1	11	30.625	5	21	30	20	9	11.025000

These tables cover the most common applications, obtaining clocks for sample rates such as 22.05kHz and 192kHz should be done by changing the P divider value or the R divider in the clock configuration diagram.

If the user needs to obtain a clock unrelated to those described above, the following method is advised. An example of obtaining 11.2896 from 12.000MHz is shown below.

Choose a small range of P so that the VCO frequency is swept between 45 and 55MHz (or 60-80MHz if VCOFAST is used). Remembering that the P divider can divide by half integers. So for P = 4.0 → 7.0 sweep the M inputs from 2.5 → 24. The most accurate N and N_MOD can be calculated by:

N = FLOOR(((Fout/Fin)*(P*M)),1)

N_MOD = ROUND(32*((((Fout)/Fin)*(P*M)-N),0)

This shows that setting M = 11.5, N = 75 N_MOD = 47 P = 7 gives a comparison frequency of just over 1MHz, a VCO frequency of just under 80MHz (so VCO_FAST must be set) and an output frequency of 11.289596 which gives a sample rate of 44.099985443kHz, or accurate to 0.33 ppm.

Care must be taken when synchronization of isochronous data is not possible, i.e. when the PLL has to be used in the above mode. The I2S should be master on the LM49321 so that the data source can support appropriate SRC as required. This method should only be used with data being read on demand to eliminate sample rate mismatch problems.

Where a system clock exists at an integer multiple of the required DAC clock rate it is preferable to use this rather than the PLL. The LM49321 is designed to work in 8,12,16,24,32, and 48kHz modes from a 12MHz clock without the use of the PLL. This saves power and reduces clock jitter.

DAC Setup Register

This register is used to configure the basic operation of the stereo DAC.

Table 20. DAC_SETUP (0Eh)

<table>
<tr><th>Bits</th><th>Register</th><th colspan="4">Description</th></tr>
<tr><td rowspan="6">1:0</td><td rowspan="6">DAC_MODE</td><td colspan="4">The DAC used in the LM49321 can operate in one of 4 oversampling modes.
The modes are described as follows:</td></tr>
<tr><td>DAC_MODE</td><td>Oversampling Rate</td><td>Typical f_S</td><td>MCLK Required</td></tr>
<tr><td>00</td><td>125</td><td>48KHz</td><td>12.000MHz (USB Mode)</td></tr>
<tr><td>01</td><td>128</td><td>44.1KHz
48KHz</td><td>11.2896MHz
12.288MHz</td></tr>
<tr><td>10</td><td>64</td><td>96KHz</td><td>12.288MHz</td></tr>
<tr><td>11</td><td>32</td><td>192KHz</td><td>24.576MHz</td></tr>
<tr><td>2</td><td>MUTE_L</td><td colspan="4">Mutes the left DAC channel on the next zero crossing.</td></tr>
<tr><td>3</td><td>MUTE_R</td><td colspan="4">Mutes the right DAC channel on the next zero crossing.</td></tr>
<tr><td>4</td><td>DITHER_OFF</td><td colspan="4">If set the dither in DAC is disabled.</td></tr>
<tr><td>5</td><td>DITHER ALWAYS_ON</td><td colspan="4">If set the dither in DAC is enabled all the time.</td></tr>
<tr><td>6</td><td>CUST_COMP</td><td colspan="4">If set the DAC frequency response can be programmed manually via a 5 tap FIR “compensation” filter. This can be used to enhance the frequency response of small loudspeakers or provide a crude tone control. The compensation Coefficients can be set by using registers 10h to 15h.</td></tr>
</table>

Interface Control Register

This register is used to control the I^2S and I^2C compatible interface on the chip.

Table 21. INTERFACE (0Fh)

<table>
<tr><th>Bits</th><th>Field</th><th colspan="2">Description</th></tr>
<tr><td rowspan="4">0</td><td rowspan="4">I2S_MASTER_SLAVE</td><td colspan="2">This enables I^2S in master or slave mode.</td></tr>
<tr><td>I2S_MASTER_SLAVE</td><td>Comments</td></tr>
<tr><td>0</td><td>LM49321 acts as a slave where both I^2S clock and word select are configured as inputs.</td></tr>
<tr><td>1</td><td>LM49321 acts as a master for I^2S, so both I^2S clock and I^2S word select are configured as outputs.</td></tr>
<tr><td rowspan="4">1</td><td rowspan="4">I2S_RESOLUTION</td><td colspan="2">This set the I^2S resolution and affects the I^2S Interface in master mode. In slave mode the I^2S Interface can support any I^2 S compatible resolution. In master mode the I^2S resolution also depends on the DAC mode as the note below explains.</td></tr>
<tr><td>I2S_RESOLUTION</td><td>Comments</td></tr>
<tr><td>0</td><td>I^2S resolution is set to 16 bits.</td></tr>
<tr><td>1</td><td>I^2S resolution is set to 32 bits.</td></tr>
<tr><td rowspan="4">2</td><td rowspan="4">I2S_MODE</td><td colspan="2">This set the I^2S mode timing.</td></tr>
<tr><td>I2S_MODE</td><td>Comments</td></tr>
<tr><td>0</td><td>I^2S interface is configured in normal I^2S mode timing.</td></tr>
<tr><td>1</td><td>I^2S is configured in left justified mode timing.</td></tr>
<tr><td rowspan="4">3</td><td rowspan="4">I2C_FAST</td><td colspan="2">This set the I^2C Clock speed.</td></tr>
<tr><td>I2C_FAST</td><td>Comments</td></tr>
<tr><td>0</td><td>I^2C speed gets its default value of a maximum of 400kHz.</td></tr>
<tr><td>1</td><td>This enables the I^2C to run in fast mode with an I^2C clock up to 3.4MHz.</td></tr>
</table>

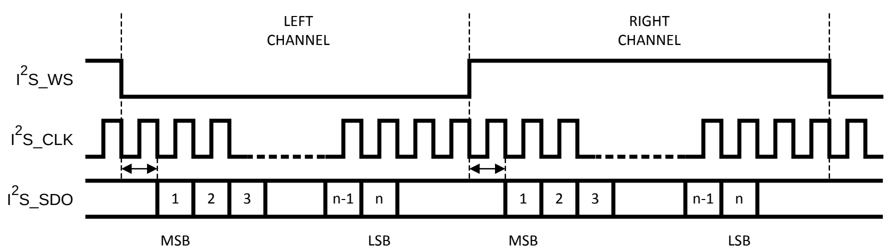


Figure 7. I^2S Mode Timing

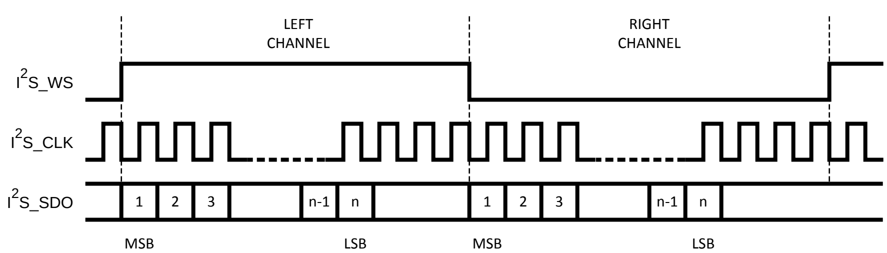


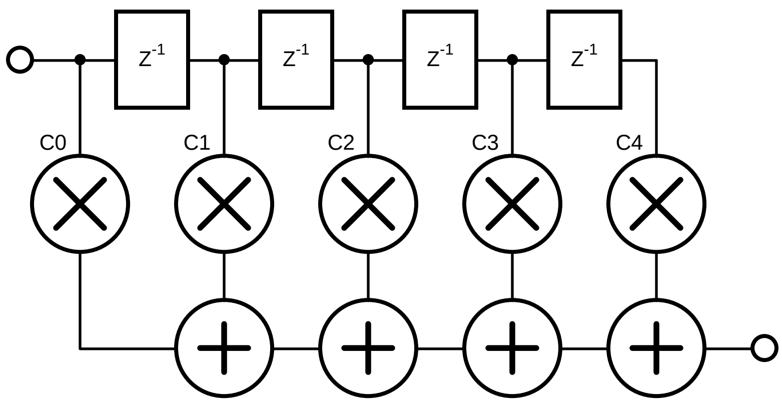
Figure 8. Left Justified Mode Timing

FIR Compensation Filter Configuration Registers

These registers are used to configure the DAC's FIR compensation filter. Three 16 bit coefficients are required and must be programmed via the I2C/SPI Interface in bytes as follows:

Table 22. COMP_COEFF (10h → 15h)

Address	Register	Description
10h	COMP_COEFF0_LSB	Bits [7:0] of the 1st and 5th FIR tap (C0 and C4)
11h	COMP_COEFF0_MSB	Bits [15:8] of the 1st and 5th FIR tap (C0 and C4)
12h	COMP_COEFF1_LSB	Bits [7:0] of the 2nd and 4th FIR tap (C1 and C3)
13h	COMP_COEFF1_MSB	Bits [15:8] of the 2nd and 4th FIR tap (C1 and C3)
14h	COMP_COEFF2_LSB	Bits [7:0] of the 3rd FIR tap (C2)
15h	COMP_COEFF2_MSB	Bits [15:8] of the 3rd FIR tap (C2)



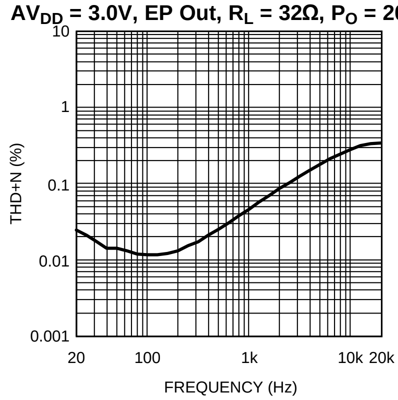
If the CUST_COMP option in register 0Eh is not set the FIR filter will use its default values for a linear response from the DAC into the analog mixer, these values are:

DAC_OSR	C0, C4	C1, C3	C2
00	434	–2291	26984
01, 10, 11	61	–371	25699

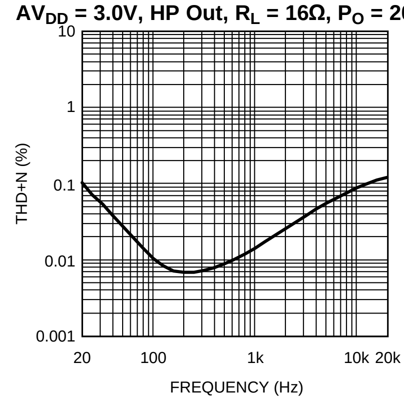
If using 96 or 192kHz data then the custom compensation may be required to obtain flat frequency responses above 24kHz. The total power of any custom filter must not exceed that of the above examples or the filters within the DAC will clip. The coefficient must be programmed in 2's complement.

Typical Performance Characteristics

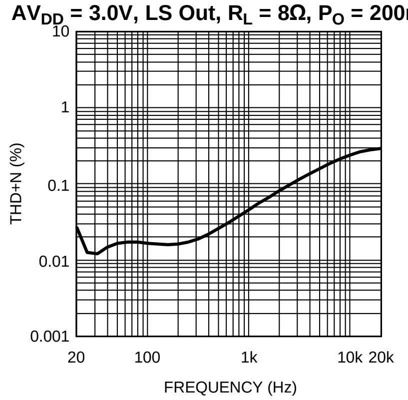
THD+N vs Frequency
AV_{DD} = 3.0V, EP Out, R_L = 32Ω, P_O = 20mW



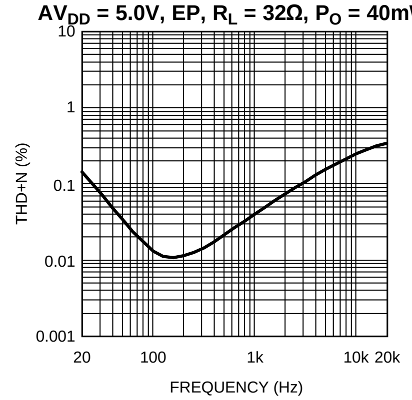
THD+N vs Frequency
AV_{DD} = 3.0V, HP Out, R_L = 16Ω, P_O = 20mW



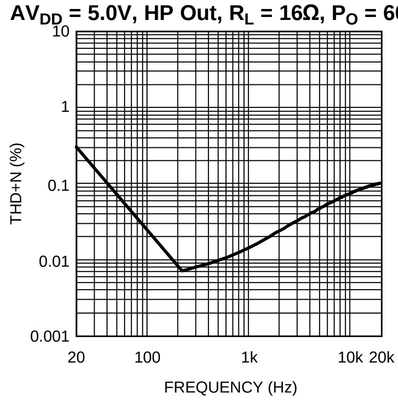
THD+N vs Frequency
AV_{DD} = 3.0V, LS Out, R_L = 8Ω, P_O = 200mW



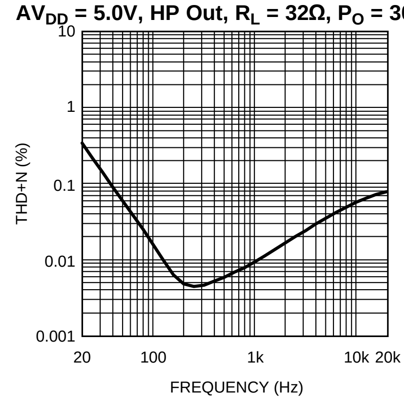
THD+N vs Frequency
AV_{DD} = 5.0V, EP, R_L = 32Ω, P_O = 40mW



THD+N vs Frequency
AV_{DD} = 5.0V, HP Out, R_L = 16Ω, P_O = 60mW

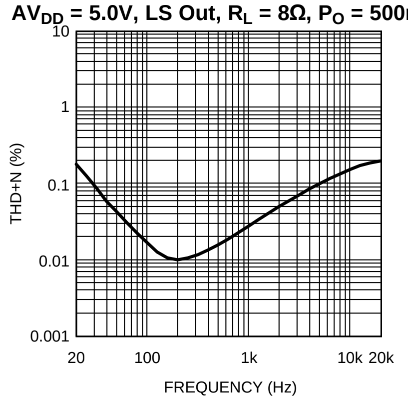


THD+N vs Frequency
AV_{DD} = 5.0V, HP Out, R_L = 32Ω, P_O = 30mW

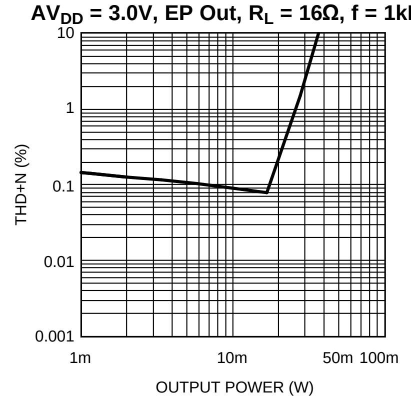


Typical Performance Characteristics (continued)

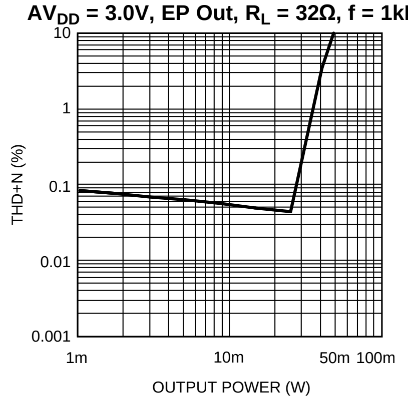
THD+N vs Frequency
AV_{DD} = 5.0V, LS Out, R_L = 8Ω, P_O = 500mW



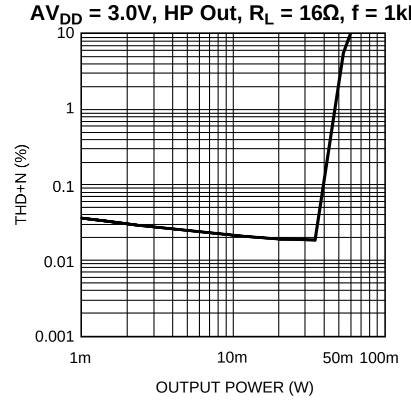
THD+N vs Output Power
AV_{DD} = 3.0V, EP Out, R_L = 16Ω, f = 1kHz



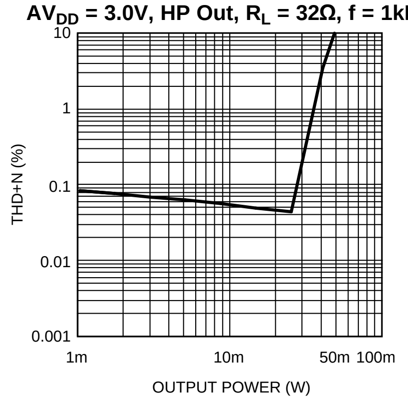
THD+N vs Output Power
AV_{DD} = 3.0V, EP Out, R_L = 32Ω, f = 1kHz



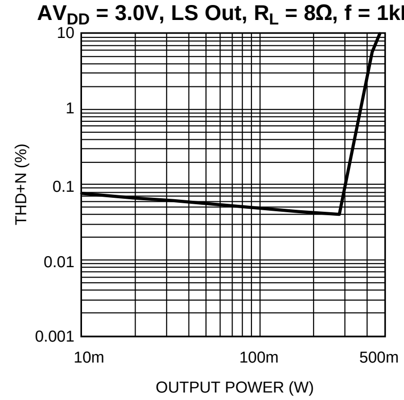
THD+N vs Output Power
AV_{DD} = 3.0V, HP Out, R_L = 16Ω, f = 1kHz



THD+N vs Output Power
AV_{DD} = 3.0V, HP Out, R_L = 32Ω, f = 1kHz

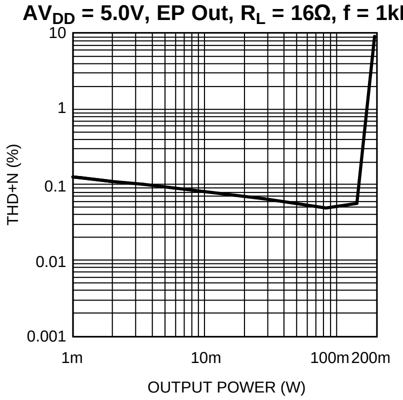


THD+N vs Output Power
AV_{DD} = 3.0V, LS Out, R_L = 8Ω, f = 1kHz

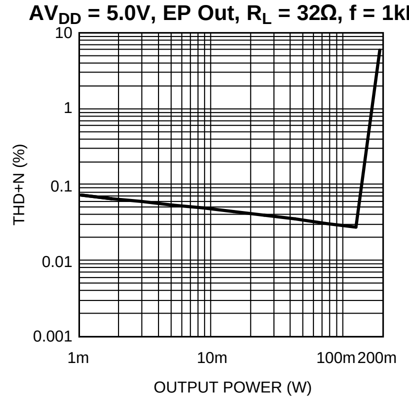


Typical Performance Characteristics (continued)

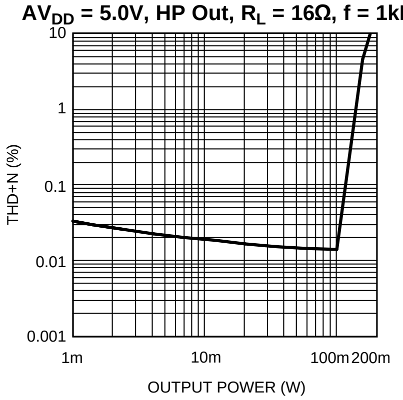
THD+N vs Output Power
AV_{DD} = 5.0V, EP Out, R_L = 16Ω, f = 1kHz



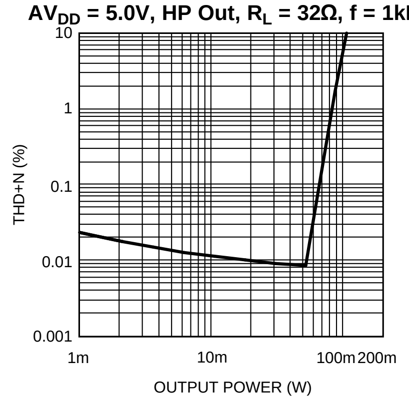
THD+N vs Output Power
AV_{DD} = 5.0V, EP Out, R_L = 32Ω, f = 1kHz



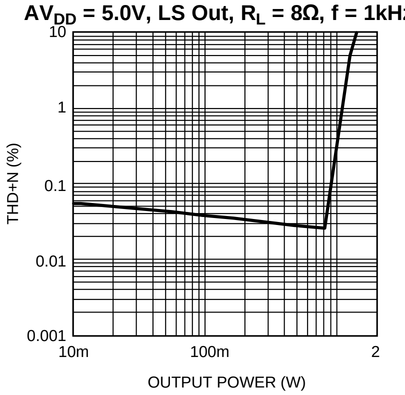
THD+N vs Output Power
AV_{DD} = 5.0V, HP Out, R_L = 16Ω, f = 1kHz



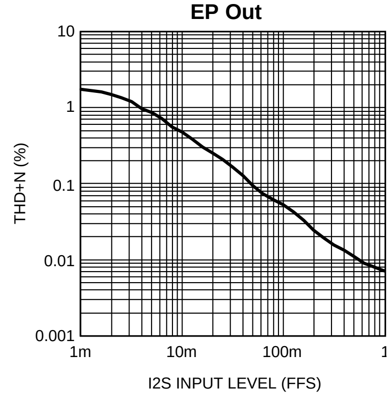
THD+N vs Output Power
AV_{DD} = 5.0V, HP Out, R_L = 32Ω, f = 1kHz



THD+N vs Output Power
AV_{DD} = 5.0V, LS Out, R_L = 8Ω, f = 1kHz

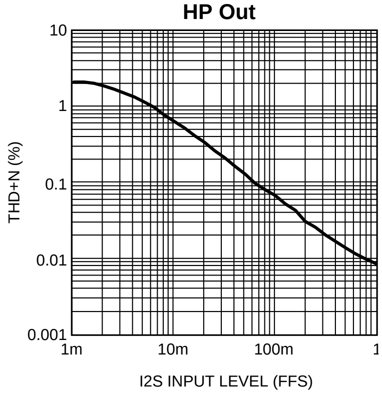


THD+N vs I^2S Level
EP Out

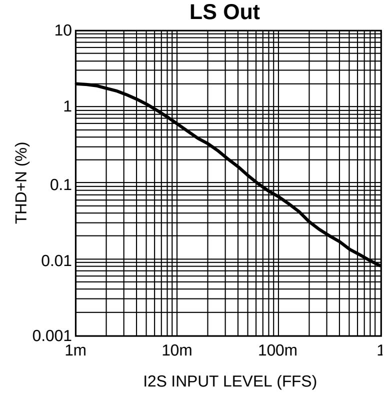


Typical Performance Characteristics (continued)

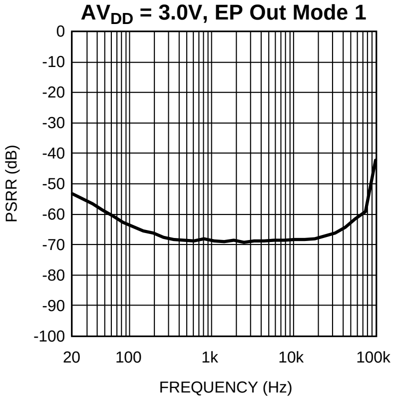
THD+N vs I^2S Level HP Out



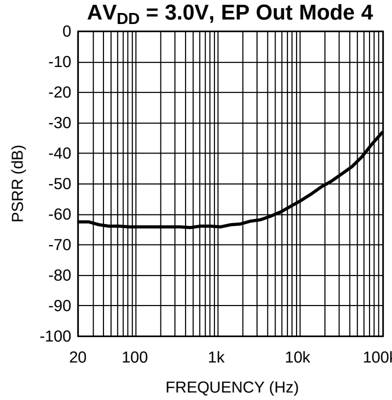
THD+N vs I^2S Level LS Out



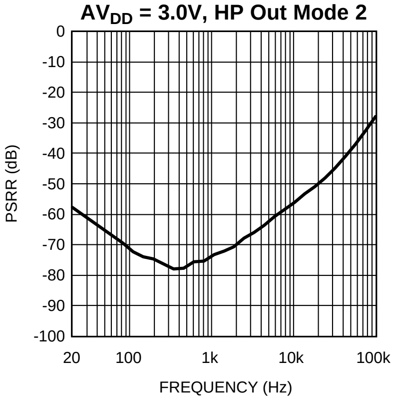
PSRR vs Frequency AV_{DD} = 3.0V, EP Out Mode 1



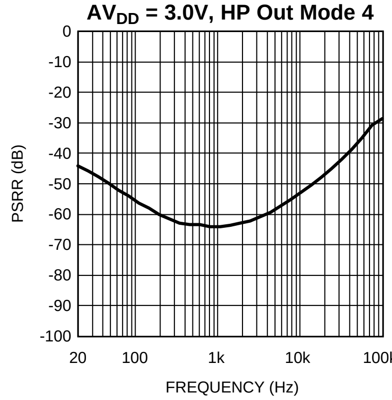
PSRR vs Frequency AV_{DD} = 3.0V, EP Out Mode 4



PSRR vs Frequency AV_{DD} = 3.0V, HP Out Mode 2

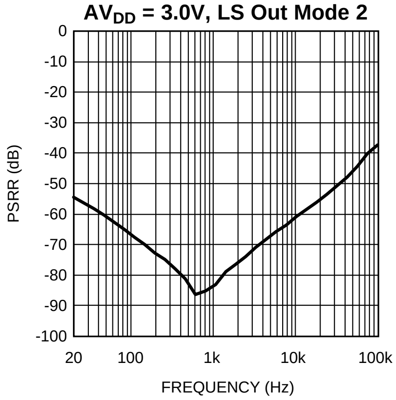


PSRR vs Frequency AV_{DD} = 3.0V, HP Out Mode 4

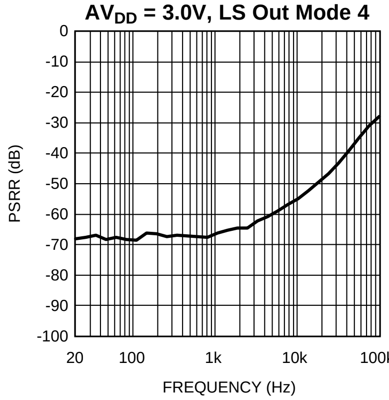


Typical Performance Characteristics (continued)

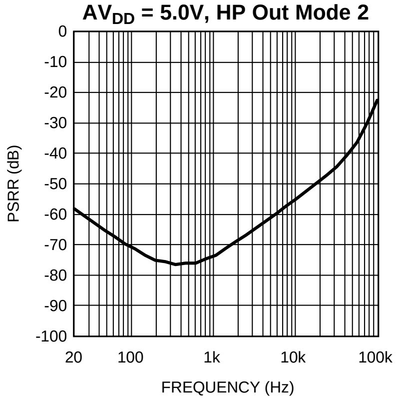
PSRR vs Frequency AV_{DD} = 3.0V, LS Out Mode 2



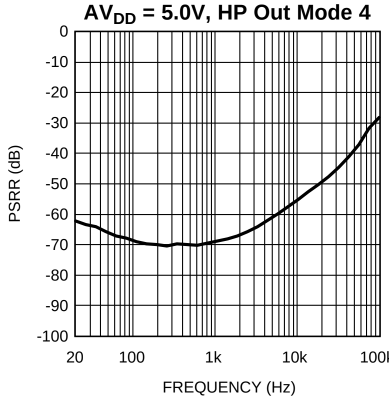
PSRR vs Frequency AV_{DD} = 3.0V, LS Out Mode 4



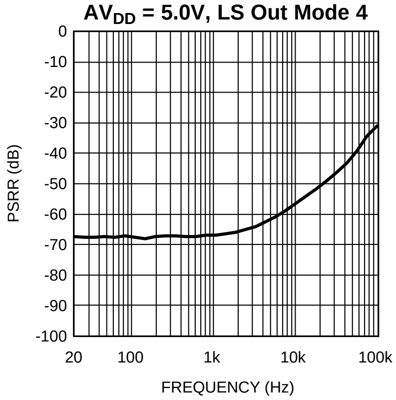
PSRR vs Frequency AV_{DD} = 5.0V, HP Out Mode 2



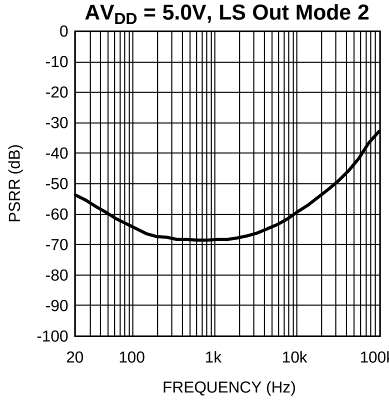
PSRR vs Frequency AV_{DD} = 5.0V, HP Out Mode 4



PSRR vs Frequency AV_{DD} = 5.0V, LS Out Mode 4

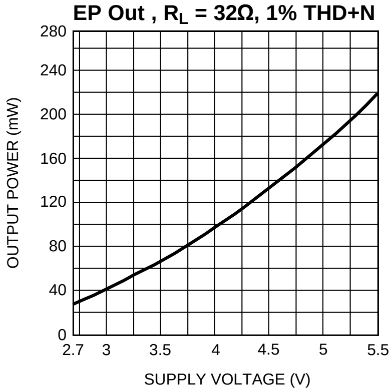


PSRR vs Frequency AV_{DD} = 5.0V, LS Out Mode 2

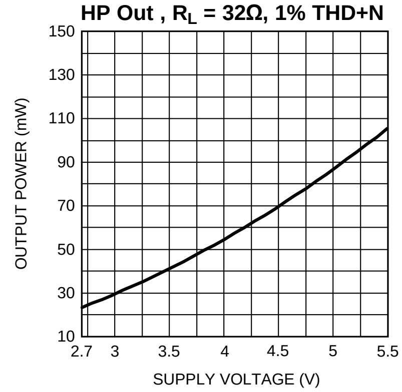


Typical Performance Characteristics (continued)

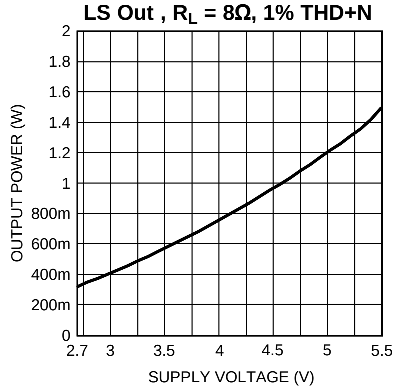
Output Power vs Supply Voltage EP Out , R_L = 32Ω, 1% THD+N



Output Power vs Supply Voltage HP Out , R_L = 32Ω, 1% THD+N



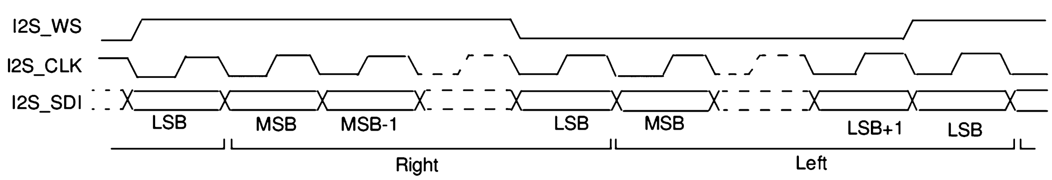
Output Power vs Supply Voltage LS Out , R_L = 8Ω, 1% THD+N



Application Information

I²S

The LM49321 supports both master and slave I²S transmission at either 16 or 32 bits per word at clock rates up to 3.072MHz (48kHz stereo, 32bit). The basic format is shown below:



MONO ONLY SETTING

The LM49321 may be restricted to mono amplification only by setting MONO_ONLY in Output Control register 0x01h to 1. This may save an additional 400μA from I_{DD}.

LM49321 DEMOBOARD OPERATION

BOARD LAYOUT

DIGITAL SUPPLIES

JP14 — Digital Power DVDD

JP10 — I/O Power IOVDD

JP13 — PLL Supply PLLVDD

JP16 — USB Board Supply BBVDD

JP15 — I^2CVDD

All supplies may be set independently. All digital ground is common. Jumpers may be used to connect all the digital supplies together.

S9 – connects VDD_PLL to VDD_D

S10 – connects VDD_D to VDD_IO

S11 – connects VDD_IO to VDD_I2C

S12 – connects VDD_I2C to Analog VDD

S17 – connects BB_VDD to USB3.3V (from USB board)

S19 – connects VDD_D to USB3.3V (from USB board)

S20 – connects VDD_D to SPDIF receiver chip

ANALOG SUPPLY

JP11 — Analog Supply

S12 — connects Analog VDD with Digital VDD (I2C_VDD)

S16 — connects Analog Ground with Digital Ground

S21 — connects Analog VDD to SPDIF receiver chip

INPUTS

Analog Inputs

JP2 — Mono Differential Input

JP6 — Left Input

JP7 — Right Input

Digital Inputs

JP19 — Digital Interface

Pin 1 — MCLK

Pin 2 — I2S_CLK

Pin 3 — I2S_SDI

Pin 4 — I^2S_WS

JP20 — Toslink SPDIF Input

JP21 — Coaxial SPDIF Input

Coaxial and Toslink inputs may be toggled between by use of S25. Only one may be used at a time. Must be used in conjunction with on-board SPDIF receiver chip.

OUTPUTS

JP5 — BTL Loudspeaker Output

JP1 — Left Headphone Output (Single-Ended or OCL)

JP3 — Right Headphone Output (Single-Ended or OCL)

P1 — Stereo Headphone Jack (Same as JP1, JP2, Single-Ended or OCL)

JP12 — Mono BTL Earpiece Output

CONTROL INTERFACE

X1, X2 – USB Control Bus for I^2C/SPI

X1

Pin 9 – Mode Select (SPI or I^2C)

X2

Pin 1 – SDA

Pin 3 – SCL

Pin 15 – ADDR/END

Pin 14 – USB5V

Pin 16 – USB3.3V

Pin 16 – USB GND

MISCELLANEOUS

I^2S BUS SELECT

S23, S24, S26, S27 – I^2S Bus select. Toggles between on-board and external I^2S (whether on-board SPDIF receiver is used). All jumpers must be set the same. Jumpers on top two pins selects external bus (JP19). Jumpers on bottom two pins selects on-board SPDIF receiver output.

HEADPHONE OUTPUT CONFIGURATION

Jumpers S1, S2, S3, and S4 are used to configure the headphone outputs for either cap-coupled outputs or output capacitorless (OCL) mode in addition to the register control internal to the LM49321 for this feature. Jumpers S1 and S3 bypass the output DC blocking capacitors when OCL mode is required. S2 connects the center amplifier HPCOUT to the headphone ring when in OCL mode. S4 connects the center ring to GND when cap-coupled mode is desired. S4 must be removed for OCL mode to function properly. Jumper settings for each mode:

OCL

S1 = ON

S2 = ON

S3 = ON

S4 = OFF

Cap-Coupled

S1 = OFF

S2 = OFF

S3 = OFF

S4 = ON

PLL FILTER CONFIGURATION

The LM49321 demo board comes with a simple filter setup by connecting jumpers S5 and S6. Removing these and connecting jumpers S7 and S8 will allow for an alternate PLL filter configuration to be used at R2 and C23.

ON-BOARD SPDIF RECEIVER

The SPDIF receiver present on the LM49321 demo board allows quick demonstration of the capabilities of the LM49321 by using the common SPDIF output found on most CD/DVD players today. There are some limitations in its useage, as the receiver will not work with digital supplies of less than 3.0V and analog supplies of less than 4V. This means low analog supply voltage testing of the LM49321 must be done on the external digital bus.

The choice of using on-board or external digital bus is made usign jumpers S23, S24, S26, and S27 as described above.

S25 selects whether the Toslink or Coaxial SPDIF input is used. The top two pins connects the toslink, the bottom two connect the coaxial input.

Power on the digital side is routed through S20 (connecting to the other digital supplies), while on the analog side it is interrupted by S21. Both jumpers must be in place for the receiver to function. The part is already configured for I^2S standard outputs. Jumper S28 allows the DATA output to be pulled either high or low. Default is high (jumper on right two pins).

It may be necessary to quickly toggle S29 to reset the receiver and start it working upon initial power up. A quick short across S29 should clear this condition.

LM49321 I^2C/SPI INTERFACE SOFTWARE

Convenient graphical user interface software is available for demonstration purposes of the LM49321. It allows for either SPI or I^2C control via either USB or parallel port connections to a Windows computer. Control options include all mode and output settings, volume controls, PLL and DAC setup, FIR setting and on-the-fly adjustment by an easy to use graphical interface. An advanced option is also present to allow direct, register-level commands. Software is available from www.national.com and is compatible with Windows operating systems of Windows 98 or more (with USB support) with the latest .NET updates from Microsoft.

Demonstration Board Schematic

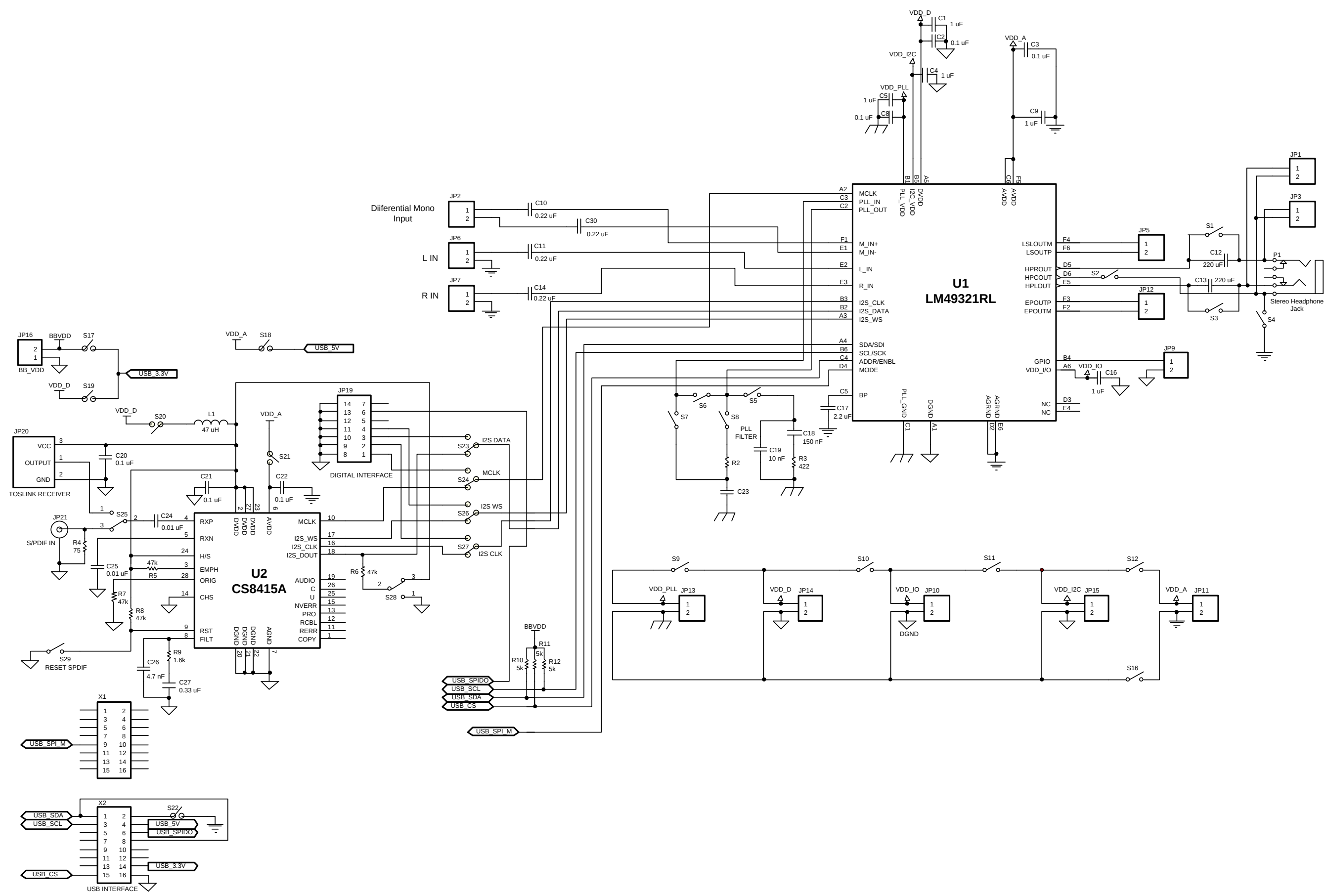


Figure 9. Complete Board Schematic

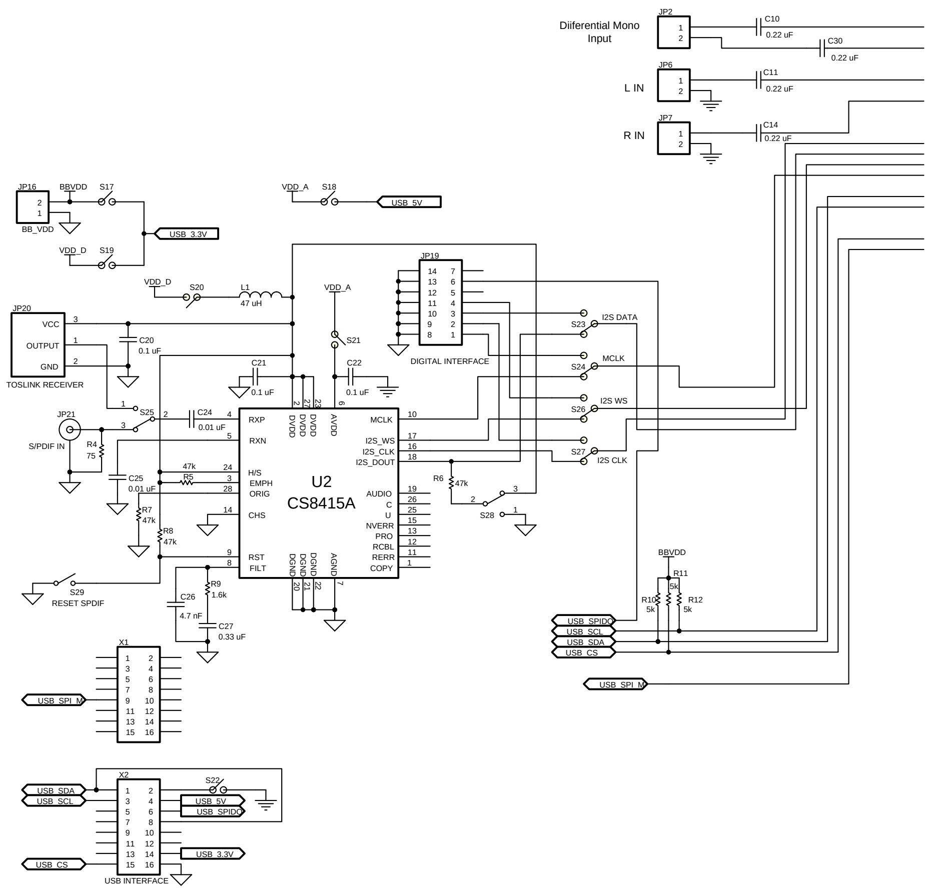


Figure 10. Enlarged Board Schematic Part 1 of 2

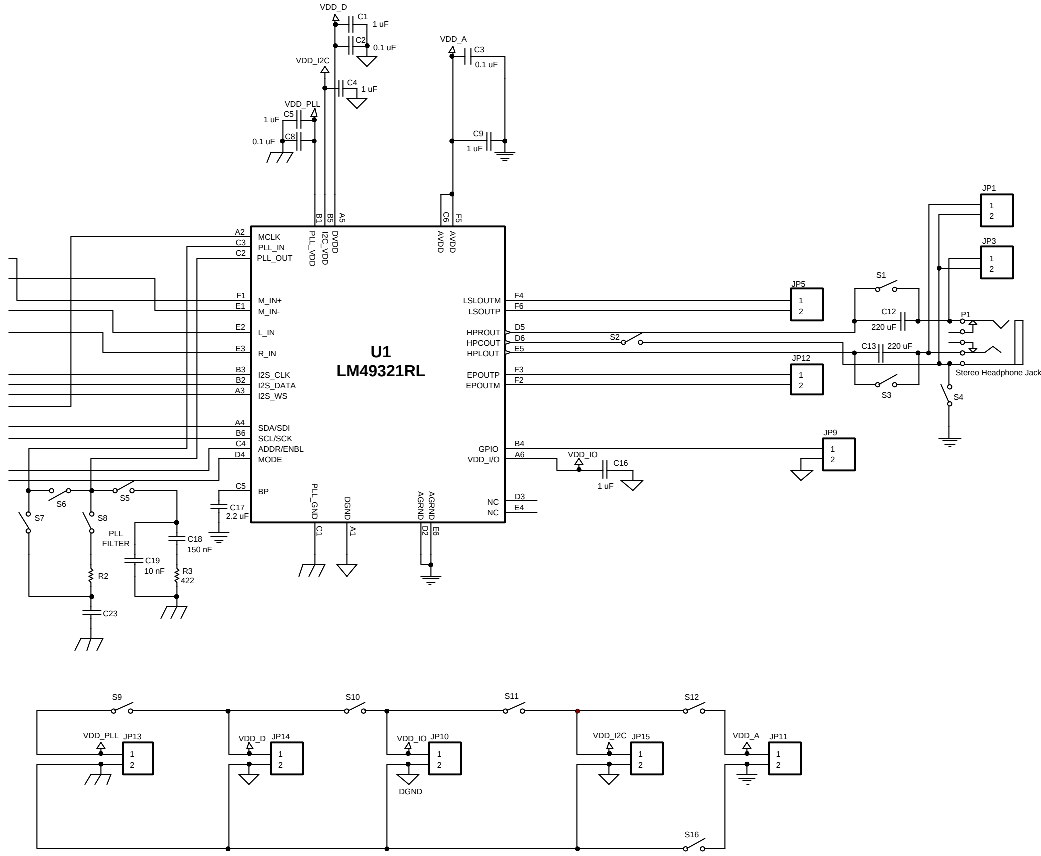


Figure 11. Enlarged Board Schematic Part 2 of 2

Revision History

Rev	Date	Description
1.0	09/10/08	Initial release.
1.01	09/23/08	Text edits.
1.02	08/31/09	Edited the package drawing and the top markings.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
LM49321RL/NOPB	ACTIVE	DSBGA	YPG	36	250	Green (RoHS & no Sb/Br)	SNAG	Level-1-260C-UNLIM	
LM49321RLX/NOPB	ACTIVE	DSBGA	YPG	36	1000	Green (RoHS & no Sb/Br)	SNAG	Level-1-260C-UNLIM	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

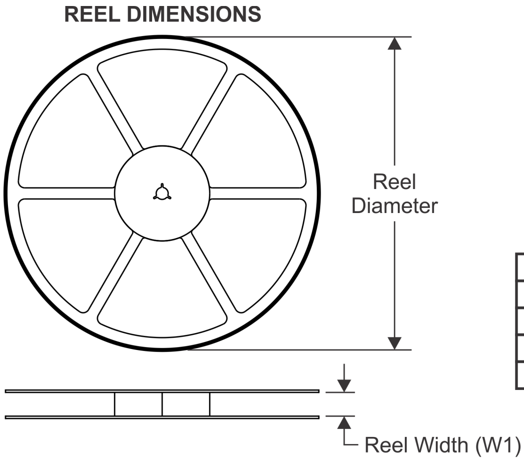
(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

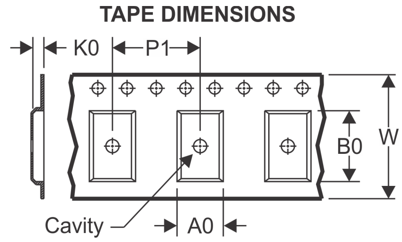
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

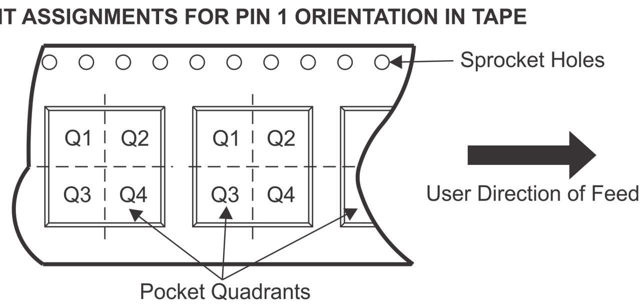
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION





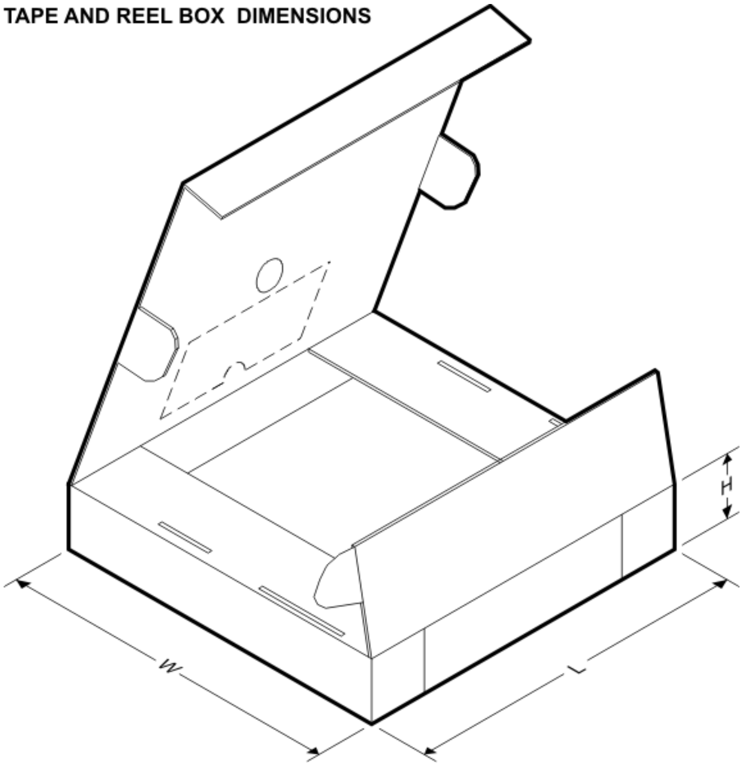
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers



*All dimensions are nominal

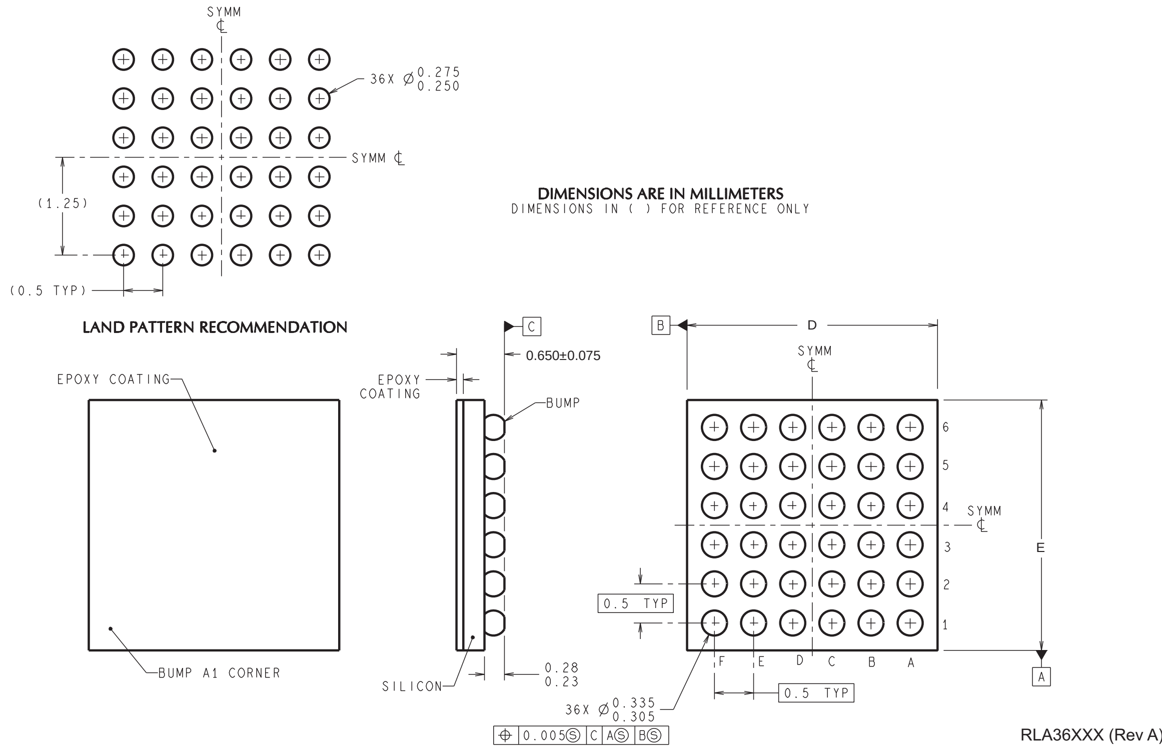
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM49321RL/NOPB	DSBGA	YPG	36	250	178.0	12.4	3.43	3.59	0.76	8.0	12.0	Q1
LM49321RLX/NOPB	DSBGA	YPG	36	1000	178.0	12.4	3.43	3.59	0.76	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM49321RL/NOPB	DSBGA	YPG	36	250	203.0	190.0	41.0
LM49321RLX/NOPB	DSBGA	YPG	36	1000	206.0	191.0	90.0



D: Max = 3.545 mm, Min =3.445 mm

E: Max = 3.288 mm, Min =3.188 mm

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NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.