LM5018 100V, 300mA Constant On-Time Synchronous Buck Regulator

Check for Samples: LM5018

FEATURES

- **Wide 9V to 100V Input Range**
- **Integrated 100V, High and Low Side Switches**
- **No Schottky Required**
- **Constant On-time Control**
- **No Loop Compensation Required**
- **Ultra-Fast Transient Response**
- **Nearly Constant Operating Frequency**
- **Intelligent Peak Current Limit**
- **Adjustable Output Voltage from 1.225V**
- **Precision 2% Feedback Reference**
- **Frequency Adjustable to 1MHz**
- **Adjustable Undervoltage Lockout**
- **Remote Shutdown**
- **Thermal Shutdown**

APPLICATIONS

- **Smart Power Meters**
- **Telecommunication Systems**
- **Automotive Electronics**
- **Isolated Bias Supply**

DESCRIPTION

The LM5018 is a 100V, 300mA synchronous step-down regulator with integrated high side and low side MOSFETs. The constant-on-time (COT) control scheme employed in the LM5018 requires no loop compensation, provides excellent transient response, and enables very low step-down ratios. The on-time varies inversely with the input voltage resulting in nearly constant frequency over the input voltage range. A high voltage startup regulator provides bias power for internal operation of the IC and for integrated gate drivers.

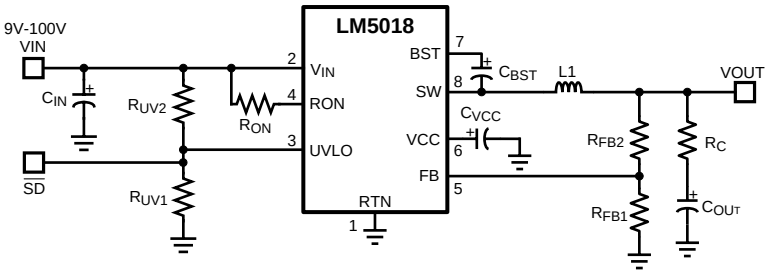
A peak current limit circuit protects against overload conditions. The undervoltage lockout (UVLO) circuit allows the input undervoltage threshold and hysteresis to be independently programmed. Other protection features include thermal shutdown and bias supply undervoltage lockout.

The LM5018 is available in LLP-8 and PSOP-8 plastic packages.

Packages

- LLP-8
- PSOP-8

Typical Application



Connection Diagram

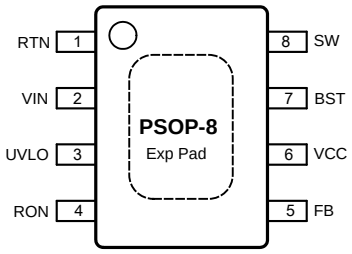


Figure 1. Top View (Connect Exposed Pad to RTN)

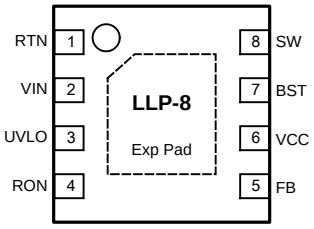


Figure 2. Top View (Connect Exposed Pad to RTN)

Pin Functions

Pin Descriptions

Pin	Name	Description	Application Information
1	RTN	Ground	Ground connection of the integrated circuit.
2	V_{IN}	Input Voltage	Operating input range is 9V to 100V.
3	UVLO	Input Pin of Undervoltage Comparator	Resistor divider from V_{IN} to UVLO to GND programs the undervoltage detection threshold. An internal current source is enabled when UVLO is above 1.225V to provide hysteresis. When UVLO pin is pulled below 0.66V externally, the parts goes in shutdown mode.
4	R_{ON}	On-Time Control	A resistor between this pin and V_{IN} sets the switch on-time as a function of V_{IN}. Minimum recommended on-time is 100ns at max input voltage.
5	FB	Feedback	This pin is connected to the inverting input of the internal regulation comparator. The regulation level is 1.225V.
6	V_{CC}	Output From the Internal High Voltage Series Pass Regulator. Regulated at 7.6V	The internal V_{CC} regulator provides bias supply for the gate drivers and other internal circuitry. A 1.0µF decoupling capacitor is recommended.
7	BST	Bootstrap Capacitor	An external capacitor is required between the BST and SW pins (0.01µF ceramic). The BST pin capacitor is charged by the V_{CC} regulator through an internal diode when the SW pin is low.
8	SW	Switching Node	Power switching node. Connect to the output inductor and bootstrap capacitor.
	EP	Exposed Pad	Exposed pad must be connected to RTN pin. Connect to system ground plane on application board for reduced thermal resistance.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings (1)

V_{IN}, UVLO to RTN	-0.3V to 100V
SW to RTN	-1.5V to V_{IN} +0.3V
BST to V_{CC}	100V
BST to SW	13V
R_{ON} to RTN	-0.3V to 100V
V_{CC} to RTN	-0.3V to 13V
FB to RTN	-0.3V to 5V
ESD Rating (Human Body Model (2)	2kV
Lead Temperature (3)	200°C
Storage Temperature Range	-55°C to +150°C

(1) Absolute Maximum Ratings are limits beyond which damage to the device may occur. Operating Ratings are conditions under which operation of the device is intended to be functional. For guaranteed specifications and test conditions, see the Electrical Characteristics. The RTN pin is the GND reference electrically connected to the substrate.
(2) The human body model is a 100pF capacitor discharged through a 1.5kΩ resistor into each pin.
(3) For detailed information on soldering plastic PSOP package, refer to the Packaging Data Book available from National Semiconductor Corporation. Max solder time not to exceed 4 seconds.

Operating Ratings (1)

V_{IN} Voltage	9V to 100V
Operating Junction Temperature	−40°C to +125°C

(1) Absolute Maximum Ratings are limits beyond which damage to the device may occur. Operating Ratings are conditions under which operation of the device is intended to be functional. For guaranteed specifications and test conditions, see the Electrical Characteristics. The RTN pin is the GND reference electrically connected to the substrate.

Electrical Characteristics

Specifications with standard typeface are for T_J = 25°C, and those with **boldface** type apply over full Operating Junction Temperature range. V_{IN} = 48V, unless otherwise stated. See (1).

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{CC} Supply						
V_{CC} Reg	V_{CC} Regulator Output	V_{IN} = 48V, I_{CC} = 20mA	**6.25**	7.6	**8.55**	V
	V_{CC} Current Limit	V_{IN} = 48V(2)	**26**			mA
	V_{CC} Undervoltage Lockout Voltage (V_{CC} Increasing)		**4.15**	4.5	**4.9**	V
	V_{CC} Undervoltage Hysteresis			300		mV
	V_{CC} Drop Out Voltage	V_{IN} = 9V, I_{CC} = 20mA		2.3		V
	I_{IN} Operating Current	Non-Switching, FB = 3V		1.75		mA
	I_{IN} Shutdown Current	UVLO = 0V		50	**225**	µA
Switch Characteristics						
	Buck Switch $R_{DS(ON)}$	I_{TEST} = 200mA, BST-SW = 7V		0.8	**1.8**	Ω
	Synchronous $R_{DS(ON)}$	I_{TEST} = 200mA		0.45	**1**	Ω
	Gate Drive UVLO	$V_{BST} - V_{SW}$ Rising	**2.4**	3	**3.6**	V
	Gate Drive UVLO Hysteresis			260		mV
Current Limit						
	Current Limit Threshold		**350**	575	**700**	mA
	Current Limit Response Time	Time to Switch Off		150		ns
	Off-Time Generator (Test 1)	FB = 0.1V, V_{IN} = 48V		12		µs
	Off-Time Generator (Test 2)	FB = 1V, V_{IN} = 48V		2.5		µs
On-Time Generator						
	T_{ON} Test 1	V_{IN} = 32V, R_{ON} = 100k	**270**	350	**460**	ns
	T_{ON} Test 2	V_{IN} = 48V, R_{ON} = 100k	**188**	250	**336**	ns
	T_{ON} Test 3	V_{IN} = 75V, R_{ON} = 250k	**250**	370	**500**	ns
	T_{ON} Test 4	V_{IN} = 10V, R_{ON} = 250k	**1880**	3200	**4425**	ns
Minimum Off-Time						
	Minimum Off-Timer	FB = 0V		144		ns
Regulation and Overvoltage Comparators						
	FB Regulation Level	Internal reference trip point for switch ON	**1.2**	1.225	**1.25**	V
	FB Overvoltage Threshold	Trip point for switch OFF		1.62		V
	FB Bias Current			60		nA
Undervoltage Sensing Function						
	UV Threshold	UV Rising	**1.19**	1.225	**1.26**	V
	UV Hysteresis Input Current	UV = 2.5V	**-10**	-20	**–29**	µA
	Remote Shutdown Threshold	Voltage at UVLO Falling	**0.32**	0.66		V
	Remote Shutdown Hysteresis			110		mV
Thermal Shutdown						
Tsd	Thermal Shutdown Temp.			165		°C
	Thermal Shutdown Hysteresis			20		°C
Thermal Resistance						
θ_{JA}	Junction to Ambient	PSOP-8		40		°C/W
		LLP-8		40		°C/W

(1) All limits are guaranteed by design. All electrical characteristics having room temperature limits are tested during production at T_A = 25°C. All hot and cold limits are guaranteed by correlating the electrical characteristics to process and temperature variations and applying statistical process control.

(2) V_{CC} provides self bias for the internal gate drive and control circuits. Device thermal limitations limit external loading.

Typical Performance Characteristics

Figure 3. Efficiency at 240kHz, 10V

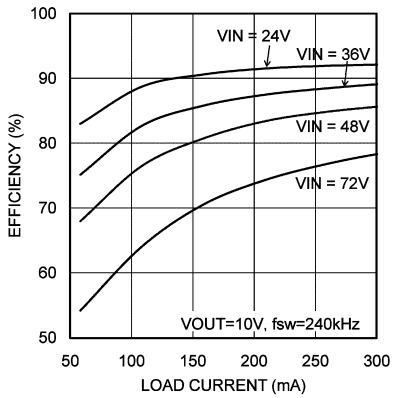


Figure 4. V_{CC} vs V_{IN}

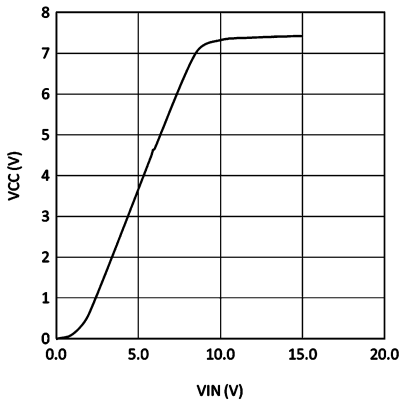
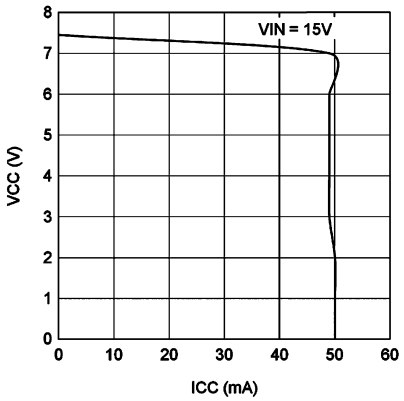


Figure 5. V_{CC} vs I_{CC}



Typical Performance Characteristics (continued)

Figure 6. I_{CC} vs External V_{CC}

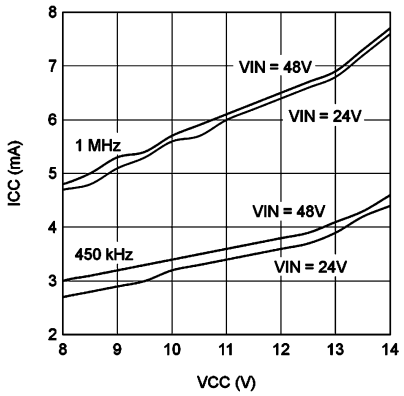


Figure 7. T_{ON} vs V_{IN} and R_{ON}

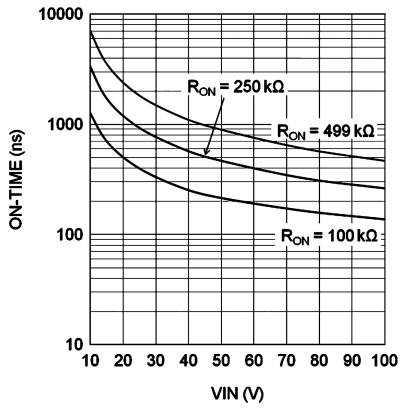
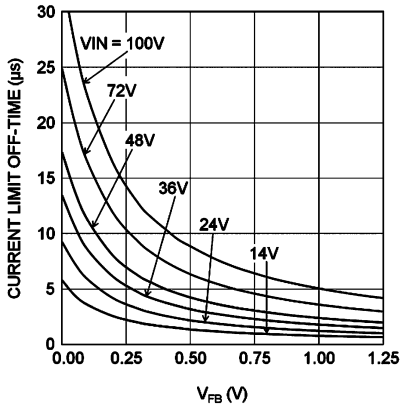


Figure 8. T_{OFF} (I_{LIM}) vs V_{FB} and V_{IN}



Typical Performance Characteristics (continued)

Figure 9. I_{IN} vs V_{IN} (Operating, Non Switching)

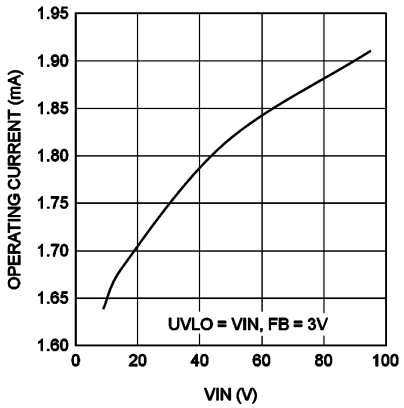


Figure 10. I_{IN} vs V_{IN} (Shutdown)

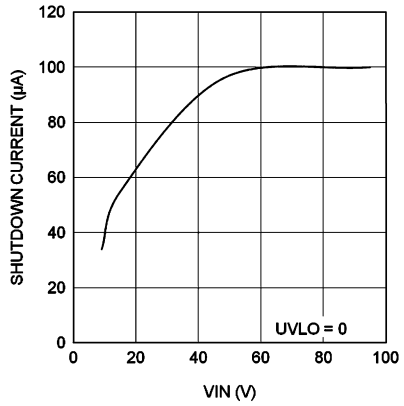
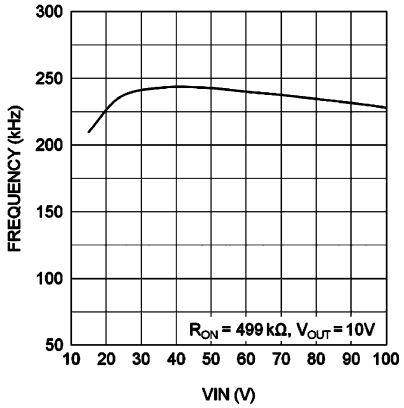


Figure 11. Switching Frequency vs V_{IN}



Block Diagram

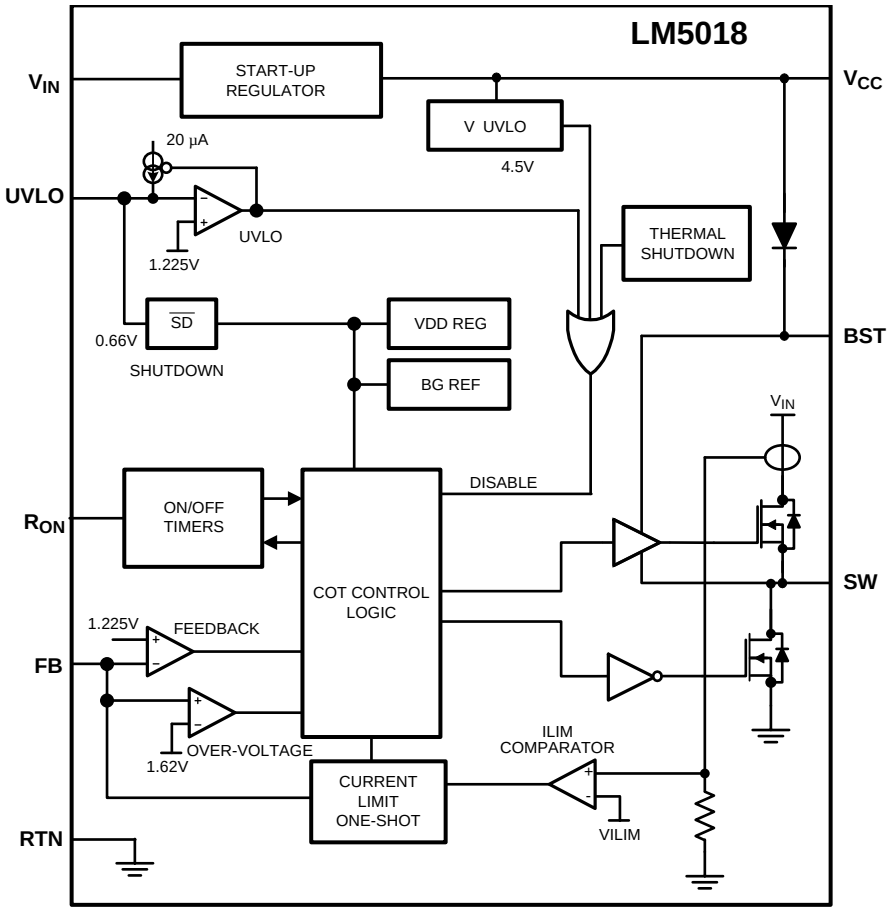


Figure 12. Functional Block Diagram

Functional Description

The LM5018 step-down switching regulator features all the functions needed to implement a low cost, efficient, buck converter capable of supplying up to 300mA to the load. This high voltage regulator contains 100V, N-channel buck and synchronous switches, is easy to implement, and is provided in thermally enhanced PSOP-8 and LLP-8 packages. The regulator operation is based on a constant on-time control scheme using an on-time inversely proportional to V_{IN}. This control scheme does not require loop compensation. The current limit is implemented with a forced off-time inversely proportional to V_{OUT}. This scheme ensures short circuit protection while providing minimum foldback. The simplified block diagram of the LM5018 is shown in Figure 12, Functional Block Diagram.

The LM5018 can be applied in numerous applications to efficiently regulate down higher voltages. This regulator is well suited for 48V telecom and 42V automotive power bus ranges. Protection features include: thermal shutdown, undervoltage lockout, minimum forced off-time, and an intelligent current limit.

Control Overview

The LM5018 buck regulator employs a control principle based on a comparator and a one-shot on-timer, with the output voltage feedback (FB) compared to an internal reference (1.225V). If the FB voltage is below the reference the internal buck switch is turned on for the one-shot timer period, which is a function of the input voltage and the programming resistor (R_{ON}). Following the on-time the switch remains off until the FB voltage falls below the reference, but never before the minimum off-time forced by the minimum off-time one-shot timer. When the FB pin voltage falls below the reference and the minimum off-time one-shot period expires, the buck switch is turned on for another on-time one-shot period. This will continue until regulation is achieved and the FB voltage is approximately equal to 1.225V (typ).

In a synchronous buck converter, the low side (sync) FET is 'on' when the high side (buck) FET is 'off.' The inductor current ramps up when the high side switch is ‘on’ and ramps down when the high side switch is ‘off’. There is no diode emulation feature in this IC, and therefore, the inductor current may ramp in the negative direction at light load. This causes the converter to operate in continuous conduction mode (CCM) regardless of the output loading. The operating frequency remains relatively constant with load and line variations. The operating frequency can be calculated as follows:

$$f_{SW} = \frac{V_{OUT}}{10^{-10} \times R_{ON}} \quad (1)$$

The output voltage (V_{OUT}) is set by two external resistors (R_{FB1}, R_{FB2}). The regulated output voltage is calculated as follows:

$$V_{OUT} = 1.225V \times \frac{R_{FB2} + R_{FB1}}{R_{FB1}} \quad (2)$$

$$\frac{R_{FB2}}{R_{FB1}} = \frac{V_{OUT} - 1.225V}{1.225V} \quad (3)$$

This regulator regulates the output voltage based on ripple voltage at the feedback input, requiring a minimum amount of ESR for the output capacitor (C_{OUT}). A minimum of 25mV of ripple voltage at the feedback pin (FB) is required for the LM5018. In cases where the capacitor ESR is too small, additional series resistance may be required (R_C in Figure 13 Low Ripple Output Configuration).

For applications where lower output voltage ripple is required the output can be taken directly from a low ESR output capacitor, as shown in Figure 13 Low Ripple Output Configuration. However, R_C slightly degrades the load regulation.

V_{CC} Regulator

The LM5018 contains an internal high voltage linear regulator with a nominal output of 7.6V. The input pin (V_{IN}) can be connected directly to the line voltages up to 100V. The V_{CC} regulator is internally current limited to 30mA. The regulator sources current into the external capacitor at V_{CC}. This regulator supplies current to internal circuit blocks including the synchronous MOSFET driver and the logic circuits. When the voltage on the V_{CC} pin reaches the undervoltage lockout threshold of 4.5V, the IC is enabled.

The V_{CC} regulator contains an internal diode connection to the BST pin to replenish the charge in the gate drive boot capacitor when SW pin is low.

At high input voltages, the power dissipated in the high voltage regulator is significant and can limit the overall achievable output power. As an example, with the input at 48V and switching at high frequency, the V_{CC} regulator may supply up to 7mA of current resulting in 48V x 7mA = 336mW of power dissipation. If the V_{CC} voltage is driven externally by an alternate voltage source, between 8V and 13V, the internal regulator is disabled. This reduces the power dissipation in the IC.

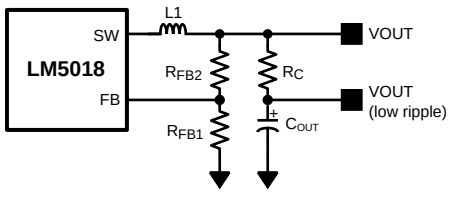


Figure 13. Low Ripple Output Configuration

Regulation Comparator

The feedback voltage at FB is compared to an internal 1.225V reference. In normal operation, when the output voltage is in regulation, an on-time period is initiated when the voltage at FB falls below 1.225V. The high side switch will stay on for the on-time, causing the FB voltage to rise above 1.225V. After the on-time period, the high side switch will stay off until the FB voltage again falls below 1.225V. During start-up, the FB voltage will be below 1.225V at the end of each on-time, causing the high side switch to turn on immediately after the minimum forced off-time of 144ns. The high side switch can be turned off before the on-time is over, if the peak current in the inductor reaches the current limit threshold.

Overvoltage Comparator

The feedback voltage at FB is compared to an internal 1.62V reference. If the voltage at FB rises above 1.62V the on-time pulse is immediately terminated. This condition can occur if the input voltage and/or the output load changes suddenly. The high side switch will not turn on again until the voltage at FB falls below 1.225V.

On-Time Generator

The on-time for the LM5018 is determined by the R_{ON} resistor, and is inversely proportional to the input voltage (V_{IN}), resulting in a nearly constant frequency as V_{IN} is varied over its range. The on-time equation for the LM5018 is:

$$T_{ON} = \frac{10^{-10} \times R_{ON}}{V_{IN}} \quad (4)$$

See figure "T_{ON} vs V_{IN} and R_{ON}" in the section "Performance Curves." R_{ON} should be selected for a minimum on-time (at maximum V_{IN}) greater than 100ns, for proper operation. This requirement limits the maximum switching frequency for high V_{IN}.

Current Limit

The LM5018 contains an intelligent current limit off-timer. If the current in the buck switch exceeds 575mA the present cycle is immediately terminated, and a non-resetable off-timer is initiated. The length of off-time is controlled by the FB voltage and the input voltage V_{IN}. As an example, when FB = 0V and V_{IN} = 48V, the maximum off-time is set to 16µs. This condition occurs when the output is shorted, and during the initial part of start-up. This amount of time ensures safe short circuit operation up to the maximum input voltage of 100V.

In cases of overload where the FB voltage is above zero volts (not a short circuit) the current limit off-time is reduced. Reducing the off-time during less severe overloads reduces the amount of foldback, recovery time, and start-up time. The off-time is calculated from the following equation:

$$T_{OFF(ILIM)} = \frac{0.07 \times V_{IN}}{V_{FB} + 0.2V} \ \mu s \quad (5)$$

The current limit protection feature is peak limited. The maximum average output will be less than the peak.

N-Channel Buck Switch and Driver

The LM5018 integrates an N-Channel Buck switch and associated floating high voltage gate driver. The gate driver circuit works in conjunction with an external bootstrap capacitor and an internal high voltage diode. A 0.01uF ceramic capacitor connected between the BST pin and the SW pin provides the voltage to the driver during the on-time. During each off-time, the SW pin is at approximately 0V, and the bootstrap capacitor charges from V_{CC} through the internal diode. The minimum off-timer, set to 144ns, ensures a minimum time each cycle to recharge the bootstrap capacitor.

Synchronous Rectifier

The LM5018 provides an internal synchronous N-Channel MOSFET rectifier. This MOSFET provides a path for the inductor current to flow when the high-side MOSFET is turned off.

The synchronous rectifier has no diode emulation mode, and is designed to keep the regulator in continuous conduction mode even during light loads which would otherwise result in discontinuous operation.

Undervoltage Detector

The LM5018 contains a dual level undervoltage lockout (UVLO) circuit. When the UVLO pin voltage is below 0.66V, the controller is in a low current shutdown mode. When the UVLO pin voltage is greater than 0.66V but less than 1.225V, the controller is in standby mode. In standby mode the V_{CC} bias regulator is active while the regulator output is disabled. When the V_{CC} pin exceeds the V_{CC} undervoltage threshold and the UVLO pin voltage is greater than 1.225V, normal operation begins. An external set-point voltage divider from V_{IN} to GND can be used to set the minimum operating voltage of the regulator.

UVLO hysteresis is accomplished with an internal 20µA current source that is switched on or off into the impedance of the set-point divider. When the UVLO threshold is exceeded, the current source is activated to quickly raise the voltage at the UVLO pin. The hysteresis is equal to the value of this current times the resistance R_{UV2}.

UVLO	V_{CC}	Mode	Description
<0.66V		Shutdown	V_{CC} Regulator Disabled. Switcher Disabled.
0.66V – 1.225V		Standby	V_{CC} Regulator Enabled Switcher Disabled.
>1.225V	V_{CC} <4.5V	Standby	V_{CC} Regulator Enabled. Switcher Disabled.
	V_{CC} >4.5V	Operating	V_{CC} Enabled. Switcher Enabled.

If the UVLO pin is wired directly to the V_{IN} pin, the regulator will begin operation once the V_{CC} undervoltage is satisfied.

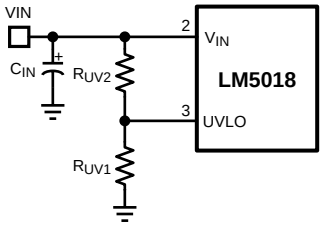


Figure 14. UVLO Resistor Setting

Thermal Protection

The LM5018 should be operated so the junction temperature does not exceed 150°C during normal operation. An internal Thermal Shutdown circuit is provided to protect the LM5018 in the event of a higher than normal junction temperature. When activated, typically at 165°C, the controller is forced into a low power reset state, disabling the buck switch and the V_{CC} regulator. This feature prevents catastrophic failures from accidental device overheating. When the junction temperature reduces below 145°C (typical hysteresis = 20°C), the V_{CC} regulator is enabled, and normal operation is resumed.

Application Information

SELECTION OF EXTERNAL COMPONENTS

Selection of external components is illustrated through a design example. The design example specifications are as follows:

Buck Converter Design Specifications	
Input Voltage Range	12.5V to 95V
Output Voltage	10V
Maximum Load Current	300mA
Switching Frequency	400kHz

R_{FB1}, R_{FB2}:

V_{OUT} = V_{FB} x (R_{FB2}/R_{FB1} + 1), and since V_{FB} = 1.225V, the ratio of R_{FB2} to R_{FB1} calculates as 7:1. Standard values of 6.98kΩ and 1.00kΩ are chosen. Other values could be used as long as the 7:1 ratio is maintained.

Frequency Selection:

At the minimum input voltage, the maximum switching frequency of LM5018 is restricted by the forced minimum off-time ($T_{OFF(MIN)}$) as given by:

$$f_{SW(MAX)} = \frac{1 - D_{MAX}}{T_{OFF(MIN)}} = \frac{1 - 10/12.5}{200\ ns} = 1\ MHz \quad (6)$$

Similarly, at maximum input voltage, the maximum switching frequency of LM5018 is restricted by the minimum T_{ON} as given by:

$$f_{SW(MAX)} = \frac{D_{MIN}}{T_{ON(MIN)}} = \frac{10/95}{100\ ns} = 1.05\ MHz \quad (7)$$

Resistor R_{ON} sets the nominal switching frequency based on the following equations:

$$f_{SW} = \frac{V_{OUT}}{K \times R_{ON}} \quad (8)$$

where $K = 1 \times 10^{-10}$. Operation at high switching frequency results in lower efficiency while providing the smallest solution. For this example a conservative 400kHz was selected, resulting in R_{ON} = 246kΩ. Selecting a standard value for R_{ON} = 237kΩ results in a nominal frequency of 416kHz.

Inductor Selection:

The inductance selection is a compromise between solution size, output ripple, and efficiency. The peak inductor current at maximum load current should be smaller than the minimum current limit of 350mA. The maximum permissible peak to peak inductor ripple is:

$\Delta IL = 2*(I_{LIM(min)} — I_{OUT(max)}) = 2*50 = 100mA$

The minimum inductance is given by:

$$\Delta I_L = \frac{V_{IN} - V_{OUT}}{L1 \times f_{SW}} \times \frac{V_{OUT}}{V_{IN}} \quad (9)$$

Resulting in L=215µH. A standard value of 220µH is selected. For proper operation the inductor saturation current should be higher than the peak encountered in the application. For robust short circuit protection, the inductor saturation current should be higher than the maximum current limit of 700mA.

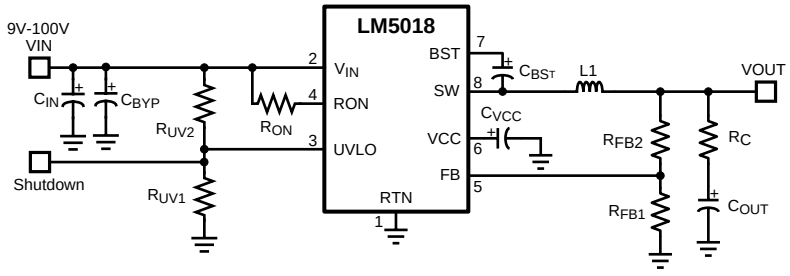


Figure 15. Reference Schematic for Selection of External Components

Output Capacitor:

The output capacitor is selected to minimize the capacitive ripple across it. The maximum ripple is observed at maximum input voltage and is given by:

$$C_{OUT} = \frac{\Delta I_L}{8 \times f_{sw} \times \Delta V_{ripple}} \quad (10)$$

where ΔV_{ripple} is the voltage ripple across the capacitor. Substituting ΔV_{ripple} = 10mV gives C_{OUT} = 2.9µF. A 4.7µF standard value is selected. An X5R or X7R type capacitor with a voltage rating 16V or higher should be selected.

Series Ripple Resistor R_C:

The series resistor should be selected to produce sufficient ripple at the feedback node. The ripple produced by R_C is proportional to the inductor current ripple, and therefore R_C should be chosen for minimum inductor current ripple which occurs at minimum input voltage. The R_C is calculated by the equation:

$$R_C \geq \frac{25\ mV}{\Delta I_{L(MIN)}} \times \frac{V_{OUT}}{V_{REF}} \quad (11)$$

This gives an R_C of greater than or equal to 10.8Ω. Selecting R_C = 11Ω results in ~1V of maximum output voltage ripple. For application requiring lower output voltage ripple, Type II or Type III ripple injection circuits should be used as described in the section “Ripple Configuration”.

V_{CC} and Bootstrap Capacitor:

The V_{CC} capacitor provides charge to bootstrap capacitor as well as internal circuitry and low side gate driver. The Bootstrap capacitor provides charge to high side gate driver. A good value for C_{VCC} is 1µF. A good value for C_{BST} is 0.01µF.

Input Capacitor:

Input capacitor should be large enough to limit the input voltage ripple:

$$C_{IN} \geq \frac{I_{OUT(MAX)}}{8 \times f_{SW} \times \Delta V_{IN}} \quad (12)$$

choosing a ΔV_{IN} = 0.5V gives a minimum C_{IN} = 0.36µF. A standard value of 1µF is selected. The input capacitor should be rated for the maximum input voltage under all conditions. A 100V, X7R dielectric should be selected for this design.

Input capacitor should be placed directly across V_{IN} and RTN (pin 2 and 1) of the IC. If it is not possible to place all of the input capacitor close to the IC, a 0.1µF capacitor should be placed near the IC to provide a bypass path for the high frequency component of the switching current. This helps limit the switching noise.

UVLO Resistors:

The UVLO resistors R_{FB1} and R_{FB2} set the UVLO threshold and hysteresis according to the following relationship:

$$V_{IN}(HYS) = I_{HYS} \times R_{UV2} \quad (13)$$

and

$$/_{IN}(UVLO,rising) = 1.225V \times \left(\frac{R_{UV2}}{R_{UV1}} + 1\right) \quad (14)$$

where I_{HYS} = 20µA. Setting UVLO hysteresis of 2.5V and UVLO rising threshold of 12V results in R_{UV1} = 14.53kΩ and R_{UV2} = 125kΩ. Selecting standard value of R_{UV1} = 14kΩ and R_{UV2} = 125kΩ results in UVLO thresholds and hysteresis of 12.4V and 2.5V respectively.

APPLICATION CIRCUIT: 12V TO 95V INPUT AND 10V, 300mA OUTPUT BUCK CONVERTER

The application schematic of a buck supply is shown in Figure 16 below. For output voltage (V_{OUT}) above the maximum regulation threshold of V_{CC} (8.3V, see electrical characteristics), the V_{CC} pin can be connected to V_{OUT} through a diode (D2), as shown below, for higher efficiency and lower power dissipation in the IC.

RIPPLE CONFIGURATION

LM5018 uses Constant-On-Time (COT) control scheme, in which the on-time is terminated by an on-timer, and the off-time is terminated by the feedback voltage (V_{FB}) falling below the reference voltage (V_{REF}). Therefore, for stable operation, the feedback voltage must decrease monotonically, in phase with the inductor current during the off-time. Furthermore, this change in feedback voltage (V_{FB}) during off-time must be large enough to suppress any noise component present at the feedback node.

Table 1 shows three different methods for generating appropriate voltage ripple at the feedback node. Type 1 and Type 2 ripple circuits couple the ripple at the output of the converter to the feedback node (FB). The output voltage ripple has two components:

1. Capacitive ripple caused by the inductor current ripple charging/discharging the output capacitor.
2. Resistive ripple caused by the inductor current ripple flowing through the ESR of the output capacitor.

The capacitive ripple is not in phase with the inductor current. As a result, the capacitive ripple does not decrease monotonically during the off-time. The resistive ripple is in phase with the inductor current and decreases monotonically during the off-time. The resistive ripple must exceed the capacitive ripple at the output node (V_{OUT}) for stable operation. If this condition is not satisfied unstable switching behavior is observed in COT converters, with multiple on-time bursts in close succession followed by a long off-time.

Type 3 ripple method uses R_r and C_r and the switch node (SW) voltage to generate a triangular ramp. This triangular ramp is ac coupled using C_{ac} to the feedback node (FB). Since this circuit does not use the output voltage ripple, it is ideally suited for applications where low output voltage ripple is required. See application note AN-1481 for more details for each ripple generation method.

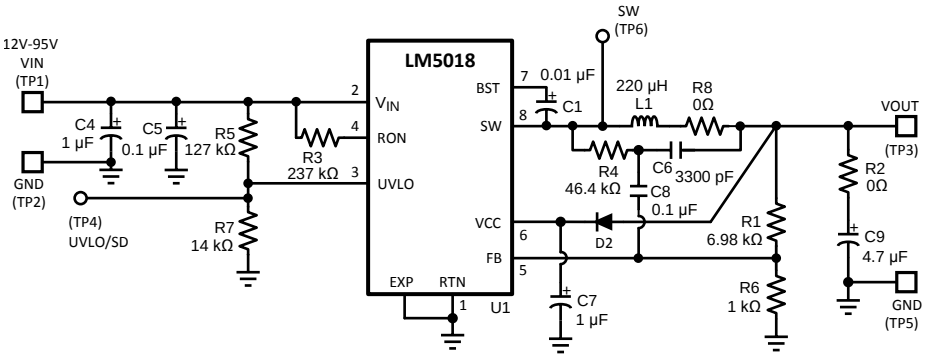
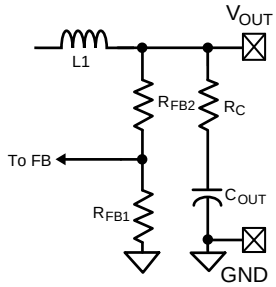
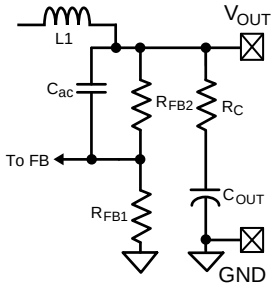
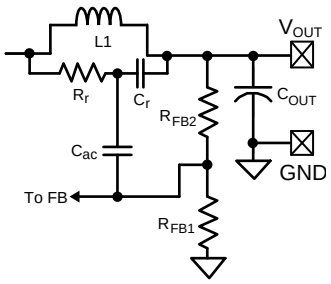


Figure 16. Final Schematic for 12V to 95V Input, and 10V, 300mA Output Buck Converter

Type 1 Lowest Cost Configuration	Type 2 Reduced Ripple Configuration	Type 3 Minimum Ripple Configuration
		
$R_C \geq \frac{25\ mV}{\Delta I_{L(MIN)}} \times \frac{V_{OUT}}{V_{REF}}$ (15)	$C_{ac} \geq 5 f_{SW} / (R_{FB2} \| R_{FB1})$ $R_C \geq \frac{25\ mV}{\Delta I_{L(MIN)}}$ (16)	$C_r = 3300\ pF$ $C_{ac} = 100\ nF$ $R_r C_r \leq \frac{(V_{IN(MIN)} - V_{OUT}) \times T_{ON}}{25\ mV}$ (17)

LAYOUT RECOMMENDATION

A proper layout is essential for optimum performance of the circuit. In particular, the following guidelines should be observed:

1. C_{IN}: The loop consisting of input capacitor (C_{IN}), V_{IN} pin, and RTN pin carries switching currents. Therefore, the input capacitor should be placed close to the IC, directly across V_{IN} and RTN pins and the connections to these two pins should be direct to minimize the loop area. In general it is not possible to accommodate all of input capacitance near the IC. A good practice is to use a 0.1µF or 0.47µF capacitor directly across the V_{IN} and RTN pins close to the IC, and the remaining bulk capacitor as close as possible (Refer to Figure 17 Placement of Bypass Capacitors).
2. C_{VCC} and C_{BST}: The V_{CC} and bootstrap (BST) bypass capacitors supply switching currents to the high and low side gate drivers. These two capacitors should also be placed as close to the IC as possible, and the connecting trace length and loop area should be minimized (See Figure 17 Placement of Bypass

Capacitors).

3. The Feedback trace carries the output voltage information and a small ripple component that is necessary for proper operation of LM5018. Therefore, care should be taken while routing the feedback trace to avoid coupling any noise to this pin. In particular, feedback trace should not run close to magnetic components, or parallel to any other switching trace.
4. SW trace: The SW node switches rapidly between V_{IN} and GND every cycle and is therefore a possible source of noise. The SW node area should be minimized. In particular, the SW node should not be inadvertently connected to a copper plane or pour.

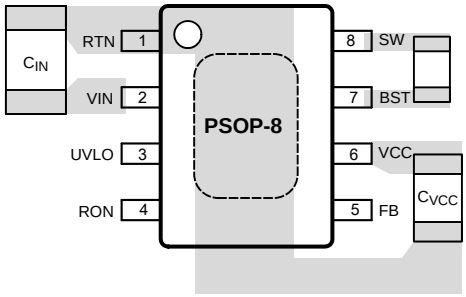


Figure 17. Placement of Bypass Capacitors

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
LM5018MR/NOPB	ACTIVE	SO PowerPAD	DDA	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR		L5018 MR	Samples
LM5018MRX/NOPB	ACTIVE	SO PowerPAD	DDA	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR		L5018 MR	Samples
LM5018SD/NOPB	ACTIVE	WSON	NGU	8	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM		L5018	Samples
LM5018SDX/NOPB	ACTIVE	WSON	NGU	8	4500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM		L5018	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

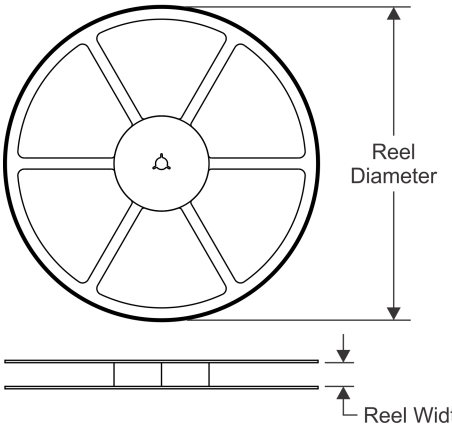
(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

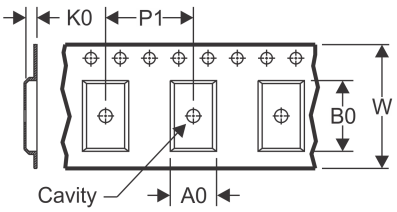
(4) Only one of markings shown within the brackets will appear on the physical device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

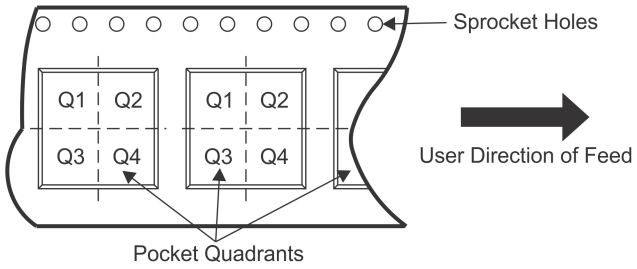


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

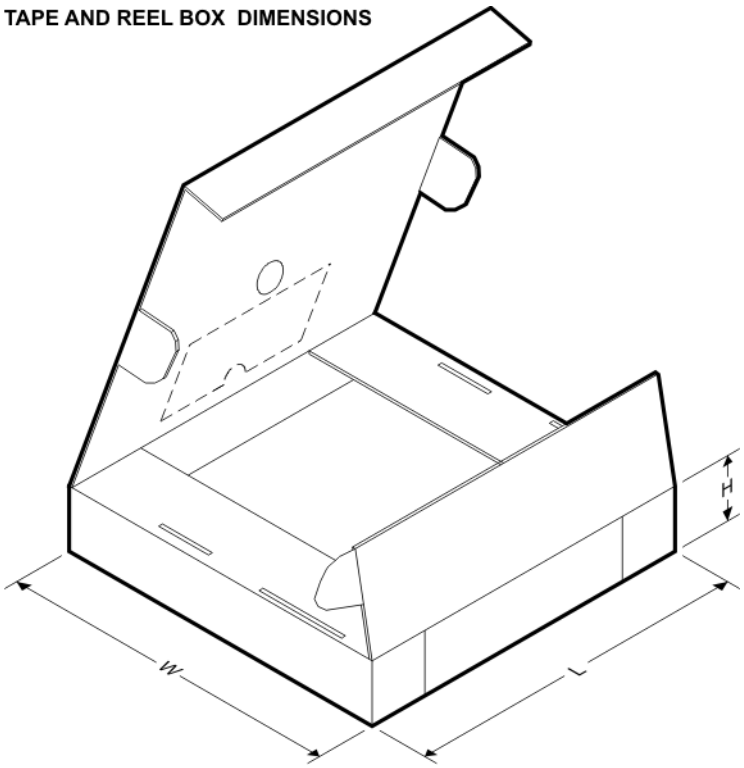
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM5018MRX/NOPB	SO Power PAD	DDA	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LM5018SD/NOPB	WSON	NGU	8	1000	178.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1
LM5018SDX/NOPB	WSON	NGU	8	4500	330.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1

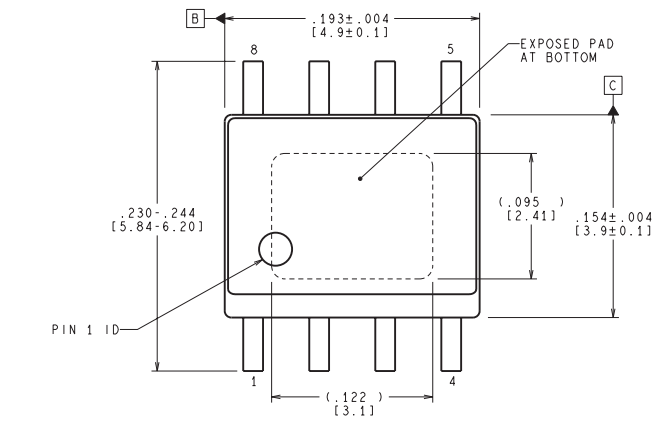
TAPE AND REEL BOX DIMENSIONS

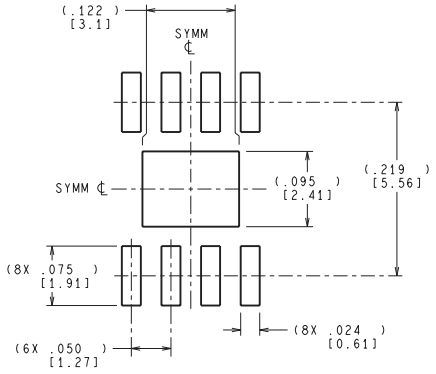


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM5018MRX/NOPB	SO PowerPAD	DDA	8	2500	358.0	343.0	63.0
LM5018SD/NOPB	WSON	NGU	8	1000	203.0	190.0	41.0
LM5018SDX/NOPB	WSON	NGU	8	4500	349.0	337.0	45.0

DDA0008B





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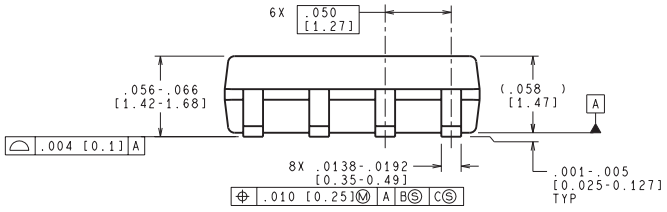

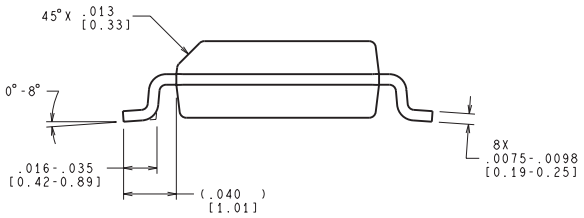

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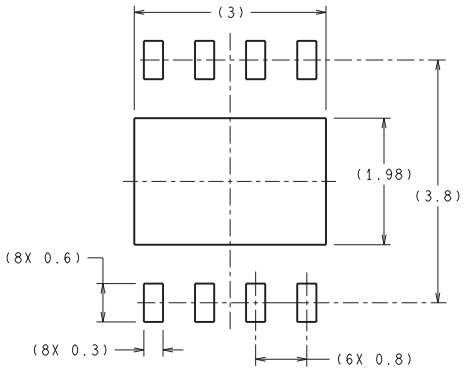

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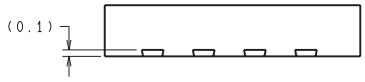

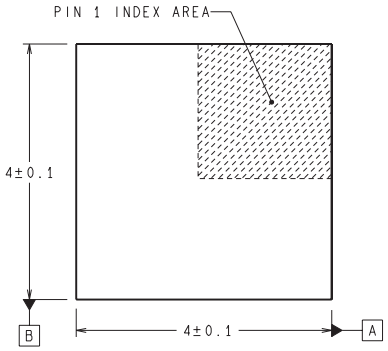

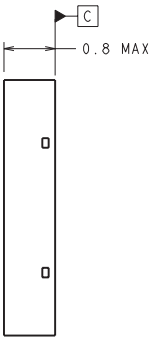

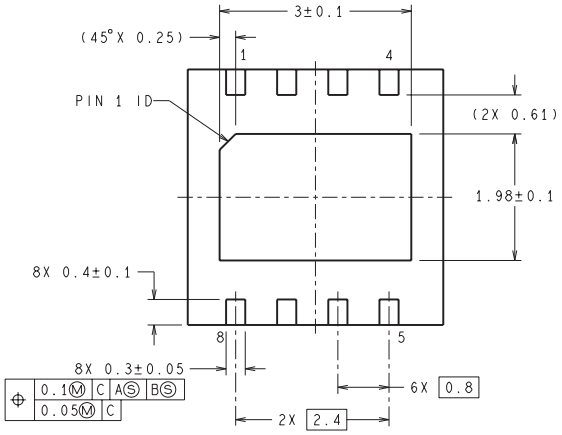

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