LM5102 High Voltage Half-Bridge Gate Driver with Programmable Delay

Check for Samples: LM5102

FEATURES

- **Drives both a High Side and Low Side N-Channel MOSFET**
- **Independently Programmable High and Low Side Rising Edge Delay**
- **Bootstrap Supply Voltage Range up to 118V DC**
- **Fast Turn-Off Propagation Delay (25 ns Typical)**
- **Drives 1000 pF Loads with 15 ns Rise and Fall Times**
- **Supply Rail Under-Voltage Lockout**
- **Low Power Consumption**
- **Timer Can be Terminated Midway through Sequence**

TYPICAL APPLICATIONS

- **Current Fed Push-Pull Power Converters**
- **Half and Full Bridge Power Converters**
- **Synchronous Buck Converters**
- **Two Switch Forward Power Converters**
- **Forward with Active Clamp Converters**

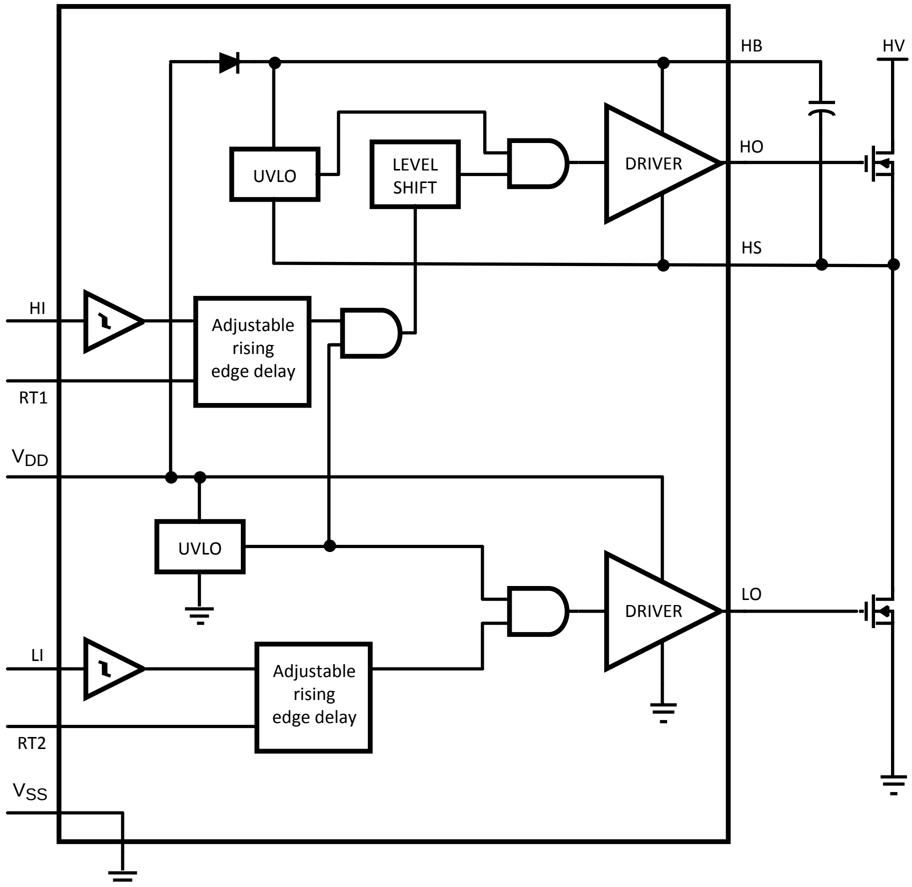
DESCRIPTION

The LM5102 High Voltage Gate Driver is designed to drive both the high side and the low side N-Channel MOSFETs in a synchronous buck or a half bridge configuration. The floating high-side driver is capable of working with supply voltages up to 100V. The outputs are independently controlled. The rising edge of each output can be independently delayed with a programming resistor. An integrated high voltage diode is provided to charge the high side gate drive bootstrap capacitor. A robust level shifter operates at high speed while consuming low power and providing clean level transitions from control logic to the high side gate driver. Under-voltage lockout is provided on both the low side and the high side power rails. This device is available in the standard VSSOP-10 pin and the WSON-10 pin packages.

Package

- VSSOP-10
- WSON-10 (4 mm x 4 mm)

Simplified Block Diagram



Connection Diagram

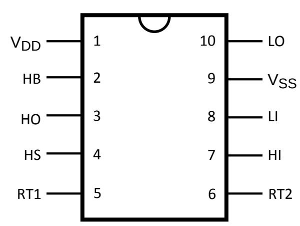


Figure 1. 10-Lead VSSOP, WSON
See DGS0010A and DPR0010A

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings[(1)(2)]

V_{DD} to V_{SS}	–0.3V to +18V
V_{HB} to V_{HS}	–0.3V to +18V
LI or HI Inputs to V_{SS}	–0.3V to V_{DD} + 0.3V
LO Output	–0.3V to V_{DD} + 0.3V
HO Output	V_{HS} – 0.3V to V_{HB} + 0.3V
V_{HS} to V_{SS}	−1V to +100V
V_{HB} to V_{SS}	118V
RT1 & RT2 to V_{SS}	–0.3V to 5V
Junction Temperature	+150°C
Storage Temperature Range	–55°C to +150°C
ESD Rating HBM[(3)]	2 kV

(1) Absolute Maximum Ratings indicate limits beyond which damage to the component may occur. Operating Ratings are conditions under which operation of the device is guaranteed. Operating Ratings do not imply guaranteed performance limits. For guaranteed performance limits and associated test conditions, see Electrical Characteristics.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.
(3) The human body model is a 100 pF capacitor discharged through a 1.5kΩ resistor into each pin. 2 kV for all pins except Pin 2, Pin 3 and Pin 4 which are rated at 500V.

Recommended Operating Conditions

V_{DD}	+9V to +14V
HS	–1V to 100V
HB	V_{HS} + 8V to V_{HS} + 14V
HS Slew Rate	< 50V/ns
Junction Temperature	–40°C to +125°C

Electrical Characteristics

Specifications in standard typeface are for T_J = +25°C, and those in **boldface type** apply over the full **operating junction temperature range**. Unless otherwise specified, V_{DD} = V_{HB} = 12V, V_{SS} = V_{HS} = 0V, RT1 = RT2 = 100kΩ. No Load on LO or HO.

Symbol	Parameter	Conditions	Min[(1)]	Typ	Max[(1)]	Units
SUPPLY CURRENTS						
I_{DD}	V_{DD} Quiescent Current	LI = HI = 0V		0.4	**0.6**	mA
I_{DDO}	V_{DD} Operating Current	f = 500 kHz		1.5	**3**	mA
I_{HB}	Total HB Quiescent Current	LI = HI = 0V		0.06	**0.2**	mA
I_{HBO}	Total HB Operating Current	f = 500 kHz		1.3	**3**	mA
I_{HBS}	HB to V_{SS} Current, Quiescent	V_{HS} = V_{HB} = 100V		0.05	**10**	µA
I_{HBSO}	HB to V_{SS} Current, Operating	f = 500 kHz		0.08		mA
INPUT PINS						
V_{IL}	Low Level Input Voltage Threshold		**0.8**	1.8		V
V_{IH}	High Level Input Voltage Threshold			1.8	**2.2**	V
R_I	Input Pulldown Resistance		**100**	200	**500**	kΩ
TIME DELAY CONTROLS						
V_{RT}	Nominal Voltage at RT1, RT2		**2.7**	3	**3.3**	V
I_{RT}	RT Pin Current Limit	RT1 = RT2 = 0V	**0.75**	1.5	**2.25**	mA
V_{th}	Timer Termination Threshold			1.8		V
T_{DL1}, T_{DH1}	Rising edge turn-on delay, RT = 10 kΩ		**75**	105	**150**	ns
T_{DL2}, T_{DH2}	Rising edge turn-on delay, RT = 100 kΩ		**530**	630	**750**	ns

(1) Min and Max limits are 100% production tested at 25°C. Limits over the operating temperature range are guaranteed through correlation using Statistical Quality Control (SQC) methods. Limits are used to calculate TI's Average Outgoing Quality Level (AOQL).

Electrical Characteristics (continued)

Specifications in standard typeface are for T_J = +25°C, and those in **boldface type** apply over the full **operating junction temperature range**. Unless otherwise specified, V_{DD} = V_{HB} = 12V, V_{SS} = V_{HS} = 0V, RT1 = RT2 = 100kΩ. No Load on LO or HO.

Symbol	Parameter	Conditions	Min[(1)]	Typ	Max[(1)]	Units
UNDER VOLTAGE PROTECTION						
V_{DDR}	V_{DD} Rising Threshold		**6.0**	6.9	**7.4**	V
V_{DDH}	V_{DD} Threshold Hysteresis			0.5		V
V_{HBR}	HB Rising Threshold		**5.7**	6.6	**7.1**	V
V_{HBH}	HB Threshold Hysteresis			0.4		V
BOOT STRAP DIODE						
V_{DL}	Low-Current Forward Voltage	I_{VDD-HB} = 100 µA		0.60	**0.9**	V
V_{DH}	High-Current Forward Voltage	I_{VDD-HB} = 100 mA		0.85	**1.1**	V
R_D	Dynamic Resistance	I_{VDD-HB} = 100 mA		0.8	**1.5**	Ω
LO GATE DRIVER						
V_{OLL}	Low-Level Output Voltage	I_{LO} = 100 mA		0.25	**0.4**	V
V_{OHL}	High-Level Output Voltage	I_{LO} = –100 mA, V_{OHL} = V_{DD} – V_{LO}		0.35	**0.55**	V
I_{OHL}	Peak Pullup Current	V_{LO} = 0V		1.6		A
I_{OLL}	Peak Pulldown Current	V_{LO} = 12V		1.8		A
HO GATE DRIVER						
V_{OLH}	Low-Level Output Voltage	I_{HO} = 100 mA		0.25	**0.4**	V
V_{OHH}	High-Level Output Voltage	I_{HO} = –100 mA, V_{OHH} = V_{HB} – V_{HO}		0.35	**0.55**	V
I_{OHH}	Peak Pullup Current	V_{HO} = 0V		1.6		A
I_{OLH}	Peak Pulldown Current	V_{HO} = 12V		1.8		A
THERMAL RESISTANCE						
θ_{JA} [(2)]	Junction to Ambient	VSSOP		200		°C/W
		WSON-10[(3)]		40		

(2) The θ_{JA} is not a given constant for the package and depends on the printed circuit board design and the operating environment.
(3) 4 layer board with Cu finished thickness 1.5/1/1/1.5 oz. Maximum die size used. 5x body length of Cu trace on PCB top. 50 x 50mm ground and power planes embedded in PCB. See Application Note AN-1187.

Switching Characteristics

Specifications in standard typeface are for T_J = +25°C, and those in **boldface type** apply over the full **operating junction temperature range**. Unless otherwise specified, V_{DD} = V_{HB} = 12V, V_{SS} = V_{HS} = 0V, No Load on LO or HO.

Symbol	Parameter	Conditions	Min[(1)]	Typ	Max[(1)]	Units
t_{LPHL}	Lower Turn-Off Propagation Delay LM5102 (LI Falling to LO Falling)			27	**56**	ns
t_{HPHL}	Upper Turn-Off Propagation Delay LM5102 (HI Falling to HO Falling)			27	**56**	ns
t_{RC}, t_{FC}	Either Output Rise/Fall Time	C_L = 1000 pF		15		ns
t_R, t_F	Either Output Rise/Fall Time (3V to 9V)	C_L = 0.1 µF		0.6		µs
t_{BS}	Bootstrap Diode Turn-Off Time	I_F = 20 mA, I_R = 200 mA		50		ns

(1) Min and Max limits are 100% production tested at 25°C. Limits over the operating temperature range are guaranteed through correlation using Statistical Quality Control (SQC) methods. Limits are used to calculate TI's Average Outgoing Quality Level (AOQL).

Typical Performance Characteristics

I_{DD} vs Frequency

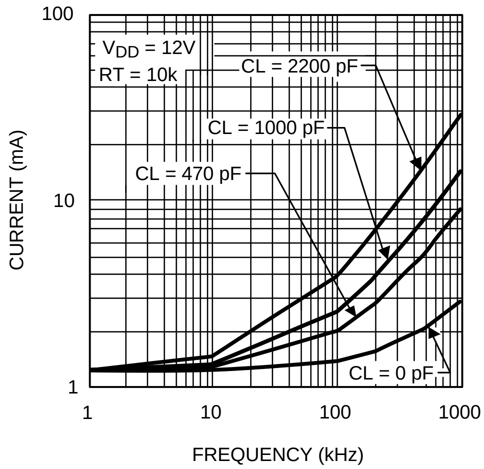


Figure 2.

Operating Current vs Temperature

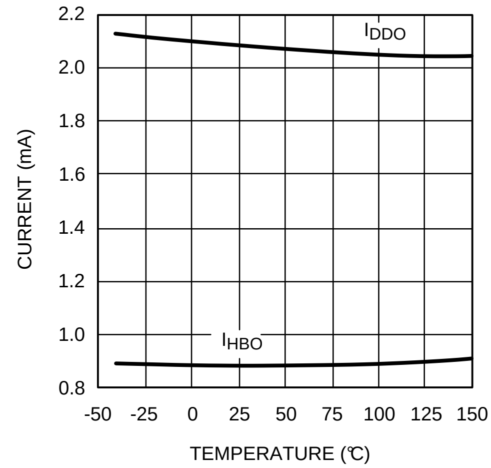


Figure 3.

Quiescent Current vs Supply Voltage

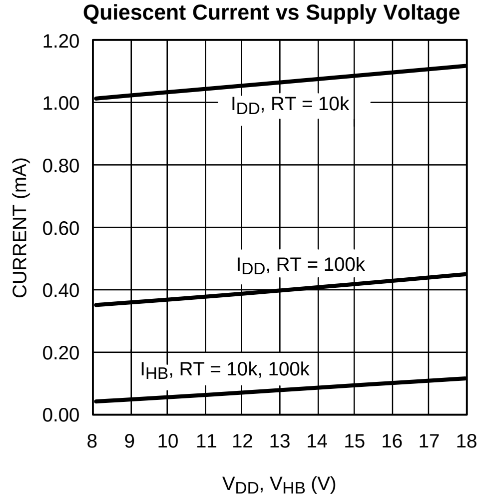


Figure 4.

Quiescent Current vs Temperature

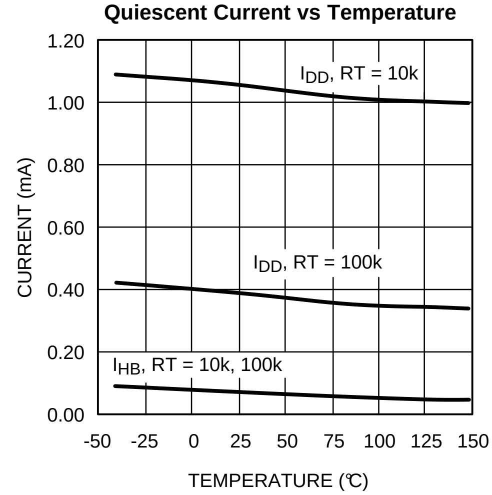


Figure 5.

I_{HB} vs Frequency

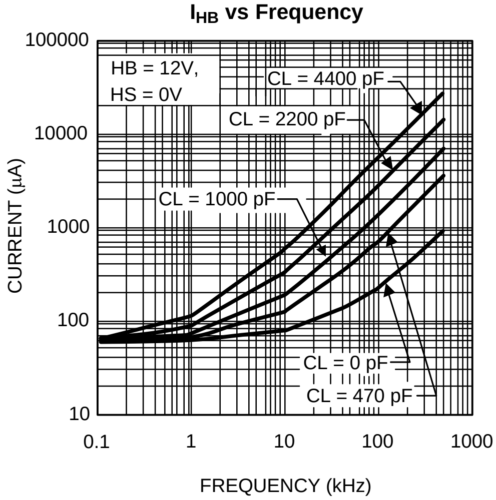


Figure 6.

HO & LO Peak Output Current vs Output Voltage

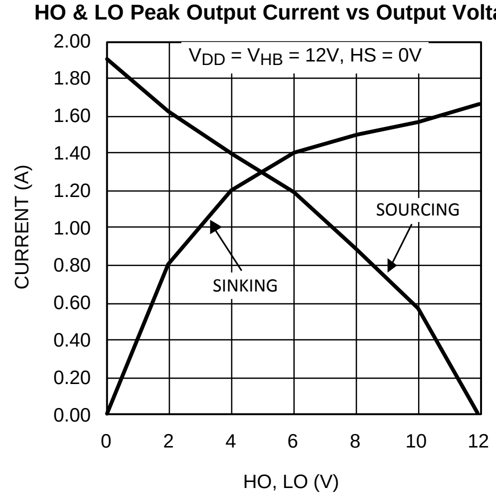


Figure 7.

Typical Performance Characteristics (continued)

Diode Forward Voltage

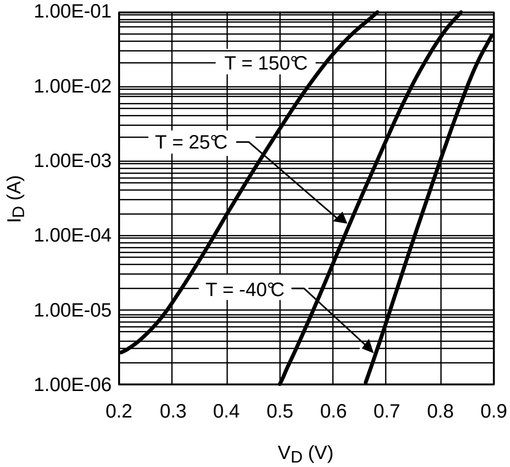


Figure 8.

Undervoltage Threshold Hysteresis vs Temperature

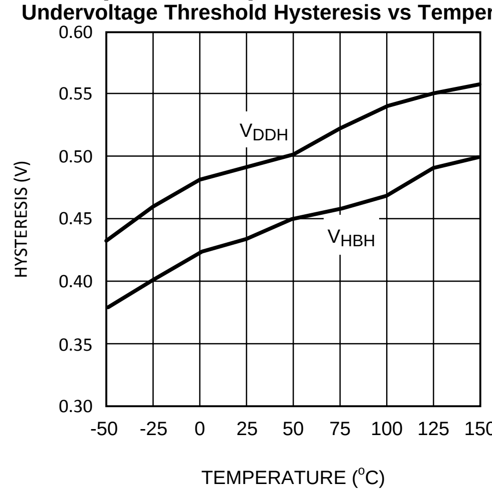


Figure 9.

Undervoltage Rising Threshold vs Temperature

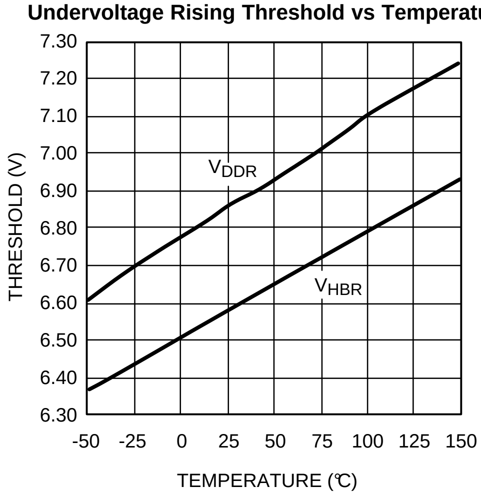


Figure 10.

LO & HO Gate Drive—High Level Output Voltage vs Temperature

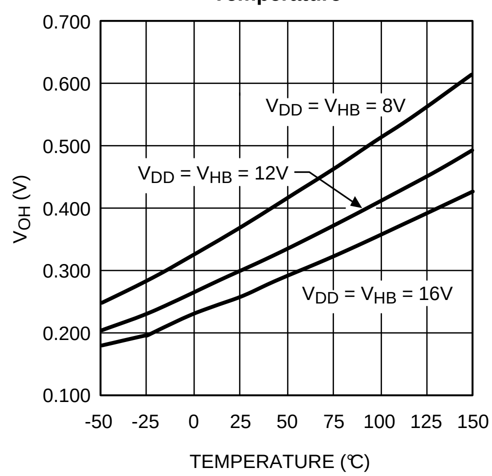


Figure 11.

LO & HO Gate Drive—Low Level Output Voltage vs Temperature

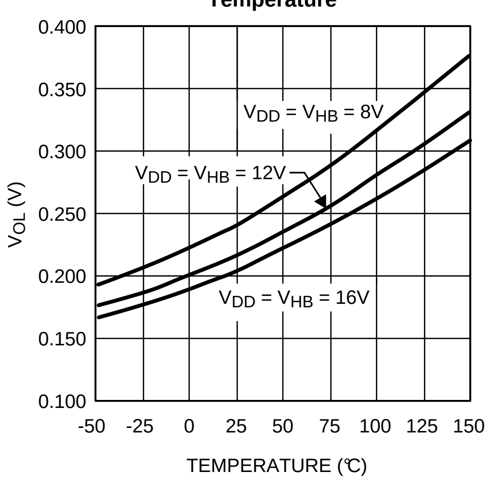


Figure 12.

Turn Off Propagation Delay vs Temperature

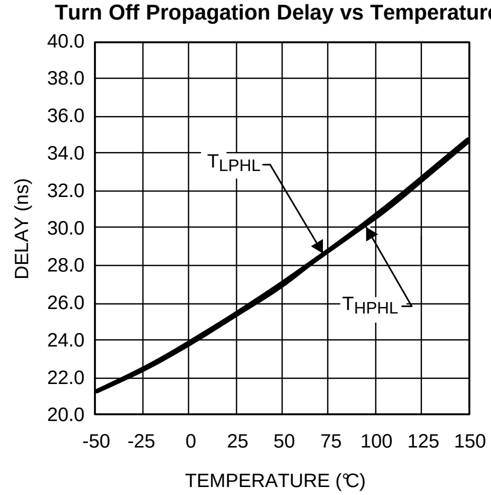


Figure 13.

Typical Performance Characteristics (continued)

Turn On Delay vs RT Resistor Value

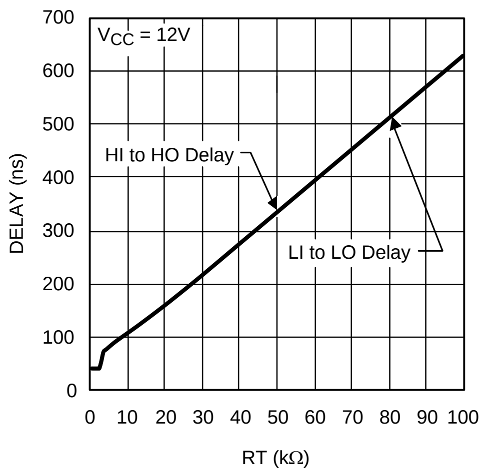


Figure 14.

Turn On Delay vs Temperature (RT = 10k)

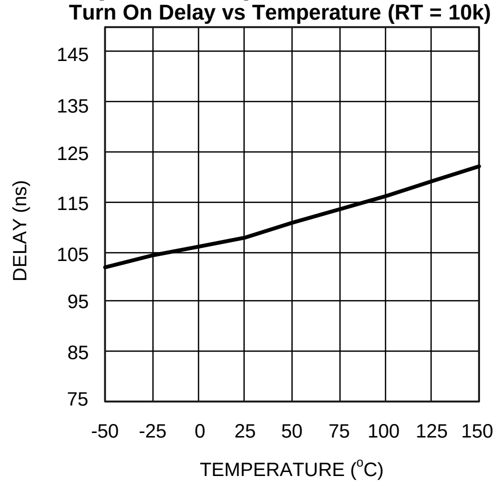


Figure 15.

Turn On Delay vs Temperature (RT = 100k)

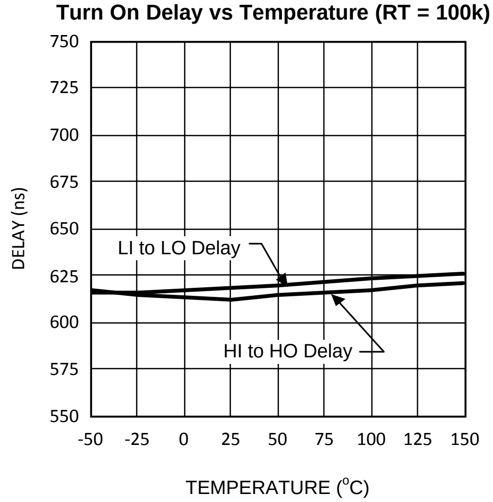


Figure 16.

LM5102 Waveforms

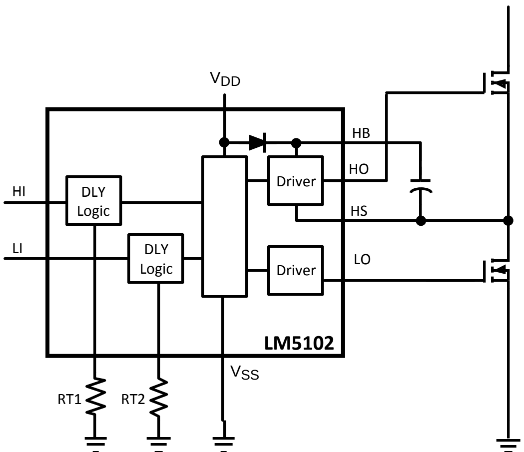


Figure 17. (a) Application Timing Waveforms

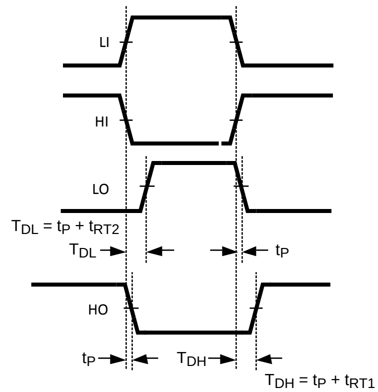


Figure 18. (b) Application Timing Waveforms

Operational Notes

The LM5102 offers a unique flexibility with independently programmable delay of the rising edge for both high and low side driver outputs independently. The delays are set with resistors at the RT1 and RT2 pins, and can be adjusted from 100 ns to 600 ns. This feature reduces component count, board space and cost compared to discrete solutions for adjusting driver dead time. The wide delay programming range provides the flexibility to optimize drive signal timing for a wide range of MOSFETs and applications.

The RT pins are biased at 3V and current limited to 1 mA maximum programming current. The time delay generator will accommodate resistor values from 5k to 100k with turn-on delay times that are proportional to the RT resistance. In addition, each RT pin is monitored by a comparator that will bypass the turn-on delay if the RT pin is pulled below the timer elimination threshold (1.8V typical). Grounding the RT pins programs the LM5102 to drive both outputs with minimum turn-on delay.

STARTUP AND UVLO

Both top and bottom drivers include under-voltage lockout (UVLO) protection circuitry which monitors the supply voltage (V_{DD}) and bootstrap capacitor voltage (V_{HB} – V_{HS}) independently. The UVLO circuit inhibits each driver until sufficient supply voltage is available to turn-on the external MOSFETs, and the built-in hysteresis prevents chattering during supply voltage transitions. When the supply voltage is applied to V_{DD} pin of LM5102, the top and bottom gates are held low until V_{DD} exceeds UVLO threshold, typically about 6.9V. Any UVLO condition on the bootstrap capacitor will disable only the high side output (HO).

LAYOUT CONSIDERATIONS

The optimum performance of high and low side gate drivers cannot be achieved without taking due considerations during circuit board layout. Following points are emphasized.

1. A low ESR/ESL capacitor must be connected close to the IC, and between V_{DD} and V_{SS} pins and between HB and HS pins to support high peak currents being drawn from V_{DD} during turn-on of the external MOSFET.
2. To prevent large voltage transients at the drain of the top MOSFET, a low ESR electrolytic capacitor must be connected between MOSFET drain and ground (V_{SS}).
3. In order to avoid large negative transients on the switch node (HS) pin, the parasitic inductances in the source of top MOSFET and in the drain of the bottom MOSFET (synchronous rectifier) must be minimized.
4. Grounding considerations:
   - The first priority in designing grounding connections is to confine the high peak currents from charging and discharging the MOSFET gate in a minimal physical area. This will decrease the loop inductance and minimize noise issues on the gate terminal of the MOSFET. The MOSFETs should be placed as close as possible to the gate driver.
   - The second high current path includes the bootstrap capacitor, the bootstrap diode, the local ground referenced bypass capacitor and low side MOSFET body diode. The bootstrap capacitor is recharged on the cycle-by-cycle basis through the bootstrap diode from the ground referenced V_{DD} bypass capacitor. The recharging occurs in a short time interval and involves high peak current. Minimizing this loop length and area on the circuit board is important to ensure reliable operation.
5. The resistors on the RT1 and RT2 timer pins must be placed very close to the IC and seperated from high current paths to avoid noise coupling to the time delay generator which could disrupt timer operation.

POWER DISSIPATION CONSIDERATIONS

The total IC power dissipation is the sum of the gate driver losses and the bootstrap diode losses. The gate driver losses are related to the switching frequency (f), output load capacitance on LO and HO (C_L), and supply voltage (V_{DD}) and can be roughly calculated as:

$$P_{DGATES} = 2 \bullet f \bullet C_L \bullet V_{DD}^2 \quad (1)$$

There are some additional losses in the gate drivers due to the internal CMOS stages used to buffer the LO and HO outputs. The following plot shows the measured gate driver power dissipation versus frequency and load capacitance. At higher frequencies and load capacitance values, the power dissipation is dominated by the power losses driving the output loads and agrees well with the above equation. This plot can be used to approximate the power losses due to the gate drivers.

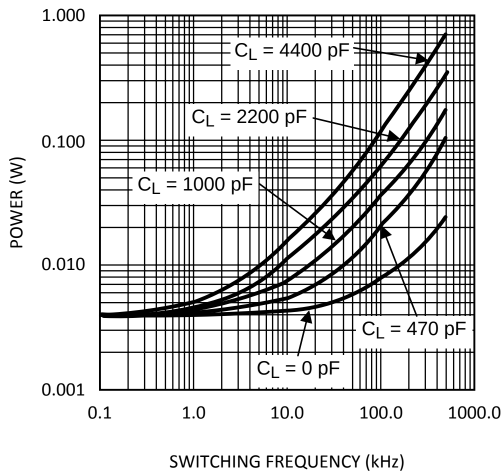


Figure 19. Gate Driver Power Dissipation (LO + HO)
V_{CC} = 12V, Neglecting Diode Losses

The bootstrap diode power loss is the sum of the forward bias power loss that occurs while charging the bootstrap capacitor and the reverse bias power loss that occurs during reverse recovery. Since each of these events happens once per cycle, the diode power loss is proportional to frequency. Larger capacitive loads require more current to recharge the bootstrap capacitor resulting in more losses. Higher input voltages (V_{IN}) to the half bridge result in higher reverse recovery losses. The following plot was generated based on calculations and lab measurements of the diode recovery time and current under several operating conditions. This can be useful for approximating the diode power dissipation.

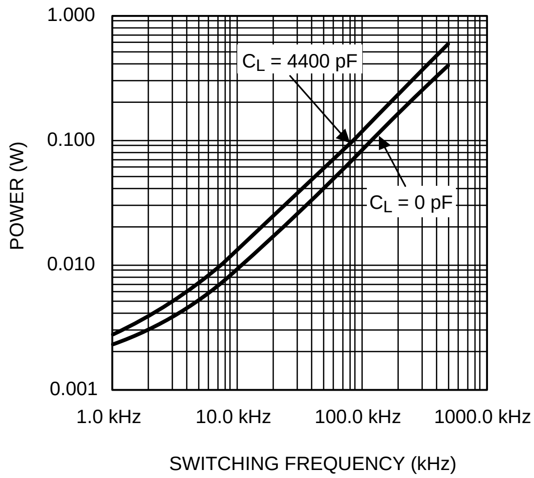


Figure 20. Diode Power Dissipation V_{IN} = 80V

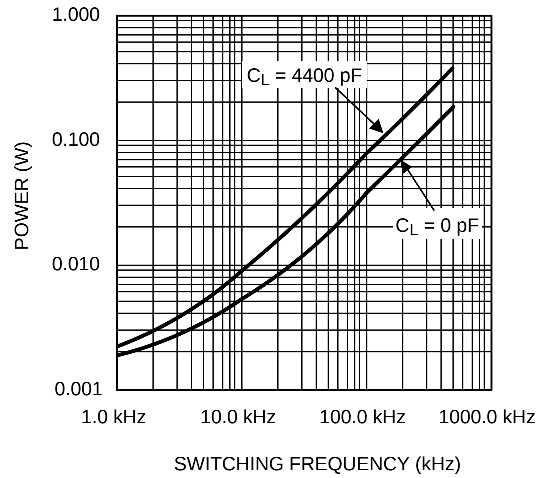


Figure 21. Diode Power Dissipation V_{IN} = 40V

The total IC power dissipation can be estimated from the above plots by summing the gate drive losses with the bootstrap diode losses for the intended application. Because the diode losses can be significant, an external diode placed in parallel with the internal bootstrap diode (refer to Figure 22) and can be helpful in removing power from the IC. For this to be effective, the external diode must be placed close to the IC to minimize series inductance and have a significantly lower forward voltage drop than the internal diode.

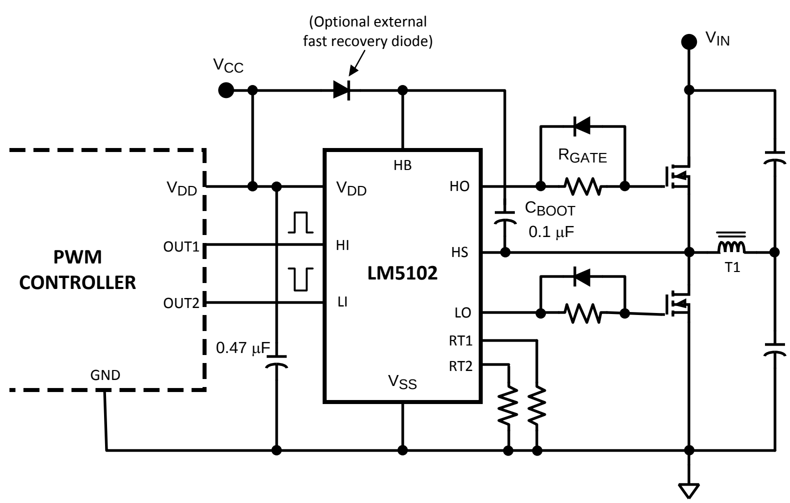


Figure 22. LM5102 Driving MOSFETs Connected in Half-Bridge Configuration

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
LM5102MM	ACTIVE	VSSOP	DGS	10	1000	TBD	Call TI	Call TI	-40 to 125	5102	Samples
LM5102MM/NOPB	ACTIVE	VSSOP	DGS	10	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	5102	Samples
LM5102MMX	ACTIVE	VSSOP	DGS	10	3500	TBD	Call TI	Call TI	-40 to 125	5102	Samples
LM5102MMX/NOPB	ACTIVE	VSSOP	DGS	10	3500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	5102	Samples
LM5102SD	ACTIVE	WSON	DPR	10	1000	TBD	Call TI	Call TI	-40 to 125	5102SD	Samples
LM5102SD/NOPB	ACTIVE	WSON	DPR	10	1000	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 125	5102SD	Samples
LM5102SDX	ACTIVE	WSON	DPR	10	4500	TBD	Call TI	Call TI	-40 to 125	5102SD	Samples
LM5102SDX/NOPB	ACTIVE	WSON	DPR	10	4500	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 125	5102SD	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Only one of markings shown within the brackets will appear on the physical device.

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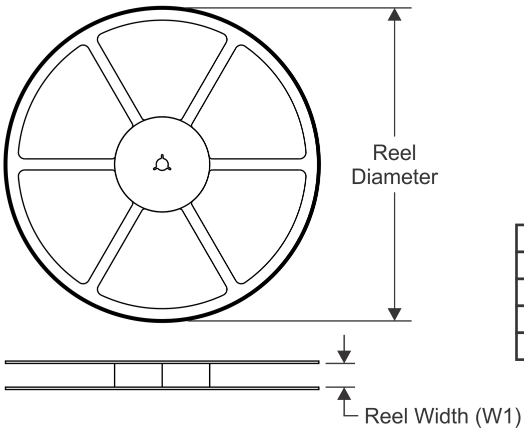
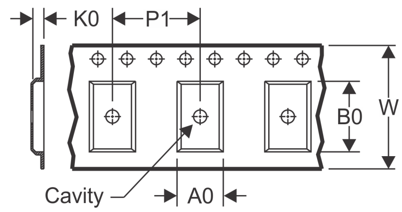
TAPE AND REEL INFORMATION

REEL DIMENSIONS

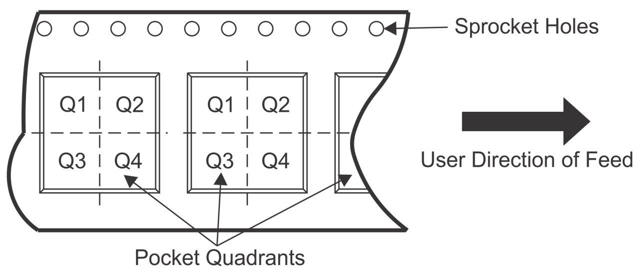


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

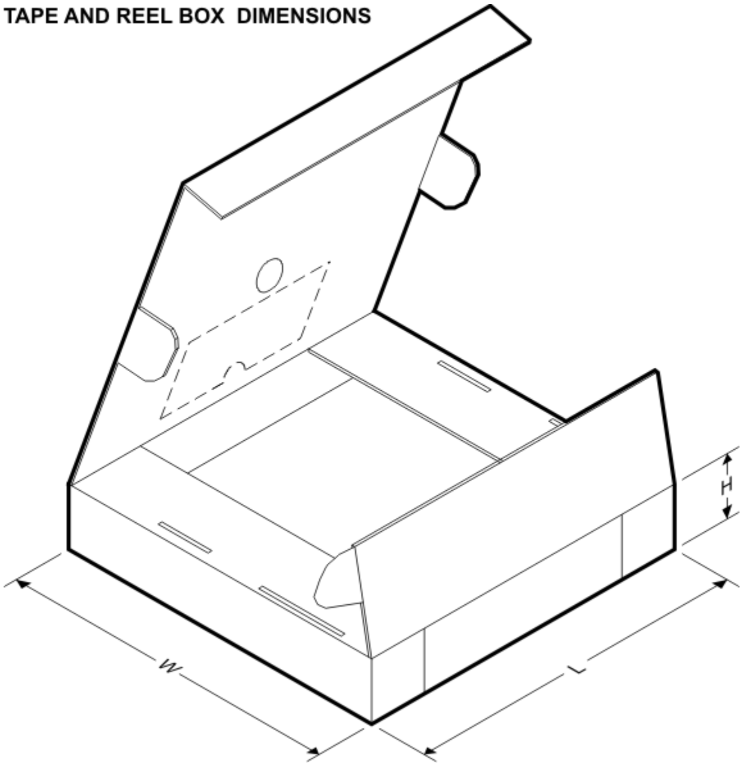
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM5102MM	VSSOP	DGS	10	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM5102MM/NOPB	VSSOP	DGS	10	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM5102MMX	VSSOP	DGS	10	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM5102MMX/NOPB	VSSOP	DGS	10	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM5102SD	WSON	DPR	10	1000	178.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1
LM5102SD/NOPB	WSON	DPR	10	1000	178.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1
LM5102SDX	WSON	DPR	10	4500	330.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1
LM5102SDX/NOPB	WSON	DPR	10	4500	330.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1

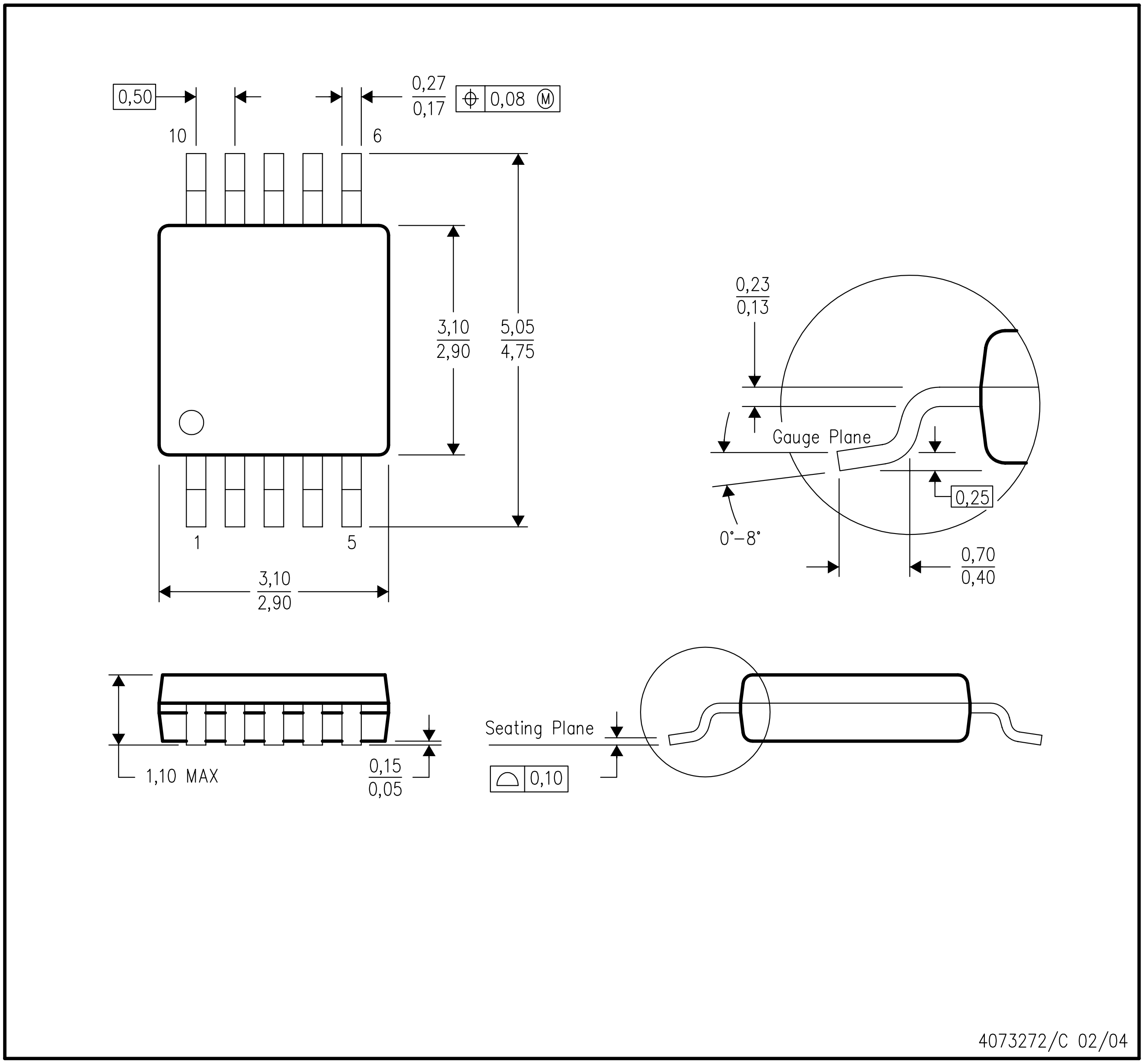
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

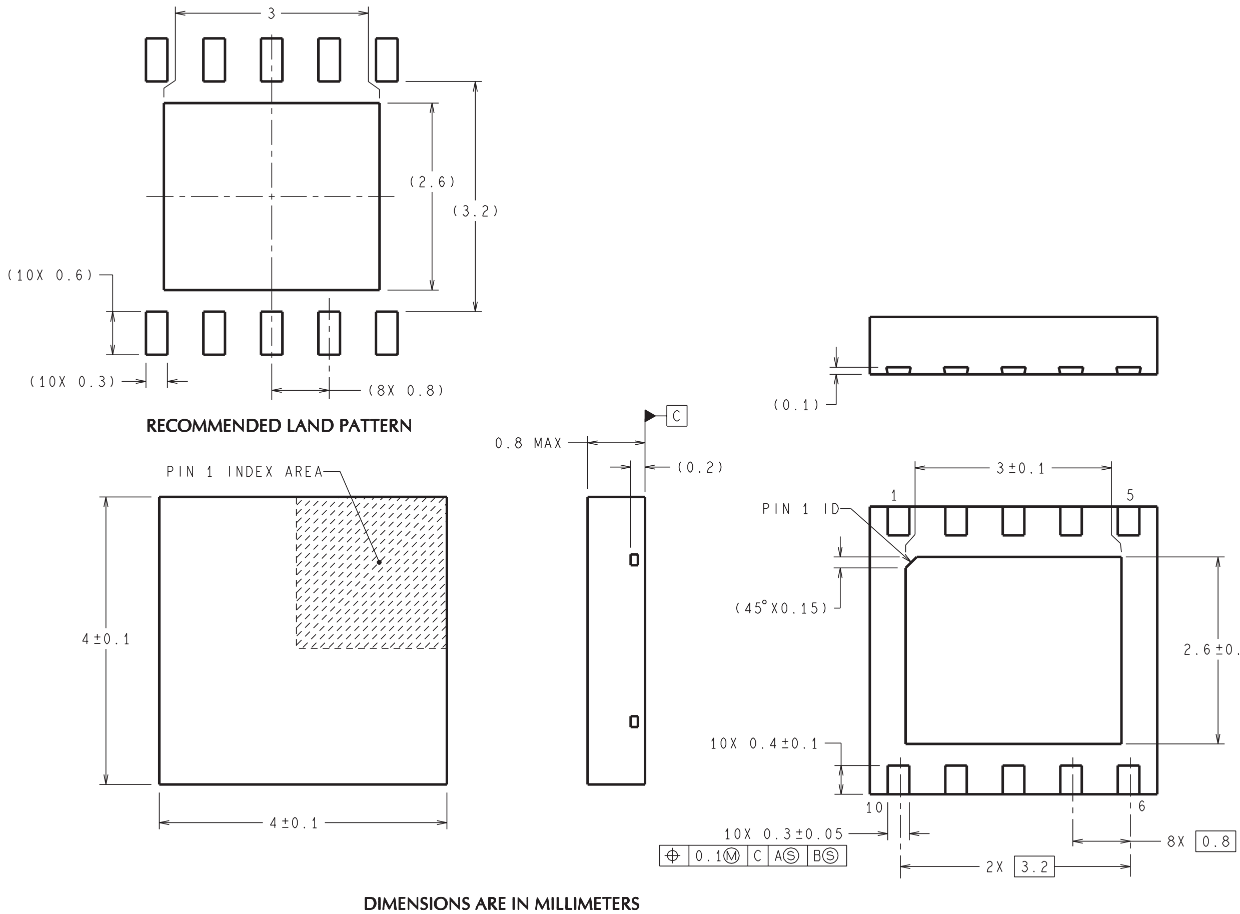
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM5102MM	VSSOP	DGS	10	1000	203.0	190.0	41.0
LM5102MM/NOPB	VSSOP	DGS	10	1000	203.0	190.0	41.0
LM5102MMX	VSSOP	DGS	10	3500	349.0	337.0	45.0
LM5102MMX/NOPB	VSSOP	DGS	10	3500	349.0	337.0	45.0
LM5102SD	WSON	DPR	10	1000	203.0	190.0	41.0
LM5102SD/NOPB	WSON	DPR	10	1000	203.0	190.0	41.0
LM5102SDX	WSON	DPR	10	4500	349.0	337.0	45.0
LM5102SDX/NOPB	WSON	DPR	10	4500	349.0	337.0	45.0

DGS (S–PDSO–G10) PLASTIC SMALL–OUTLINE PACKAGE



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. Falls within JEDEC MO–187 variation BA.

DPR0010A



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