# LM555QML Timer

**Check for Samples: LM555QML**

## FEATURES

- **Direct replacement for SE555/NE555**
- **Timing from microseconds through hours**
- **Operates in both astable and monostable modes**
- **Adjustable duty cycle**
- **Output can source or sink 200 mA**
- **Output and supply TTL compatible**
- **Temperature stability better than 0.005% per °C**
- **Normally on and normally off output**

## APPLICATIONS

- **Precision timing**
- **Pulse generation**
- **Sequential timing**
- **Time delay generation**
- **Pulse width modulation**
- **Pulse position modulation**
- **Linear ramp generator**

## DESCRIPTION

The LM555 is a highly stable device for generating accurate time delays or oscillation. Additional terminals are provided for triggering or resetting if desired. In the time delay mode of operation, the time is precisely controlled by one external resistor and capacitor. For astable operation as an oscillator, the free running frequency and duty cycle are accurately controlled with two external resistors and one capacitor. The circuit may be triggered and reset on falling waveforms, and the output circuit can source or sink up to 200mA or drive TTL circuits.

### Connection Diagram

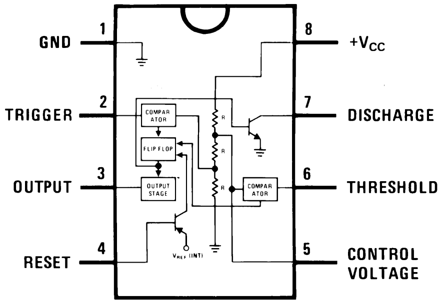


Figure 1. Dual-In-Line Package

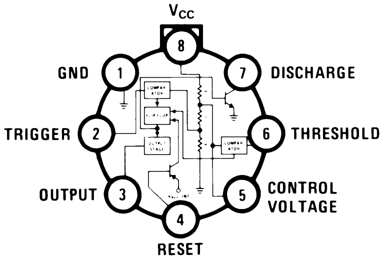
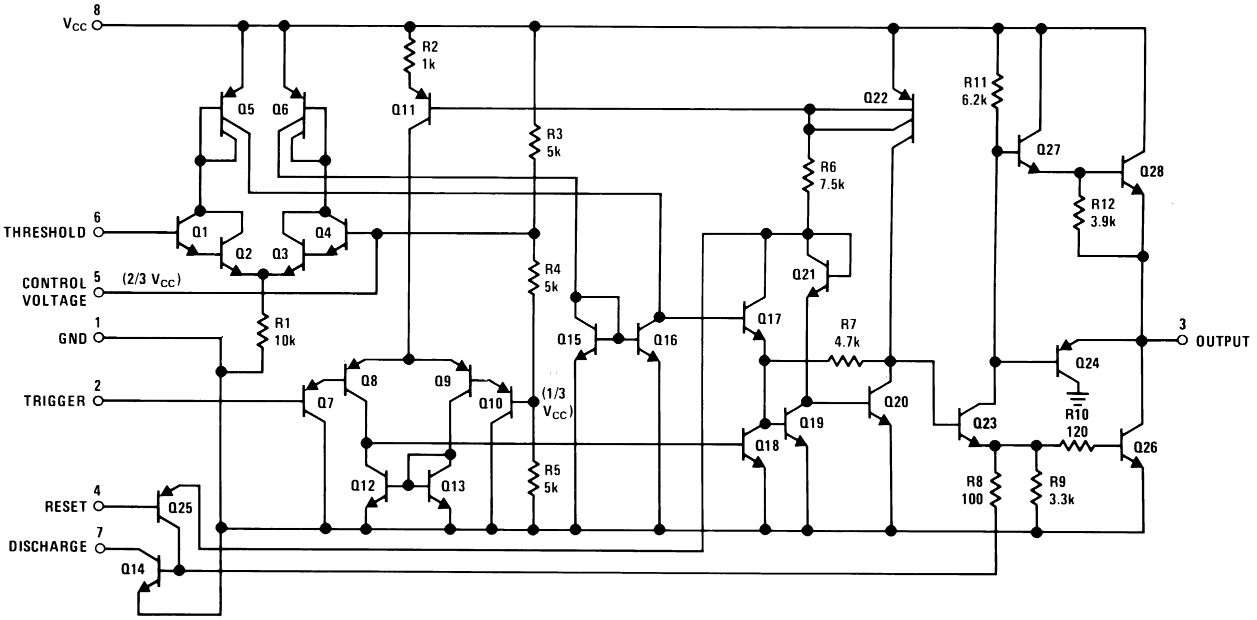


Figure 2. Metal Can Package

## Schematic Diagram



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## Absolute Maximum Ratings [(1)]

| | |
|---|---|
| Supply Voltage | +18V |
| Power Dissipation [(2)] | |
| Metal Can | 760 mW |
| CERDIP | 1180 mW |
| Operating Temperature Range | $-55°C \le T_A \le +125°C$ |
| Maximum Junction Temperature ($T_{Jmax}$) | +150°C |
| Storage Temperature Range | $-65°C \le T_A \le +150°C$ |
| Soldering Information (Soldering 10 Seconds) | 260°C |
| Thermal Resistance | |
| $\theta_{JA}$ | |
| CERDIP Still Air | 125°C/W |
| CERDIP 500LF / Min Air Flow | 71°C/W |
| Metal Can Still Air | 176°C/W |
| Metal Can 500LF / Min Air Flow | 96°C/W |
| $\theta_{JC}$ | |
| CERDIP | 20°C/W |
| Metal Can | 42°C/W |
| ESD Tolerance [(3)] | 500V |

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

(2) The maximum power dissipation must be derated at elevated temperatures and is dictated by $T_{Jmax}$ (maximum junction temperature), $\theta_{JA}$ (package junction to ambient thermal resistance), and $T_A$ (ambient temperature). The maximum allowable power dissipation at any temperature is $P_{Dmax} = (T_{Jmax} - T_A)/\theta_{JA}$ or the number given in the Absolute Maximum Ratings, whichever is lower.

(3) Human body model, 1.5KΩ in series with 100pF.

### Table 1. Quality Conformance Inspection

| Subgroup | Description | Temp °C |
|---|---|---|
| 1 | Static tests at | 25 |
| 2 | Static tests at | 125 |
| 3 | Static tests at | -55 |
| 4 | Dynamic tests at | 25 |
| 5 | Dynamic tests at | 125 |
| 6 | Dynamic tests at | -55 |
| 7 | Functional tests at | 25 |
| 8A | Functional tests at | 125 |
| 8B | Functional tests at | -55 |
| 9 | Switching tests at | 25 |
| 10 | Switching tests at | 125 |
| 11 | Switching tests at | -55 |
| 12 | Settling time at | 25 |
| 13 | Settling time at | 125 |
| 14 | Settling time at | -55 |

## Electrical Characteristics DC Parameters

The following conditions apply to all the following parameters, unless otherwise specified.
DC: +5V ≤ $V_{CC}$ ≤ +15V

| Symbol | Parameter | Conditions | Notes | Min | Max | Unit | Sub-groups |
|---|---|---|---|---|---|---|---|
| $I_{CCL}$ | Supply Current Low State | $V_{CC}$ = 5V, $R_L$ = ∞ | | | 5.0 | mA | 1 |
| | | $V_{CC}$ = 15V, $R_L$ = ∞ | | | 12.0 | mA | 1 |
| | | $V_{CC}$ = 18V, $R_L$ = ∞,<br>$V_2$ = $V_6$ = 18V | | | 18.5 | mA | 1 |
| $I_{L7}$ | Leakage Current Pin 7 | $V_{CC}$ = 18V, $V_7$ = 18V,<br>$V_2$ = $V_6$ = 0 | | | 100 | nA | 1 |
| $V_{Sat}$ | Saturation Voltage Pin 7 | $V_{CC}$ = 15V, $I_7$ = 15mA,<br>$V_2$ = $V_6$ = 12V | (1) | | 240 | mV | 1 |
| | | $V_{CC}$ = 4.5V, $I_7$ = 4.5mA | (1) | | 80 | mV | 1 |
| $V_{CO}$ | Control Voltage | $V_{CC}$ = 5V,<br>$V_2$ = $V_6$ = 4V | | 2.9 | 3.8 | V | 1, 2, 3 |
| | | $V_{CC}$ = 15V,<br>$V_2$ = $V_6$ = 12V | | 9.6 | 10.4 | V | 1, 2, 3 |
| $V_{Th}$ | Threshold Voltage | | | 9.5 | 10.5 | V | 1 |
| $I_{Th}$ | Threshold Current | $V_6$ = $V_{Th}$, $V_2$ = 7.5V,<br>$V_{Th}$ = $V_{Th}$ Test Measured Value | (2) | | 250 | nA | 1 |
| $I_{Trig}$ | Trigger Current | $V_2$ = 0 | | | 500 | nA | 1 |
| $V_{Trig}$ | Trigger Voltage | $V_{CC}$ = 15V | | 4.8 | 5.2 | V | 1 |
| | | | | 3.0 | 6.0 | V | 2, 3 |
| | | $V_{CC}$ = 5V | (3) | 1.45 | 1.9 | V | 1, 2, 3 |
| $I_{Reset}$ | Reset Current | $V_2$ = $V_6$ = Gnd | | | 0.4 | mA | 1 |
| $V_{Reset}$ | Reset Voltage | | | 0.4 | 1.0 | V | 1 |
| $V_{OL}$ | Output Voltage Drop Low | $V_{CC}$ = 5V, $I_{Sink}$ = +8mA,<br>$V_7$ = 5V, $V_6$ = 5V | | | 250 | mV | 1, 2, 3 |
| | | $V_{CC}$ = 15V, $I_{Sink}$ = +10mA,<br>$V_2$ = $V_6$ = 15V | | | 150 | mV | 1 |
| | | | | | 250 | mV | 2, 3 |
| | | $V_{CC}$ = 15V, $I_{Sink}$ = +50mA,<br>$V_2$ = $V_6$ = 15V | | | 500 | mV | 1 |
| | | | | | 800 | mV | 2, 3 |
| | | $V_{CC}$ = 15V, $I_{Sink}$ = +85mA,<br>$V_2$ = $V_6$ = 15V | | | 2.2 | V | 1, 2, 3 |
| $V_{OH}$ | Output Voltage Drop High | $V_{CC}$ = 15V, $I_{Source}$= 85mA | | 13 | | V | 1 |
| | | | | 12.75 | | V | 2, 3 |
| | | $V_{CC}$ = 5V, $I_{Source}$ = 85mA | | 3 | | V | 1 |
| | | | | 2.75 | | V | 2, 3 |
| A*f* | A Stable Frequency | | (4) | 45 | 51 | KHz | 1 |
| tE | Timing Error | $V_{CC}$ = 5V | (4) | | ±2 | % | 1, 2, 3 |
| | | $V_{CC}$ = 15V, 1KΩ ≤ $R_A$ ≤ 100KΩ,<br>Timing error decreases with an increase in $V_{CC}$ | (4) | | ±2 | % | 1, 2, 3 |
| ΔtE / $\Delta V_{CC}$ | Timing Drift with Supply | 5V ≤ $V_{CC}$ ≤ 15V | (4) | | 0.2 | % / V | 1, 2, 3 |

(1) No protection against excessive pin 7 current is necessary providing the package dissipation rating will not be exceeded.
(2) This will determine the maximum value of $R_A$ + $R_B$ for 15V operation. The maximum total ($R_A$ + $R_B$) is 20MΩ.
(3) Guaranteed by tests at $V_{CC}$ = 15V.
(4) Guaranteed parameter, not tested.

## Electrical Characteristics AC Parameters

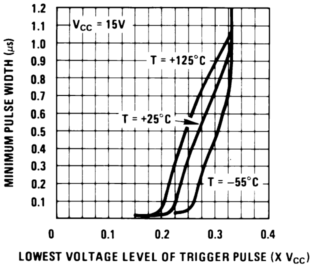
The following conditions apply to all the following parameters, unless otherwise specified.
AC: +5V ≤ $V_{CC}$ ≤ +15V

| Symbol | Parameter | Conditions | Notes | Min | Max | Unit | Sub-groups |
|---|---|---|---|---|---|---|---|
| tR | Rise Time | $V_{Trig}$ = 5V | (1) | | 250 | nS | 9, 10 |
| | | | (1) | | 400 | nS | 11 |
| tF | Fall Time | $V_{Trig}$ = 5V | (1) | | 250 | nS | 9, 10 |
| | | | (1) | | 400 | nS | 11 |

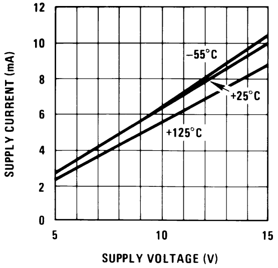
(1) Guaranteed parameter, not tested.

## Typical Performance Characteristics

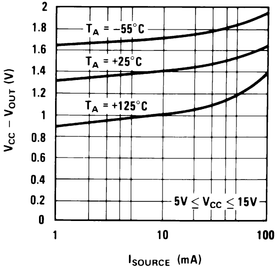
### Minimum Pulse Width Required for Triggering



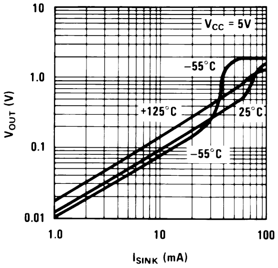
### Supply Current vs. Supply Voltage



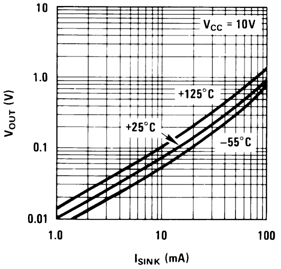
### High Output Voltage vs. Output Source Current



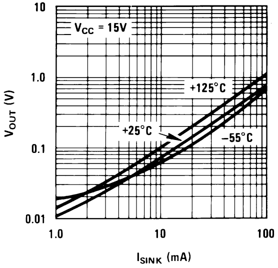
### Low Output Voltage vs. Output Sink Current



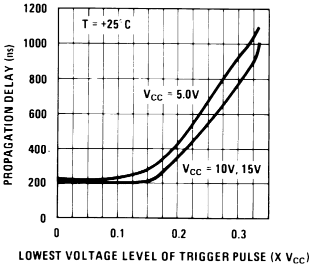
### Low Output Voltage vs. Output Sink Current



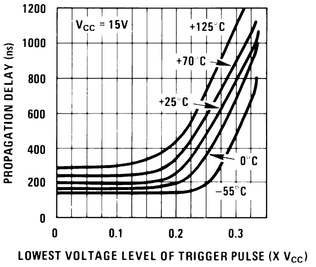
### Low Output Voltage vs. Output Sink Current



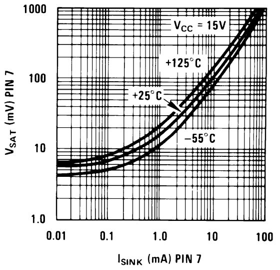
### Output Propagation Delay vs. Voltage Level of Trigger Pulse



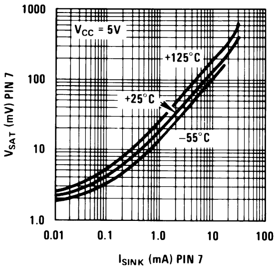
### Output Propagation Delay vs. Voltage Level of Trigger Pulse



### Discharge Transistor (Pin 7) Voltage vs. Sink Current



### Discharge Transistor (Pin 7) Voltage vs. Sink Current



## Applications Information

### MONOSTABLE OPERATION

In this mode of operation, the timer functions as a one-shot (Figure 3). The external capacitor is initially held discharged by a transistor inside the timer. Upon application of a negative trigger pulse of less than 1/3 $V_{CC}$ to pin 2, the flip-flop is set which both releases the short circuit across the capacitor and drives the output high.

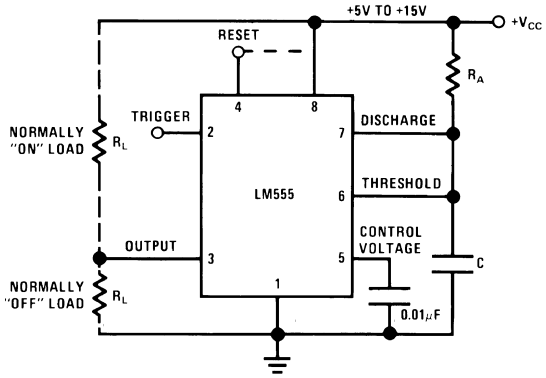
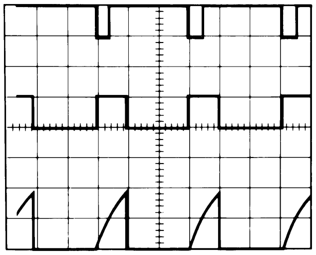


**Figure 3. Monostable**

The voltage across the capacitor then increases exponentially for a period of t = 1.1 $R_A$ C, at the end of which time the voltage equals 2/3 $V_{CC}$. The comparator then resets the flip-flop which in turn discharges the capacitor and drives the output to its low state. Figure 4 shows the waveforms generated in this mode of operation. Since the charge and the threshold level of the comparator are both directly proportional to supply voltage, the timing interval is independent of supply.



$V_{CC}$ = 5V
TIME = 0.1 ms/DIV.
$R_A$ = 9.1kΩ
C = 0.01μF

Top Trace: Input 5V/Div.
Middle Trace: Output 5V/Div.
Bottom Trace: Capacitor Voltage 2V/Div.

**Figure 4. Monostable Waveforms**

During the timing cycle when the output is high, the further application of a trigger pulse will not effect the circuit so long as the trigger input is returned high at least 10μs before the end of the timing interval. However the circuit can be reset during this time by the application of a negative pulse to the reset terminal (pin 4). The output will then remain in the low state until a trigger pulse is again applied.

When the reset function is not in use, it is recommended that it be connected to $V_{CC}$ to avoid any possibility of false triggering.

Figure 5 is a nomograph for easy determination of R, C values for various time delays.

**NOTE:** In monostable operation, the trigger should be driven high before the end of timing cycle.

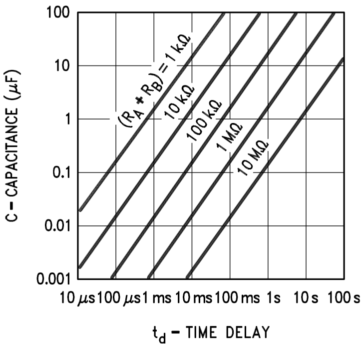


Figure 5. Time Delay

## ASTABLE OPERATION

If the circuit is connected as shown in Figure 6 (pins 2 and 6 connected) it will trigger itself and free run as a multivibrator. The external capacitor charges through $R_A$ + $R_B$ and discharges through $R_B$. Thus the duty cycle may be precisely set by the ratio of these two resistors.

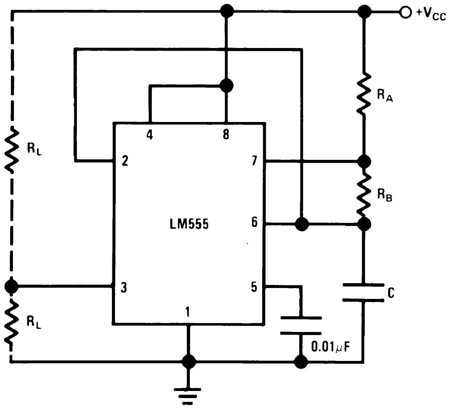
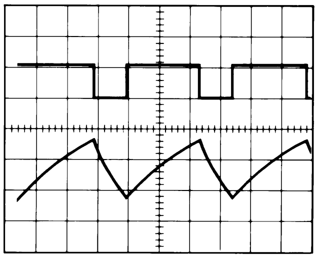


Figure 6. Astable

In this mode of operation, the capacitor charges and discharges between 1/3 $V_{CC}$ and 2/3 $V_{CC}$. As in the triggered mode, the charge and discharge times, and therefore the frequency are independent of the supply voltage.

Figure 7 shows the waveforms generated in this mode of operation.



$V_{CC}$ = 5V
TIME = 20μs/DIV.
$R_A$ = 3.9kΩ
$R_B$ = 3kΩ
C = 0.01μF

Top Trace: Output 5V/Div.
Bottom Trace: Capacitor Voltage 1V/Div.

Figure 7. Astable Waveforms

The charge time (output high) is given by:

$$t_1 = 0.693\,(R_A + R_B)\,C \tag{1}$$

And the discharge time (output low) by:

$$t_2 = 0.693\,(R_B)\,C \tag{2}$$

Thus the total period is:

$$T = t_1 + t_2 = 0.693\,(R_A + 2R_B)\,C \tag{3}$$

The frequency of oscillation is:

$$f = \frac{1}{T} = \frac{1.44}{(R_A + 2\,R_B)\,C} \tag{4}$$

Figure 8 may be used for quick determination of these RC values.

The duty cycle is:

$$D = \frac{R_B}{R_A + 2R_B} \tag{5}$$

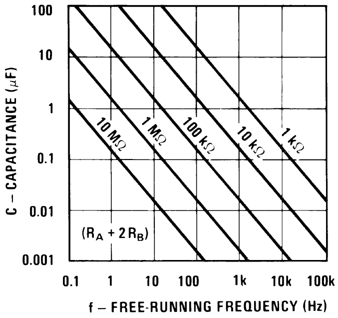
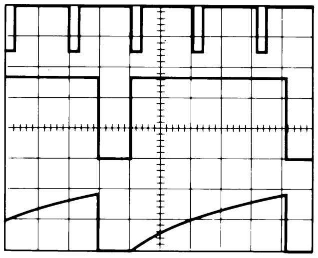


**Figure 8. Free Running Frequency**

## FREQUENCY DIVIDER

The monostable circuit of Figure 3 can be used as a frequency divider by adjusting the length of the timing cycle. Figure 9 shows the waveforms generated in a divide by three circuit.



$V_{CC}$ = 5V
TIME = 20μs/DIV.
$R_A$ = 9.1kΩ
C = 0.01μF

Top Trace: Input 4V/Div.
Middle Trace: Output 2V/Div.
Bottom Trace: Capacitor 2V/Div.

**Figure 9. Frequency Divider**

## PULSE WIDTH MODULATOR

When the timer is connected in the monostable mode and triggered with a continuous pulse train, the output pulse width can be modulated by a signal applied to pin 5. Figure 10 shows the circuit, and in Figure 11 are some waveform examples.

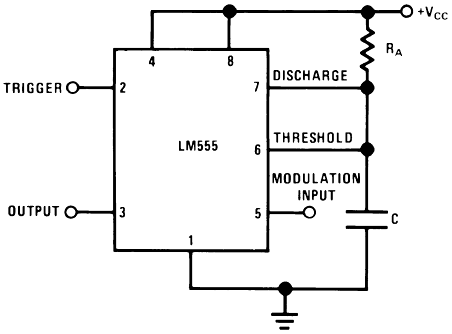
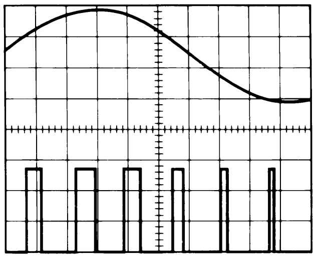


Figure 10. Pulse Width Modulator



$V_{CC}$ = 5V Top Trace: Modulation 1V/Div.
TIME = 0.2 ms/DIV. Bottom Trace: Output Voltage 2V/Div.
$R_A$ = 9.1kΩ
C = 0.01μF

Figure 11. Pulse Width Modulator

## PULSE POSITION MODULATOR

This application uses the timer connected for astable operation, as in Figure 12, with a modulating signal again applied to the control voltage terminal. The pulse position varies with the modulating signal, since the threshold voltage and hence the time delay is varied. Figure 13 shows the waveforms generated for a triangle wave modulation signal.

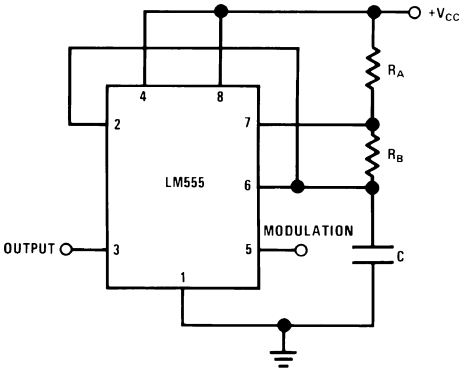
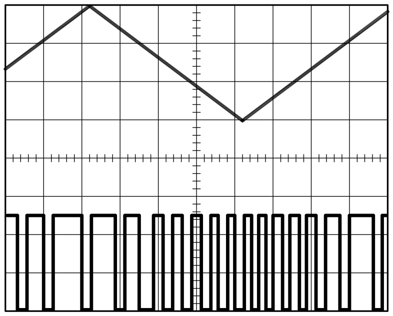


Figure 12. Pulse Position Modulator



$V_{CC} = 5V$ Top Trace: Modulation Input 1V/Div.
TIME = 0.1 ms/DIV. Bottom Trace: Output 2V/Div.
$R_A = 3.9k\Omega$
$R_B = 3k\Omega$
$C = 0.01\mu F$

**Figure 13. Pulse Position Modulator**

## LINEAR RAMP

When the pullup resistor, $R_A$, in the monostable circuit is replaced by a constant current source, a linear ramp is generated. Figure 14 shows a circuit configuration that will perform this function.

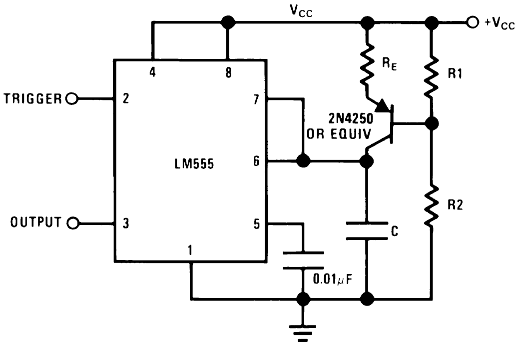


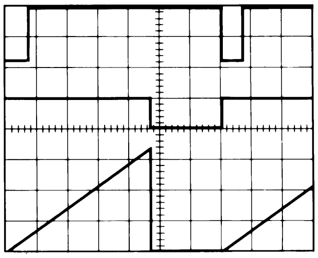
**Figure 14. Linear Ramp Circuit Configuration**

Figure 15 shows waveforms generated by the linear ramp.

The time interval is given by:

$$T = \frac{2/3\, V_{CC}\, R_E\, (R_1 + R_2)\, C}{R_1\, V_{CC} - V_{BE}\, (R_1 + R_2)} \qquad V_{BE} \cong 0.6V \tag{6}$$

$$V_{BE} \approx 0.6V \tag{7}$$



$V_{CC}$ = 5V Top Trace: Input 3V/Div.
TIME = 20μs/DIV. Middle Trace: Output 5V/Div.
$R_1$ = 47kΩ Bottom Trace: Capacitor Voltage 1V/Div.
$R_2$ = 100kΩ
$R_E$ = 2.7 kΩ
C = 0.01 μF

**Figure 15. Linear Ramp**

## 50% DUTY CYCLE OSCILLATOR

For a 50% duty cycle, the resistors $R_A$ and $R_B$ may be connected as in Figure 16. The time period for the output high is the same as previous, $t_1 = 0.693\ R_A\ C$. For the output low it is $t_2$ =

$$\left[(R_A R_B)/(R_A + R_B)\right] C\ \ell n \left[\frac{R_B - 2R_A}{2R_B - R_A}\right] \tag{8}$$

Thus the frequency of oscillation is

$$f = \frac{1}{t_1 + t_2} \tag{9}$$

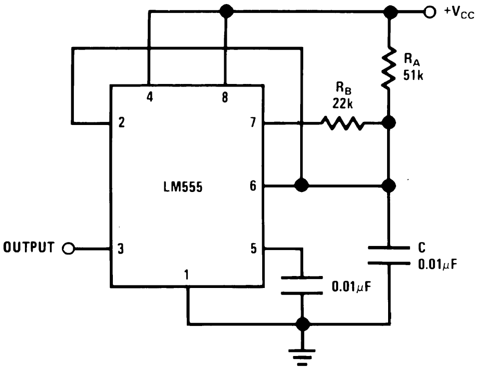


**Figure 16. 50% Duty Cycle Oscillator**

Note that this circuit will not oscillate if $R_B$ is greater than 1/2 $R_A$ because the junction of $R_A$ and $R_B$ cannot bring pin 2 down to 1/3 $V_{CC}$ and trigger the lower comparator.

## ADDITIONAL INFORMATION

Adequate power supply bypassing is necessary to protect associated circuitry. Minimum recommended is 0.1μF in parallel with 1μF electrolytic.

Lower comparator storage time can be as long as 10μs when pin 2 is driven fully to ground for triggering. This limits the monostable pulse width to 10μs minimum.

Delay time reset to output is 0.47μs typical. Minimum reset pulse width must be 0.3μs, typical.

Pin 7 current switches within 30ns of the output (pin 3) voltage.

## Table 2. Revision History

| Date Released | Revision | Section | Originator | Changes |
|---|---|---|---|---|
| 08/04/05 | A | New Release to corporate format | L. Lytle | 1 MDS datasheet converted into once datasheet in the corporate format. Removed drift endpoints since not performed on 883 product. MNLM555-X Rev 0B0 to be archived |
| 04/10/06 | B | Ordering Information Table | R. Malone | NS Package Number and Description was referenced incorrectly. Revision A will be Archived. |
| 07/25/06 | C | Applications Information, page 8 | R. Malone | Correct a typo in the paragraph after figure 1 (change the word internal to interval) to reflect same change made to Commercial data sheet. Revision B will be Archived. |

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish | MSL Peak Temp (3) | Samples (Requires Login) |
|---|---|---|---|---|---|---|---|---|---|
| LM555H/883 | ACTIVE | TO-99 | LMC | 8 | 20 | TBD | POST-PLATE | Level-1-NA-UNLIM | |
| LM555J/883 | ACTIVE | CDIP | NAB | 8 | 40 | TBD | A42 SNPB | Level-1-NA-UNLIM | |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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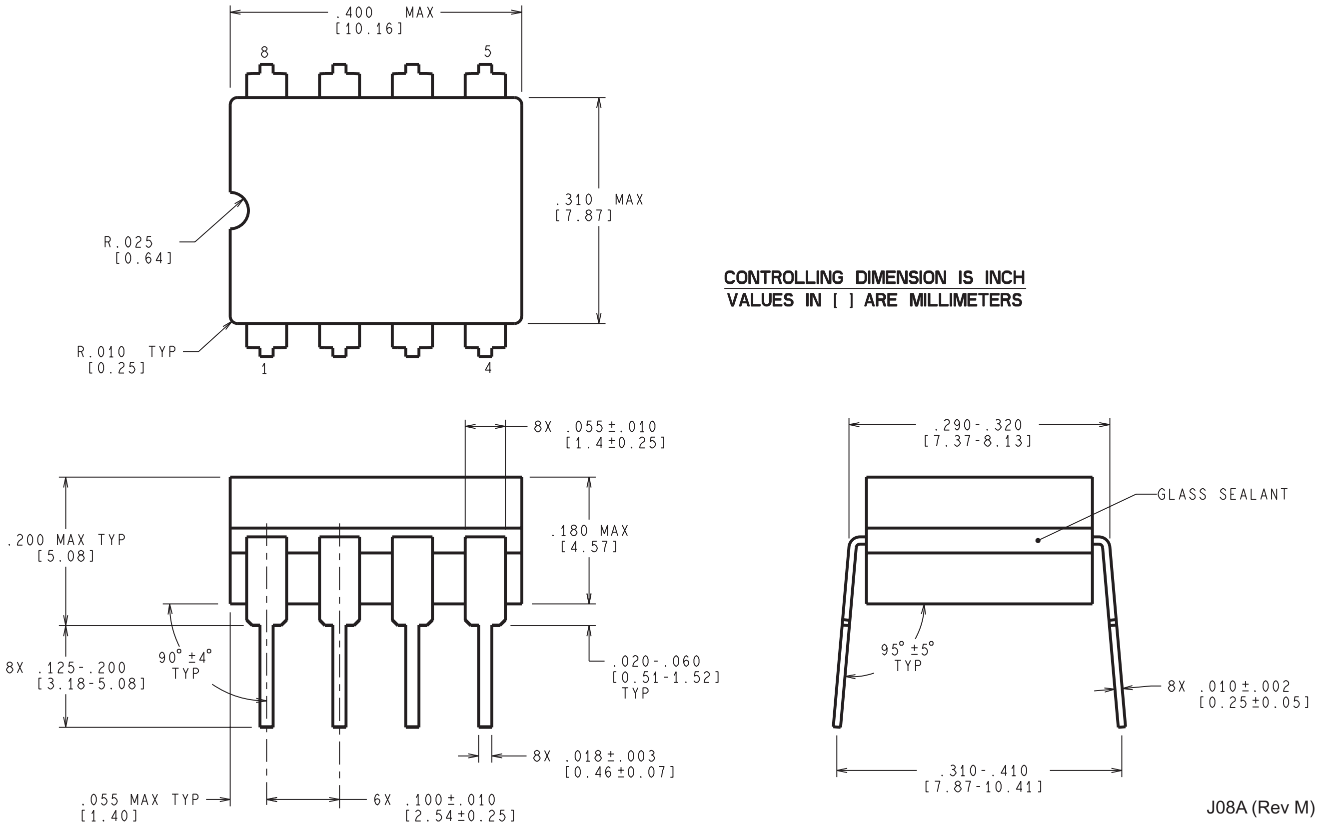
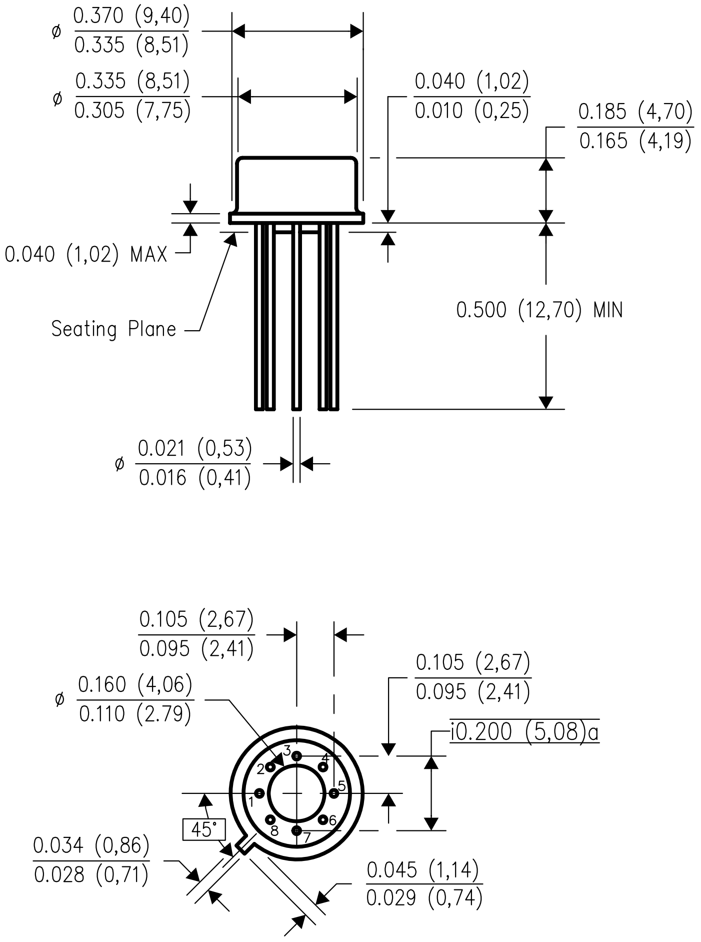
# NAB0008A



CONTROLLING DIMENSION IS INCH
VALUES IN [ ] ARE MILLIMETERS

J08A (Rev M)

# LMC (O–MBCY–W8) METAL CYLINDRICAL PACKAGE



4202483/B 09/07

NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Leads in true position within 0.010 (0,25) R @ MMC at seating plane.
- D. Pin numbers shown for reference only. Numbers may not be marked on package.
- E. Falls within JEDEC MO–002/TO–99.

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