LM613 Dual Operational Amplifiers, Dual Comparators, and Adjustable Reference

Check for Samples: LM613

FEATURES

OP AMP

- **Low operating current (Op Amp): 300 µA**
- **Wide supply voltage range: 4V to 36V**
- **Wide common-mode range: V^- to (V^+ − 1.8V)**
- **Wide differential input voltage: ±36V**
- **Available in plastic package rated for Military Temp. Range Operation**

REFERENCE

- **Adjustable output voltage: 1.2V to 6.3V**
- **Tight initial tolerance available: ±0.6%**
- **Wide operating current range: 17 µA to 20 mA**
- **Tolerant of load capacitance**

APPLICATIONS

- **Transducer bridge driver**
- **Process and mass flow control systems**
- **Power supply voltage monitor**
- **Buffered voltage references for A/D's**

DESCRIPTION

The LM613 consists of dual op-amps, dual comparators, and a programmable voltage reference in a 16-pin package. The op-amps out-performs most single-supply op-amps by providing higher speed and bandwidth along with low supply current. This device was specifically designed to lower cost and board space requirements in transducer, test, measurement, and data acquisition systems.

Combining a stable voltage reference with wide output swing op-amps makes the LM613 ideal for single supply transducers, signal conditioning and bridge driving where large common-mode-signals are common. The voltage reference consists of a reliable band-gap design that maintains low dynamic output impedance (1Ω typical), excellent initial tolerance (0.6%), and the ability to be programmed from 1.2V to 6.3V via two external resistors. The voltage reference is very stable even when driving large capacitive loads, as are commonly encountered in CMOS data acquisition systems.

As a member of National's Super-Block™ family, the LM613 is a space-saving monolithic alternative to a multi-chip solution, offering a high level of integration without sacrificing performance.

Connection Diagram

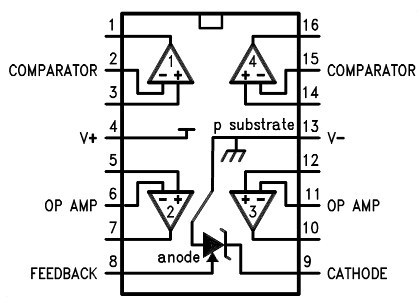


Figure 1. Top View

Figure 2. E Package Pinout

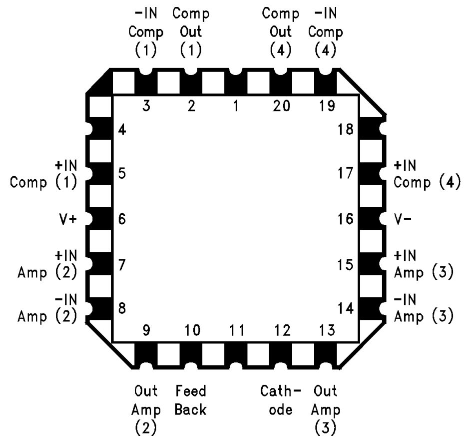
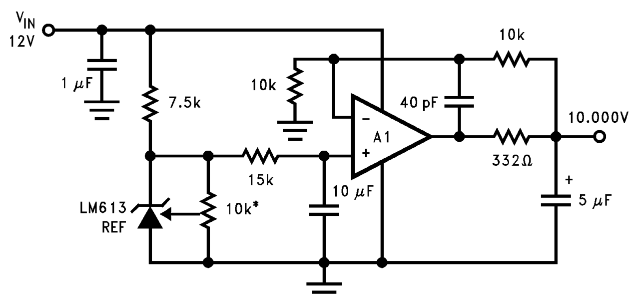


Figure 3. Ultra Low Noise, 10.00V Reference. Total output noise is typically 14 μV$_{RMS}$.



*10k must be low
t.c. trimpot

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings [1]

Voltage on Any Pin Except V_R (referred to V^-pin) [2] [3]	36V (Max) −0.3V (Min)
Current through Any Input Pin & V_R Pin	±20 mA
Differential Input Voltage Military and Industrial Commercial	±36V ±32V
Storage Temperature Range	−65°C ≤ T_J ≤ +150°C
Maximum Junction Temp. [4]	150°C
Thermal Resistance, Junction-to-Ambient [5] N Package WM Package	100°C/W 150°C/W
Soldering Information (10 Sec.) N Package WM Package	260°C 220°C
ESD Tolerance [6]	±1 kV

(1) Absolute maximum ratings indicate limits beyond which damage to the component may occur. Electrical specifications do not apply when operating the device beyond its rated operating conditions.
(2) Input voltage above V^+ is allowed. As long as one input pin voltage remains inside the common-mode range, the comparator will deliver the correct output.
(3) More accurately, it is excessive current flow, with resulting excess heating, that limits the voltages on all pins. When any pin is pulled a diode drop below V^-, a parasitic NPN transistor turns ON. No latch-up will occur as long as the current through that pin remains below the Maximum Rating. Operation is undefined and unpredictable when any parasitic diode or transistor is conducting.
(4) Simultaneous short-circuit of multiple comparators while using high supply voltages may force junction temperature above maximum, and thus should not be continuous.
(5) Junction temperature may be calculated using $T_J = T_A + P_D \theta_{JA}$. The given thermal resistance is worst-case for packages in sockets in still air. For packages soldered to copper-clad board with dissipation from one comparator or reference output transistor, nominal θ_{JA} is 90°C/W for the N package, and 135°C/W for the WM package.
(6) Human body model, 100 pF discharged through a 1.5 kΩ resistor.

Operating Temperature Range

LM613AI, LM613BI:	−40°C to +85°C
LM613AM, LM613M:	−55°C to +125°C
LM613C:	0°C ≤ T_J ≤ +70°C

Electrical Characteristics

These specifications apply for $V^- = GND = 0V$, $V^+ = 5V$, $V_{CM} = V_{OUT} = 2.5V$, $I_R = 100\ \mu A$, FEEDBACK pin shorted to GND, unless otherwise specified. Limits in standard typeface are for $T_J = 25°C$; limits in **boldface type** apply over the **Operating Temperature Range**.

Symbol	Parameter	Conditions	Typical (1)	LM613AM LM613AI Limits (2)	LM613M LM613I LM613C Limits (2)	Units
I_S	Total Supply Current	$R_{LOAD} = \infty$,	450	940	1000	μA (Max)
		$4V \le V^+ \le 36V$ (32V for LM613C)	**550**	**1000**	**1070**	μA (Max)
V_S	Supply Voltage Range		2.2	2.8	2.8	V (Min)
			2.9	**3**	**3**	V (Min)
			46	36	32	V (Max)
			43	**36**	**32**	V (Max)
OPERATIONAL AMPLIFIERS						
V_{OS1}	V_{OS} Over Supply	$4V \le V^+ \le 36V$	1.5	3.5	5.0	mV (Max)
		($4V \le V^+ \le 32V$ for LM613C)	**2.0**	**6.0**	**7.0**	mV (Max)
V_{OS2}	V_{OS} Over V_{CM}	$V_{CM} = 0V$ through $V_{CM} =$	1.0	3.5	5.0	mV (Max)
		$(V^+ - 1.8V)$, $V^+ = 30V$, $V^- = 0V$	**1.5**	**6.0**	**7.0**	mV (Max)
$\frac{V_{OS3}}{\Delta T}$	Average V_{OS} Drift	(2)	**15**			μV/°C (Max)
I_B	Input Bias Current		10	25	35	nA (Max)
			11	**30**	**40**	nA (Max)
I_{OS}	Input Offset Current		0.2	4	4	nA (Max)
			0.3	**5**	**5**	nA (Max)
$\frac{I_{OS1}}{\Delta T}$	Average Offset Current		**4**			pA/°C
R_{IN}	Input Resistance	Differential	1000			MΩ
C_{IN}	Input Capacitance	Common-Mode	6			pF
e_n	Voltage Noise	f = 100 Hz, Input Referred	74			$nV/\sqrt{Hz}$
I_n	Current Noise	f = 100 Hz, Input Referred	58			$fA/\sqrt{Hz}$
CMRR	Common-Mode	$V^+ = 30V$, $0V \le V_{CM} \le (V^+ - 1.8V)$	95	80	75	dB (Min)
	Rejection Ratio	$CMRR = 20 \log (\Delta V_{CM}/\Delta V_{OS})$	**90**	**75**	**70**	dB (Min)
PSRR	Power Supply	$4V \le V^+ \le 30V$, $V_{CM} = V^+/2$,	110	80	75	dB (Min)
	Rejection Ratio	$PSRR = 20 \log (\Delta V^+/V_{OS})$	**100**	**75**	**70**	dB (Min)
A_V	Open Loop	$R_L = 10\ k\Omega$ to GND, $V^+ = 30V$,	500	100	94	V/mV
	Voltage Gain	$5V \le V_{OUT} \le 25V$	**50**	**40**	**40**	(Min)
SR	Slew Rate	$V^+ = 30V$ (3)	0.70	0.55	0.50	V/μs
			0.65	**0.45**	**0.45**	
GBW	Gain Bandwidth	$C_L = 50\ pF$	0.8			MHz
			0.5			MHz

(1) Typical values in standard typeface are for $T_J = 25°C$; values in **bold face type** apply for the full operating temperature range. These values represent the most likely parametric norm.
(2) All limits are guaranteed at room temperature (standard type face) or at operating temperature extremes **(bold type face)**.
(3) Slew rate is measured with the op amp in a voltage follower configuration. For rising slew rate, the input voltage is driven from 5V to 25V, and the output voltage transition is sampled at 10V and @ 20V. For falling slew rate, the input voltage is driven from 25V to 5V, and the output voltage transition is sampled at 20V and 10V.

Electrical Characteristics (continued)

These specifications apply for $V^- = GND = 0V$, $V^+ = 5V$, $V_{CM} = V_{OUT} = 2.5V$, $I_R = 100\ \mu A$, FEEDBACK pin shorted to GND, unless otherwise specified. Limits in standard typeface are for $T_J = 25°C$; limits in **boldface type** apply over the **Operating Temperature Range**.

Symbol	Parameter	Conditions	Typical (1)	LM613AM LM613AI Limits (2)	LM613M LM613I LM613C Limits (2)	Units
V_{O1}	Output Voltage	R_L = 10 kΩ to GND,	$V^+ - 1.4$	$V^+ - 1.7$	$V^+ - 1.8$	V (Min)
	Swing High	V^+ = 36V (32V for LM613C)	**$V^+ - 1.6$**	**$V^+ - 1.9$**	**$V^+ - 1.9$**	V (Min)
V_{O2}	Output Voltage	R_L = 10 kΩ to V^+,	$V^- + 0.8$	$V^- + 0.9$	$V^- + 0.95$	V (Max)
	Swing Low	V^+ = 36V (32V for LM613C)	**$V^- + 0.9$**	**$V^- + 1.0$**	**$V^- + 1.0$**	V (Max)
I_{OUT}	Output Source Current	V_{OUT} = 2.5V, V^+_{IN} = 0V,	25	20	16	mA (Min)
		V^-_{IN} = −0.3V	**15**	**13**	**13**	mA (Min)
I_{SINK}	Output Sink Current	V_{OUT} = 1.6V, V^+_{IN} = 0V,	17	14	13	mA (Min)
		V^-_{IN} = 0.3V	**9**	**8**	**8**	mA (Min)
I_{SHORT}	Short Circuit Current	V_{OUT} = 0V,V^+_{IN} = 3V,	30	50	50	mA (Max)
		V^-_{IN} = 2V	**40**	**60**	**60**	mA (Max)
		V_{OUT} = 5V, V^+_{IN} = 2V,	30	60	70	mA (Max)
		V^-_{IN} = 3V	**32**	**80**	**90**	mA (Max)
COMPARATORS						
V_{OS}	Offset Voltage	4V ≤ V^+ ≤ 36V (32V for LM613C),	1.0	3.0	5.0	mV (Max)
		R_L = 15 kΩ	**2.0**	**6.0**	**7.0**	mV (Max)
$\frac{V_{OS}}{V_{CM}}$	Offset Voltage	0V ≤ V_{CM} ≤ 36V	1.0	3.0	5.0	mV (Max)
	over V_{CM}	V^+ = 36V, (32V for LM613C)	**1.5**	**6.0**	**7.0**	mV (Max)
$\frac{V_{OS}}{\Delta T}$	Average Offset		**15**			μV/°C
	Voltage Drift					(Max)
I_B	Input Bias Current		5	25	35	nA (Max)
			8	**30**	**40**	nA (Max)
I_{OS}	Input Offset Current		0.2	4	4	nA (Max)
			0.3	**5**	**5**	nA (Max)
A_V	Voltage Gain	R_L = 10 kΩ to 36V (32V for LM613C)	500			V/mV
		2V ≤ V_{OUT} ≤ 27V	**100**			V/mV
t_r	Large Signal	V^+_{IN} = 1.4V, V^-_{IN} = TTL Swing,	1.5			μs
	Response Time	R_L = 5.1 kΩ	**2.0**			μs
I_{SINK}	Output Sink Current	V^+_{IN} = 0V, V^-_{IN} = 1V,	20	10	10	mA (Min)
		V_{OUT} = 1.5V	**13**	**8**	**8**	mA (Min)
		V_{OUT} = 0.4V	2.8	1.0	0.8	mA (Min)
			2.4	**0.5**	**0.5**	mA (Min)
I_{LEAK}	Output Leakage	V^+_{IN} = 1V, V^-_{IN} = 0V,	0.1	10	10	μA (Max)
	Current	V_{OUT} = 36V (32V for LM613C)	**0.2**			μA (Max)
VOLTAGE REFERENCE						
V_R	Voltage Reference	(4)	1.244	1.2365	1.2191	V (Min)
				1.2515	1.2689	V (Max)
				(±0.6%)	(±2%)	

(4) V_R is the Cathode-to-feedback voltage, nominally 1.244V.

Electrical Characteristics (continued)

These specifications apply for V^- = GND = 0V, V^+ = 5V, V_{CM} = V_{OUT} = 2.5V, I_R = 100 μA, FEEDBACK pin shorted to GND, unless otherwise specified. Limits in standard typeface are for T_J = 25°C; limits in **boldface type** apply over the **Operating Temperature Range**.

Symbol	Parameter	Conditions	Typical (1)	LM613AM LM613AI Limits (2)	LM613M LM613I LM613C Limits (2)	Units
$\frac{\Delta V_R}{\Delta T}$	Average Temp. Drift	(5)	**10**	**80**	**150**	ppm/°C (Max)
$\frac{\Delta V_R}{\Delta T_J}$	Hysteresis	(6)	**3.2**			μV/°C
$\frac{\Delta V_R}{\Delta I_R}$	V_R Change	$V_{R(100\ \mu A)} - V_{R(17\ \mu A)}$	0.05	1	1	mV (Max)
	with Current		**0.1**	**1.1**	**1.1**	mV (Max)
		$V_{R(10\ mA)} - V_{R(100\ \mu A)}$	1.5	5	5	mV (Max)
		(7)	**2.0**	**5.5**	**5.5**	mV (Max)
R	Resistance	$\Delta V_{R(10 \rightarrow 0.1\ mA)}$/9.9 mA	**0.2**	**0.56**	**0.56**	Ω (Max)
		$\Delta V_{R(100 \rightarrow 17\ \mu A)}$/83 μA	**0.6**	**13**	**13**	Ω (Max)
$\frac{V_R}{\Delta V_{RO}}$	V_R Change	$V_{R(Vro = Vr)} - V_{R(Vro = 6.3V)}$	2.5	7	7	mV (Max)
	with High V_{RO}	(5.06V between Anode and	**2.8**	**10**	**10**	mV (Max)
		FEEDBACK)				
$\frac{V_R}{\Delta V^+}$	V_R Change with	$V_{R(V+ = 5V)} - V_{R(V+ = 36V)}$	0.1	1.2	1.2	mV (Max)
	V_{ANODE} Change	(V^+ = 32V for LM613C)	**0.1**	**1.3**	**1.3**	mV (Max)
		$V_{R(V+ = 5V)} - V_{R(V+ = 3V)}$	0.01	1	1	mV (Max)
			0.01	**1.5**	**1.5**	mV (Max)
I_{FB}	FEEDBACK Bias	$V_{ANODE} \le V_{FB} \le$ 5.06V	22	35	50	nA (Max)
	Current		**29**	**40**	**55**	nA (Max)
e_n	V_R Noise	10 Hz to 10 kHz,	30			μV_{RMS}
		$V_{RO} = V_R$				

(5) Average reference drift is calculated from the measurement of the reference voltage at 25°C and at the temperature extremes. The drift, in ppm/°C, is $10^6 \bullet \Delta V_R/(V_{R[25°C]} \bullet \Delta T_J)$, where ΔV_R is the lowest value subtracted from the highest, $V_{R[25°C]}$ is the value at 25°C, and ΔT_J is the temperature range. This parameter is guaranteed by design and sample testing.
(6) Hysteresis is the change in V_R caused by a change in T_J, after the reference has been “dehysterized”. To dehysterize the reference; that is minimize the hysteresis to the typical value, its junction temperature should be cycled in the following pattern, spiraling in toward 25°C: 25°C, 85°C, −40°C, 70°C, 0°C, 25°C.
(7) Low contact resistance is required for accurate measurement.

Simplified Schematic Diagrams

Figure 4. Op Amp

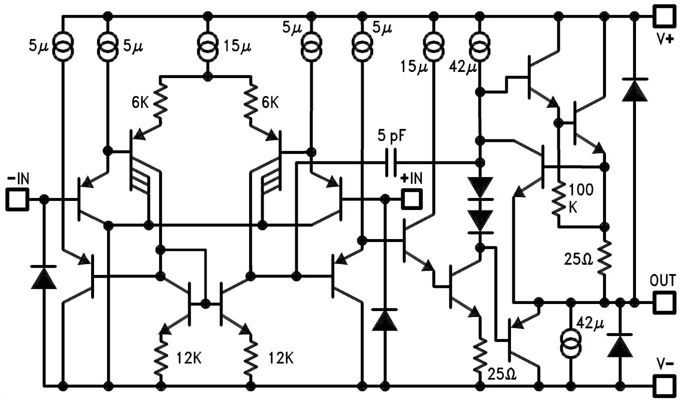


Figure 5. Comparator

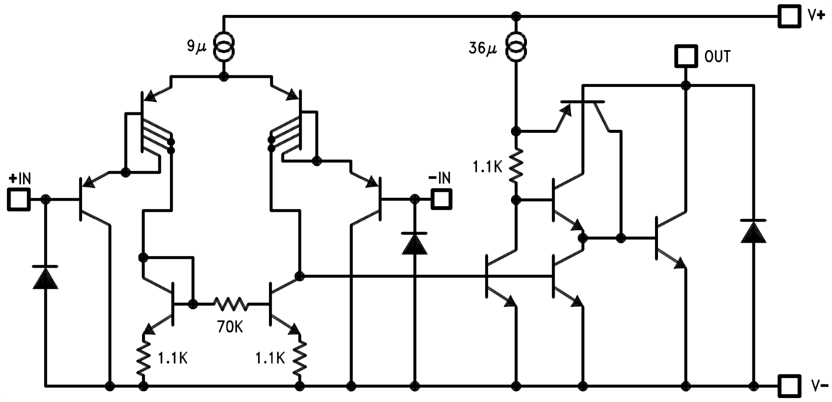
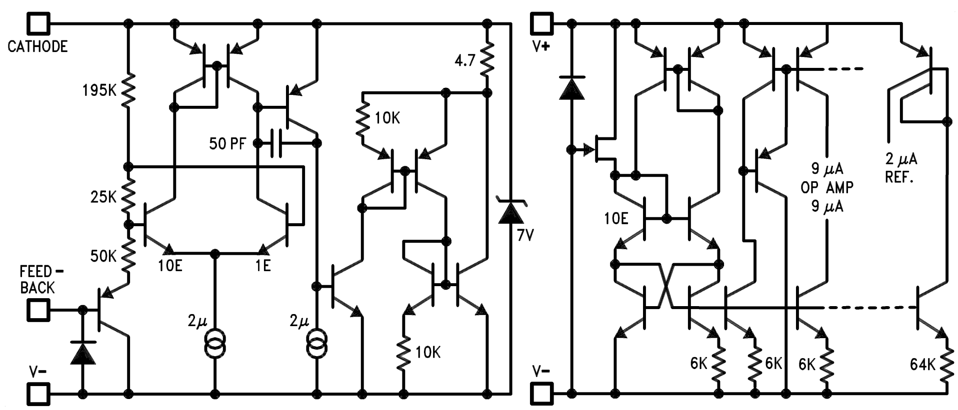


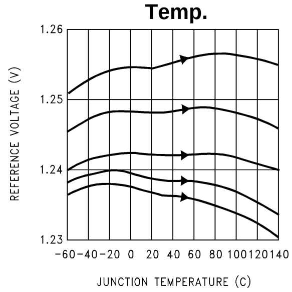
Figure 6. Reference/Bias



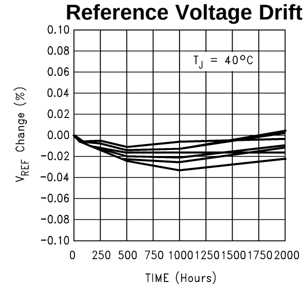
Typical Performance Characteristics (Reference)

T_J = 25°C, FEEDBACK pin shorted to V^- = 0V, unless otherwise noted

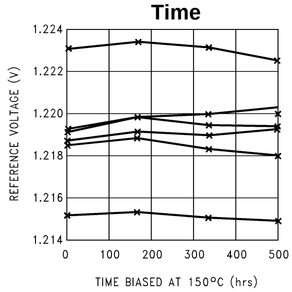
Reference Voltage vs Temp.



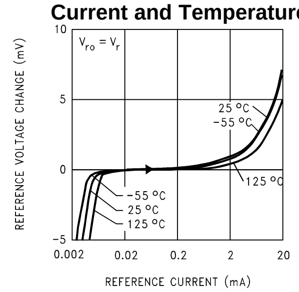
Reference Voltage Drift



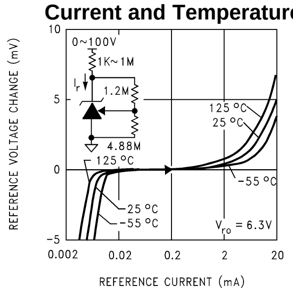
Accelerated Reference Voltage Drift vs Time



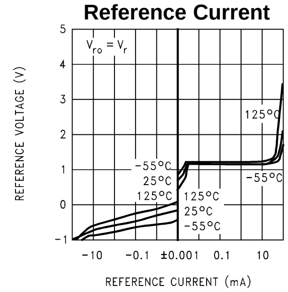
Reference Voltage vs Current and Temperature



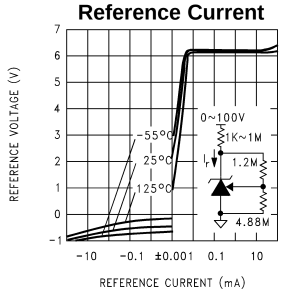
Reference Voltage vs Current and Temperature



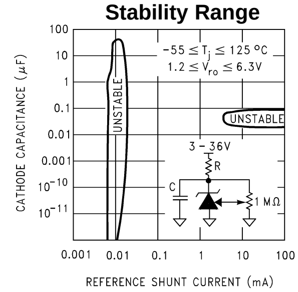
Reference Voltage vs Reference Current



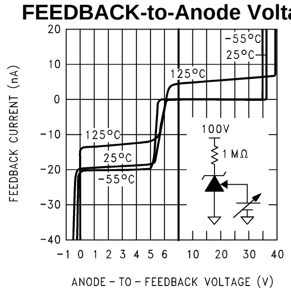
Reference Voltage vs Reference Current



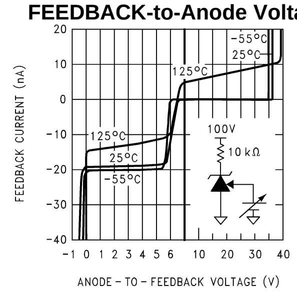
Reference AC Stability Range



FEEDBACK Current vs FEEDBACK-to-Anode Voltage



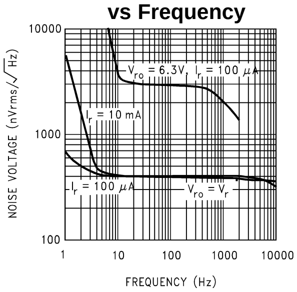
FEEDBACK Current vs FEEDBACK-to-Anode Voltage



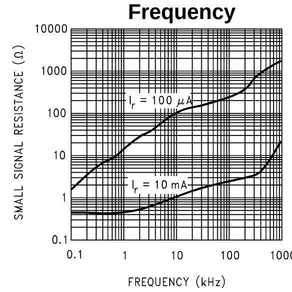
Typical Performance Characteristics (Reference) (continued)

T_J = 25°C, FEEDBACK pin shorted to V^- = 0V, unless otherwise noted

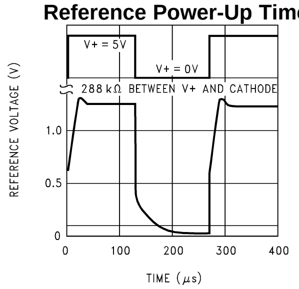
Reference Noise Voltage vs Frequency



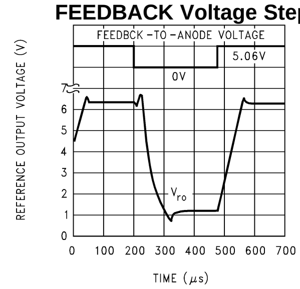
Reference Small-Signal Resistance vs Frequency



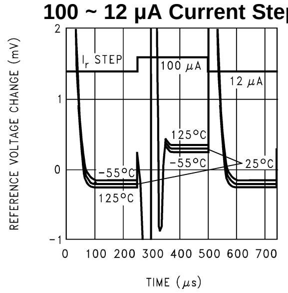
Reference Power-Up Time



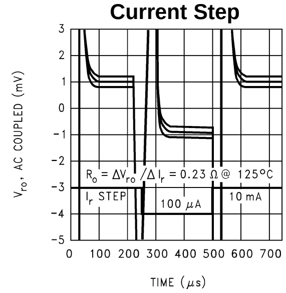
Reference Voltage with FEEDBACK Voltage Step



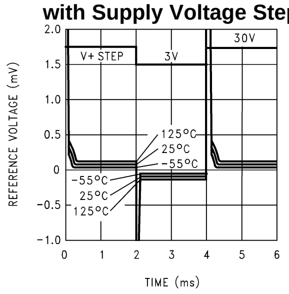
Reference Voltage with 100 ~ 12 µA Current Step



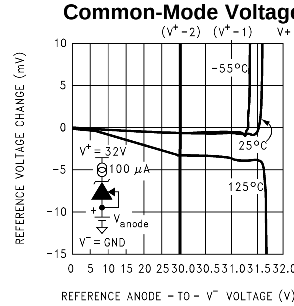
Reference Step Response for 100 µA ~ 10 mA Current Step



Reference Voltage Change with Supply Voltage Step



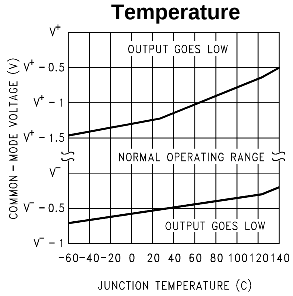
Reference Change vs Common-Mode Voltage



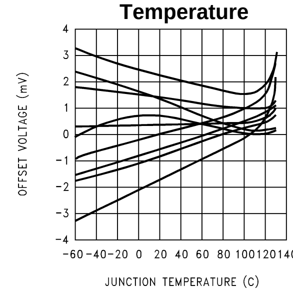
Typical Performance Characteristics (Op Amps)

$V^+ = 5V$, $V^- = GND = 0V$, $V_{CM} = V^+/2$, $V_{OUT} = V^+/2$, $T_J = 25°C$, unless otherwise noted

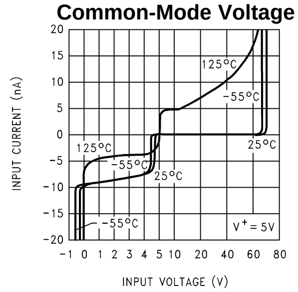
Input Common-Mode Voltage Range vs Temperature



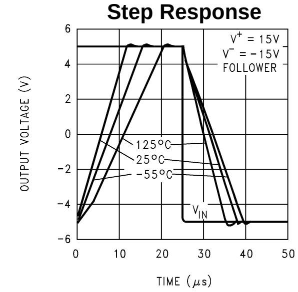
V_{OS} vs Junction Temperature



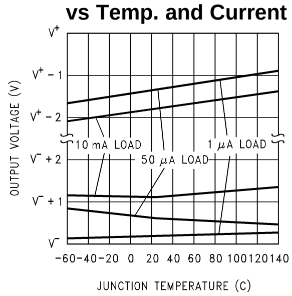
Input Bias Current vs Common-Mode Voltage



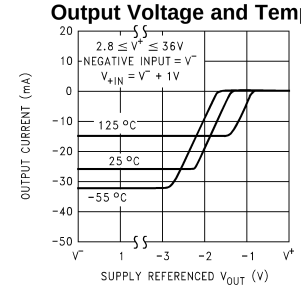
Large-Signal Step Response



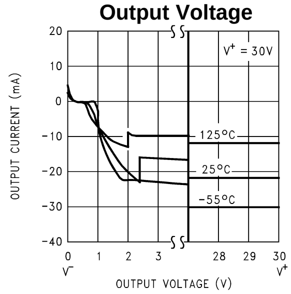
Output Voltage Swing vs Temp. and Current



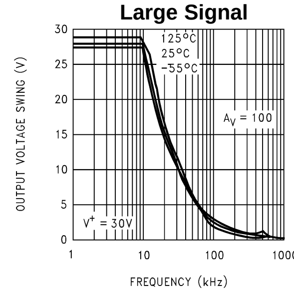
Output Source Current vs Output Voltage and Temp.



Output Sink Current vs Output Voltage



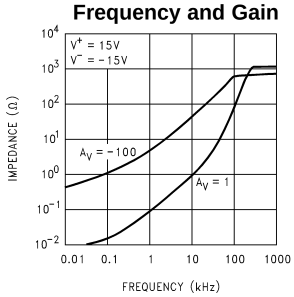
Output Swing, Large Signal



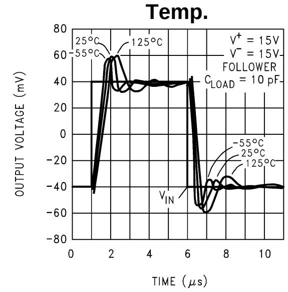
Typical Performance Characteristics (Op Amps) (continued)

$V^+ = 5V$, $V^- = GND = 0V$, $V_{CM} = V^+/2$, $V_{OUT} = V^+/2$, $T_J = 25°C$, unless otherwise noted

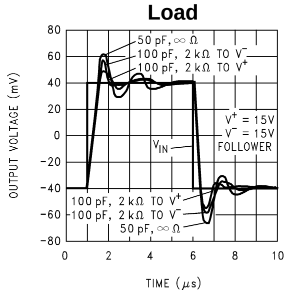
Output Impedance vs Frequency and Gain



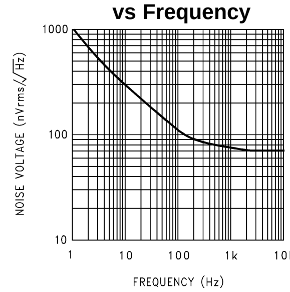
Small Signal Pulse Response vs Temp.



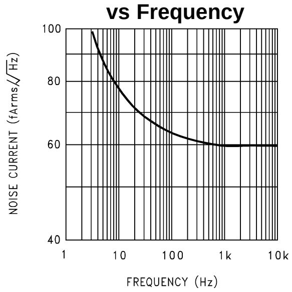
Small-Signal Pulse Response vs Load



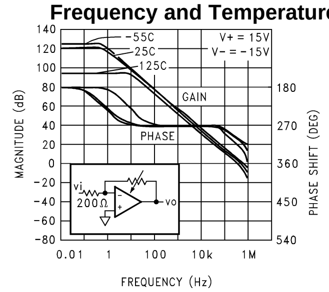
Op Amp Voltage Noise vs Frequency



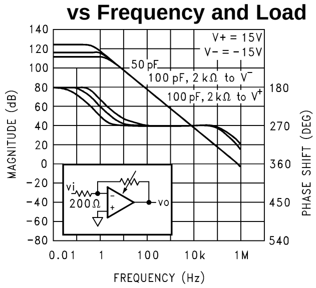
Op Amp Current Noise vs Frequency



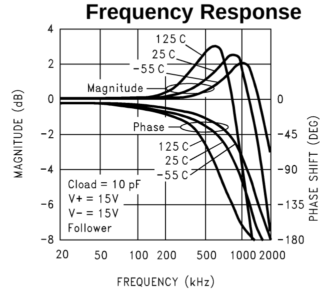
Small-Signal Voltage Gain vs Frequency and Temperature



Small-Signal Voltage Gain vs Frequency and Load



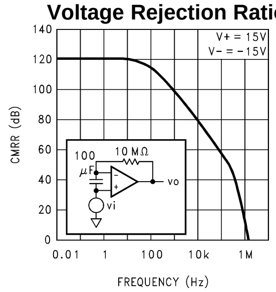
Follower Small-Signal Frequency Response



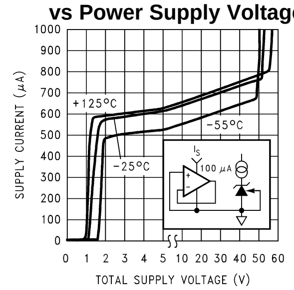
Typical Performance Characteristics (Op Amps) (continued)

V^+ = 5V, V^- = GND = 0V, V_{CM} = V^+/2, V_{OUT} = V^+/2, T_J = 25°C, unless otherwise noted

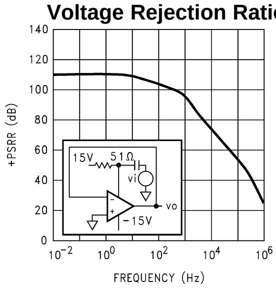
Common-Mode Input Voltage Rejection Ratio



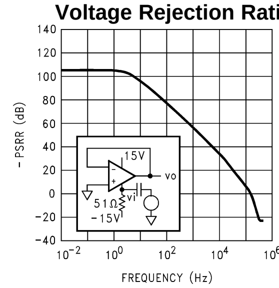
Power Supply Current vs Power Supply Voltage



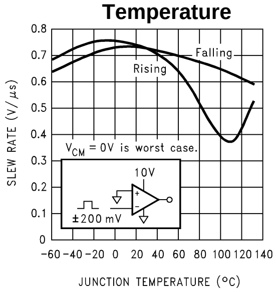
Positive Power Supply Voltage Rejection Ratio



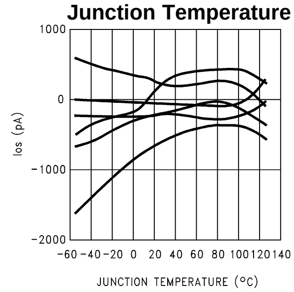
Negative Power Supply Voltage Rejection Ratio



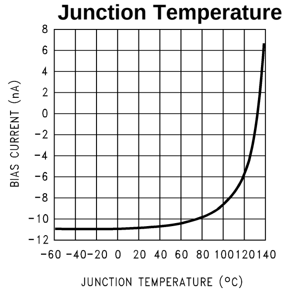
Slew Rate vs Temperature



Input Offset Current vs Junction Temperature

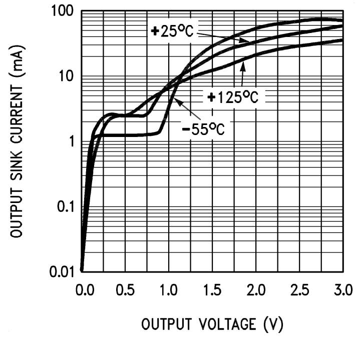


Input Bias Current vs Junction Temperature

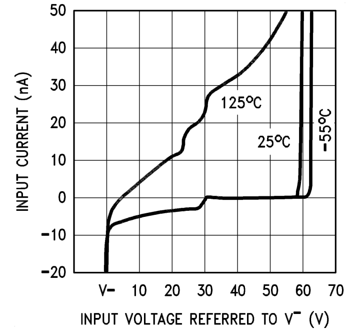


Typical Performance Characteristics (Comparators)

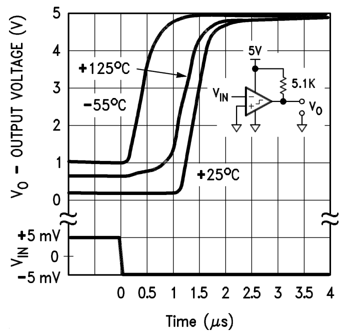
Output Sink Current



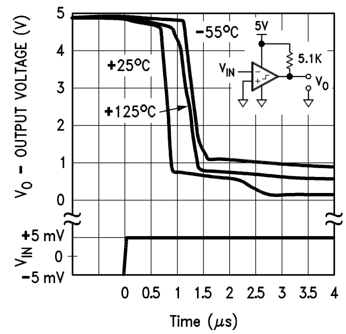
Input Bias Current vs Common-Mode Voltage



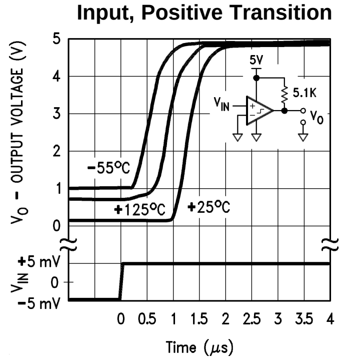
Comparator Response Times—Inverting Input, Positive Transition



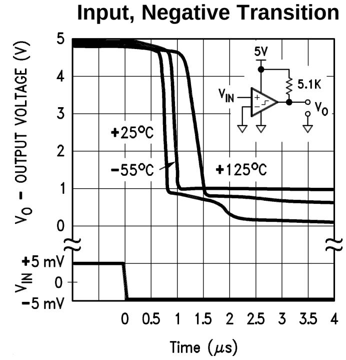
Comparator Response Times—Inverting Input, Negative Transition



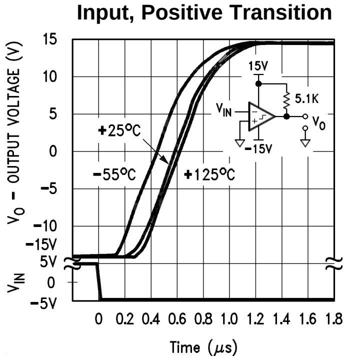
Comparator Response Times—Non-Inverting Input, Positive Transition



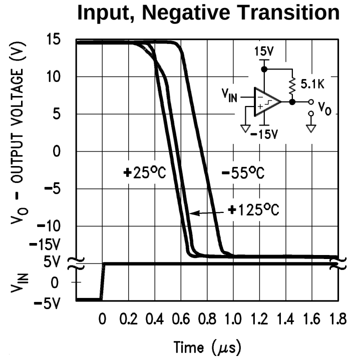
Comparator Response Times—Non-Inverting Input, Negative Transition



Comparator Response Times—Inverting Input, Positive Transition

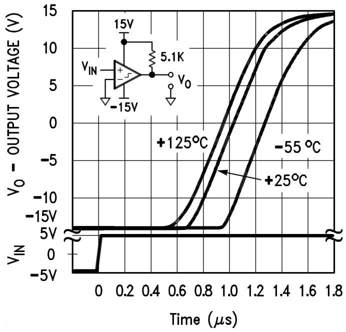


Comparator Response Times—Inverting Input, Negative Transition

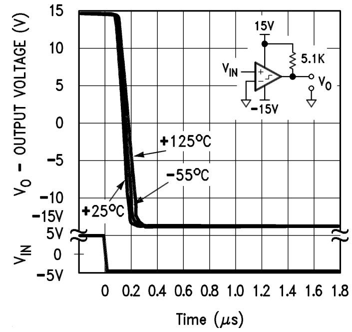


Typical Performance Characteristics (Comparators) (continued)

Comparator Response Times—Non-Inverting Input, Positive Transition



Comparator Response Times—Non-Inverting Input, Negative Transition



Typical Performance Distributions

Figure 7. Average V_{OS} Drift Military Temperature Range

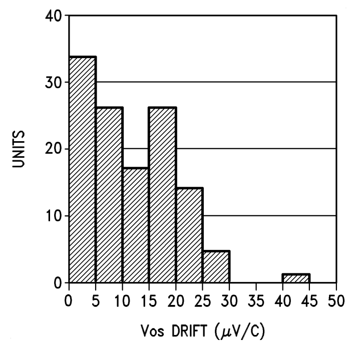


Figure 8. Average V_{OS} Drift Industrial Temperature Range

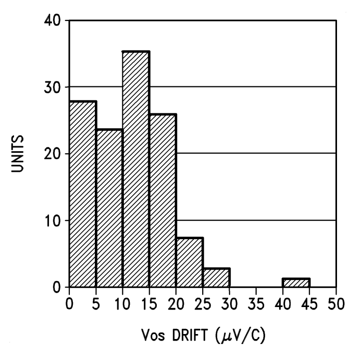


Figure 9. Average V_{OS} Drift Commercial Temperature Range

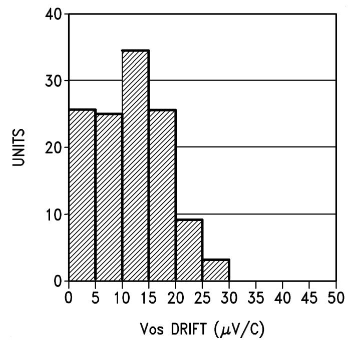


Figure 10. Average I_{OS} Drift Military Temperature Range

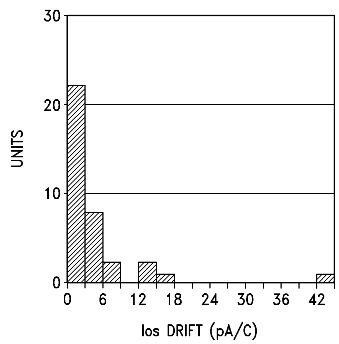


Figure 11. Average I_{OS} Drift Industrial Temperature Range

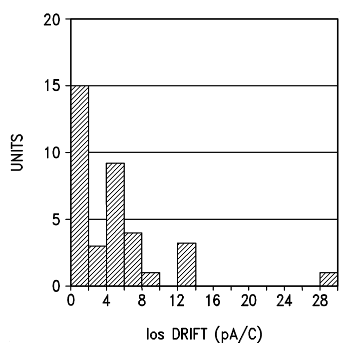


Figure 12. Op Amp Voltage Noise Distribution

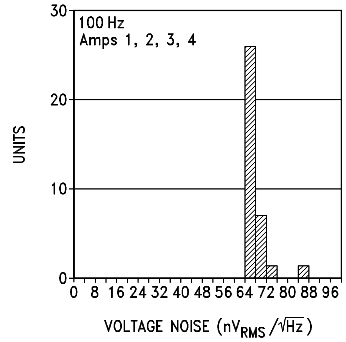


Figure 13. Average I_{OS} Drift Commercial Temperature Range

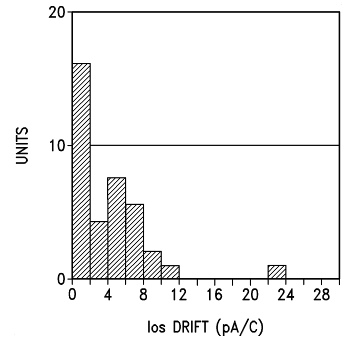


Figure 14. Op Amp Current Noise Distribution

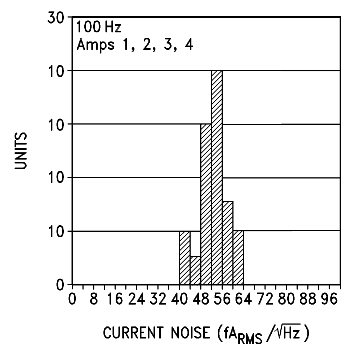
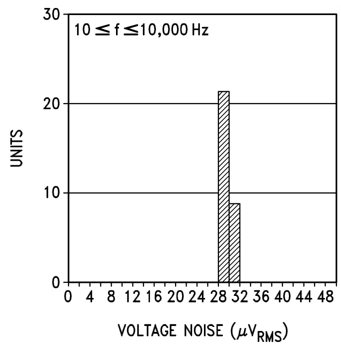


Figure 15. Voltage Reference Broad-Band Noise Distribution



Application Information

VOLTAGE REFERENCE

Reference Biasing

The voltage reference is of a shunt regulator topology that models as a simple zener diode. With current I_r flowing in the “forward” direction there is the familiar diode transfer function. I_r flowing in the reverse direction forces the reference voltage to be developed from cathode to anode. The cathode may swing from a diode drop below V^- to the reference voltage or to the avalanche voltage of the parallel protection diode, nominally 7V. A 6.3V reference with V^+ = 3V is allowed.

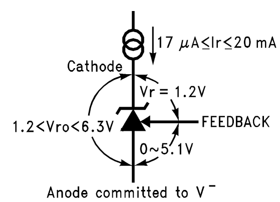


Figure 16. Voltage Associated with Reference (current source I_r is external)

The reference equivalent circuit reveals how V_r is held at the constant 1.2V by feedback, and how the FEEDBACK pin passes little current.

To generate the required reverse current, typically a resistor is connected from a supply voltage higher than the reference voltage. Varying that voltage, and so varying I_r, has small effect with the equivalent series resistance of less than an ohm at the higher currents. Alternatively, an active current source, such as the LM134 series, may generate I_r.

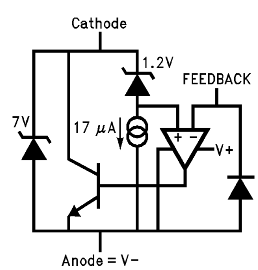


Figure 17. Reference Equivalent Circuit

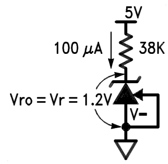


Figure 18. 1.2V Reference

Capacitors in parallel with the reference are allowed. See the Reference AC Stability Range typical curve for capacitance values—from 20 μA to 3 mA any capacitor value is stable. With the reference's wide stability range with resistive and capacitive loads, a wide range of RC filter values will perform noise filtering.

Adjustable Reference

The FEEDBACK pin allows the reference output voltage, V_{ro}, to vary from 1.24V to 6.3V. The reference attempts to hold V_r at 1.24V. If V_r is above 1.24V, the reference will conduct current from Cathode to Anode; FEEDBACK current always remains low. If FEEDBACK is connected to Anode, then $V_{ro} = V_r = 1.24V$. For higher voltages FEEDBACK is held at a constant voltage above Anode—say 3.76V for V_{ro} = 5V. Connecting a resistor across the constant V_r generates a current I=R1/V_r flowing from Cathode into FEEDBACK node. A Thevenin equivalent 3.76V is generated from FEEDBACK to Anode with R2=3.76/I. Keep I greater than one thousand times larger than FEEDBACK bias current for <0.1% error—I≥32 μA for the military grade over the military temperature range (I≥5.5 μA for a 1% untrimmed error for a commercial part).

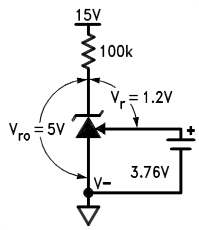
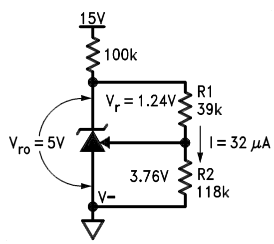


Figure 19. Thevenin Equivalent of Reference with 5V Output



R1 = Vr/I = 1.24/32μ = 39k
R2 = R1 {(Vro/Vr) − 1} = 39k {(5/1.24) − 1)} = 118k

Figure 20. Resistors R1 and R2 Program Reference Output Voltage to be 5V

Understanding that V_r is fixed and that voltage sources, resistors, and capacitors may be tied to the FEEDBACK pin, a range of V_r temperature coefficients may be synthesized.

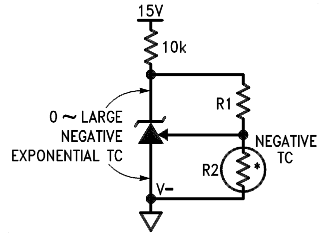


Figure 21. Output Voltage has Negative Temperature Coefficient (TC) if R2 has Negative TC

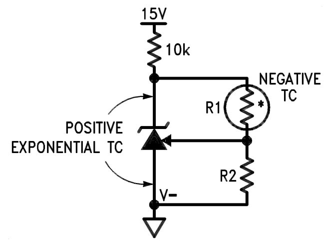


Figure 22. Output Voltage has Positive TC if R1 has Negative TC

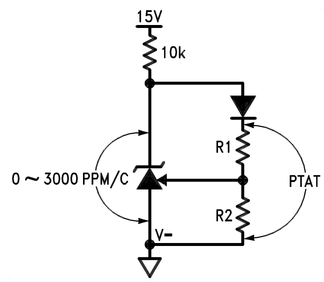
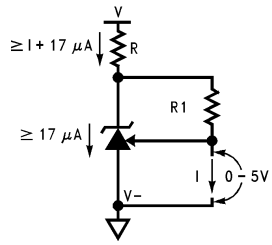


Figure 23. Diode in Series with R1 Causes Voltage Across R1 and R2 to be Proportional to Absolute Temperature (PTAT)

Connecting a resistor across Cathode-to-FEEDBACK creates a 0 TC current source, but a range of TCs may be synthesized.



I = Vr/R1 = 1.24/R1

Figure 24. Current Source is Programmed by R1

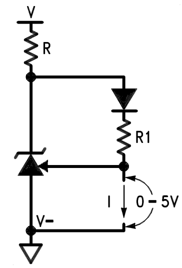


Figure 25. Proportional-to-Absolute-Temperature Current Source

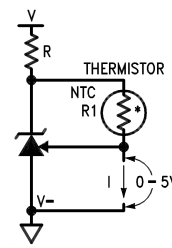


Figure 26. Negative-TC Current Source

Reference Hysteresis

The reference voltage depends, slightly, on the thermal history of the die. Competitive micro-power products vary— always check the data sheet for any given device. Do not assume that no specification means no hysteresis.

OPERATIONAL AMPLIFIERS AND COMPARATORS

Any amp, comparator, or the reference may be biased in any way with no effect on the other sections of the LM613, except when a substrate diode conducts, see Electrical Characteristics [(1)]. For example, one amp input may be outside the common-mode range, another amp may be operating as a comparator, and all other sections may have all terminals floating with no effect on the others. Tying inverting input to output and non-inverting input to V^- on unused amps is preferred. Unused comparators should have non-inverting input and output tied to V^+, and inverting input tied to V^-. Choosing operating points that cause oscillation, such as driving too large a capacitive load, is best avoided.

Op Amp Output Stage

These op amps, like the LM124 series, have flexible and relatively wide-swing output stages. There are simple rules to optimize output swing, reduce cross-over distortion, and optimize capacitive drive capability:

1. Output Swing: Unloaded, the 42 μA pull-down will bring the output within 300 mV of V^- over the military temperature range. If more than 42 μA is required, a resistor from output to V^- will help. Swing across any load may be improved slightly if the load can be tied to V^+, at the cost of poorer sinking open-loop voltage gain.
2. Cross-Over Distortion: The LM613 has lower cross-over distortion (a 1 V_{BE} deadband versus 3 V_{BE} for the LM124), and increased slew rate as shown in the characteristic curves. A resistor pull-up or pull-down will force class-A operation with only the PNP or NPN output transistor conducting, eliminating cross-over distortion.
3. Capacitive Drive: Limited by the output pole caused by the output resistance driving capacitive loads, a pull-down resistor conducting 1 mA or more reduces the output stage NPN r_e until the output resistance is that of the current limit 25Ω. 200 pF may then be driven without oscillation.

(1) Absolute maximum ratings indicate limits beyond which damage to the component may occur. Electrical specifications do not apply when operating the device beyond its rated operating conditions.

Comparator Output Stage

The comparators, like the LM139 series, have open-collector output stages. A pull-up resistor must be added from each output pin to a positive voltage for the output transistor to switch properly. When the output transistor is OFF, the output voltage will be this external positive voltage.

For the output voltage to be under the TTL-low voltage threshold when the output transistor is ON, the output current must be less than 8 mA (over temperature). This impacts the minimum value of pull-up resistor.

The offset voltage may increase when the output voltage is low and the output current is less than 30 μA. Thus, for best accuracy, the pull-up resistor value should be low enough to allow the output transistor to sink more than 30 μA.

Op Amp and Comparator Input Stage

The lateral PNP input transistors, unlike those of most op amps, have BV_{EBO} equal to the absolute maximum supply voltage. Also, they have no diode clamps to the positive supply nor across the inputs. These features make the inputs look like high impedances to input sources producing large differential and common-mode voltages.

Typical Applications

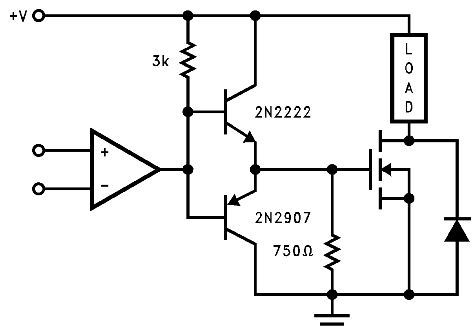


Figure 27. High Current, High Voltage Switch

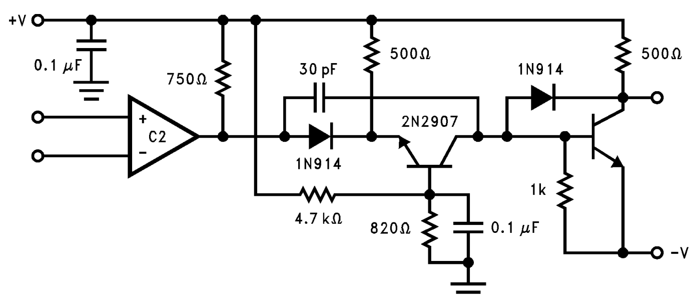
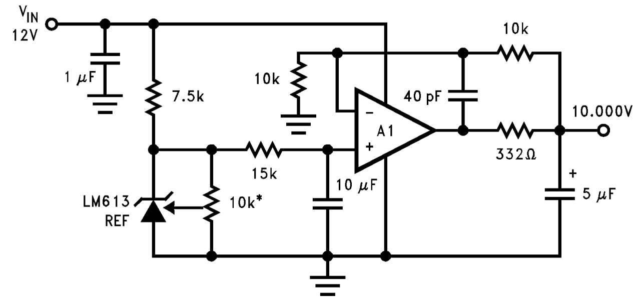


Figure 28. High Speed Level Shifter. Response time is approximately 1.5 μs, where output is either approximately +V or −V.



*10k must be low
t.c. trimpot

Figure 29. Ultra Low Noise, 10.00V Reference. Total output noise is typically 14 μV_{RMS}.

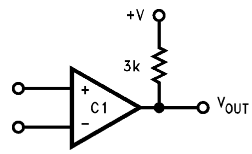


Figure 30. Basic Comparator

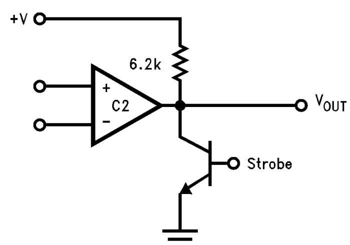


Figure 31. Basic Comparator with External Strobe

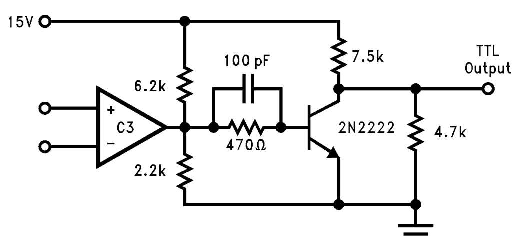


Figure 32. Wide-Input Range Comparator with TTL Output

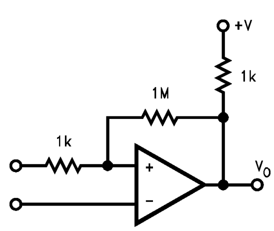


Figure 33. Comparator with Hysteresis ($\Delta V_H = {}^{+}V(1k/1M)$)

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
LM613IWM	ACTIVE	SOIC	DW	16	45	TBD	CU SNPB	Level-2A-220C-4 WEEK	-40 to 85	LM613IWM	Samples
LM613IWM/NOPB	ACTIVE	SOIC	DW	16	45	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	-40 to 85	LM613IWM	Samples
LM613IWMX	ACTIVE	SOIC	DW	16	1000	TBD	CU SNPB	Level-2A-220C-4 WEEK	-40 to 85	LM613IWM	Samples
LM613IWMX/NOPB	ACTIVE	SOIC	DW	16	1000	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	-40 to 85	LM613IWM	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Only one of markings shown within the brackets will appear on the physical device.

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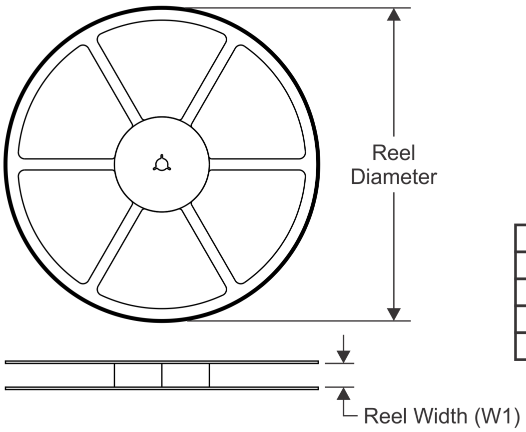
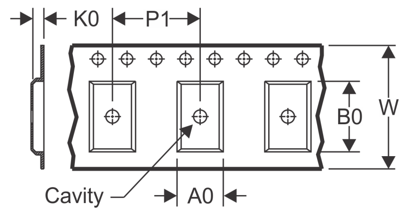
TAPE AND REEL INFORMATION

REEL DIMENSIONS

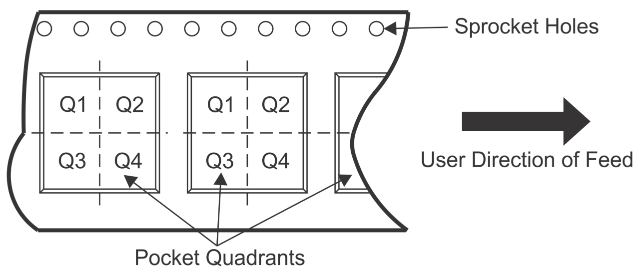


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

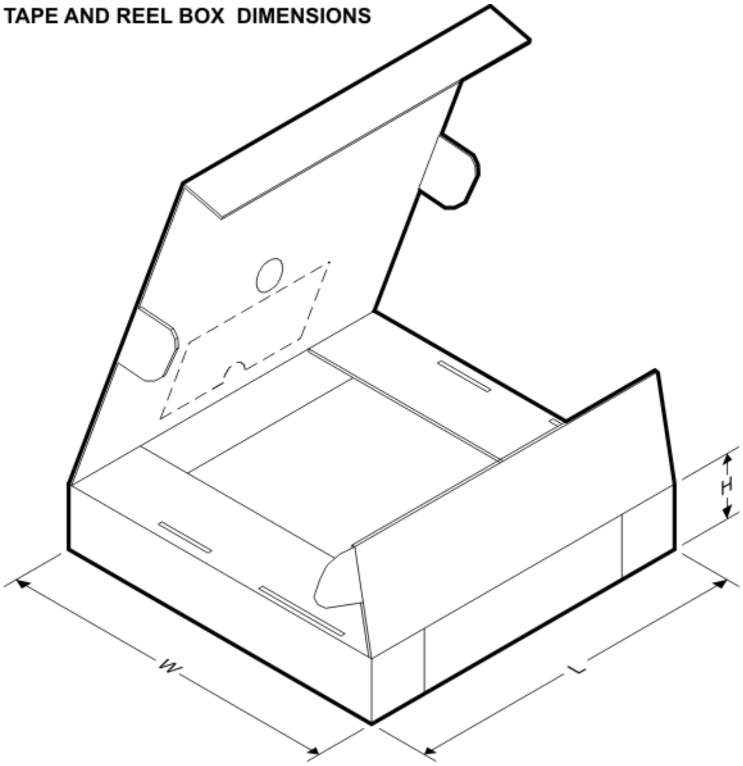
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM613IWMX	SOIC	DW	16	1000	330.0	16.4	10.9	10.7	3.2	12.0	16.0	Q1
LM613IWMX/NOPB	SOIC	DW	16	1000	330.0	16.4	10.9	10.7	3.2	12.0	16.0	Q1

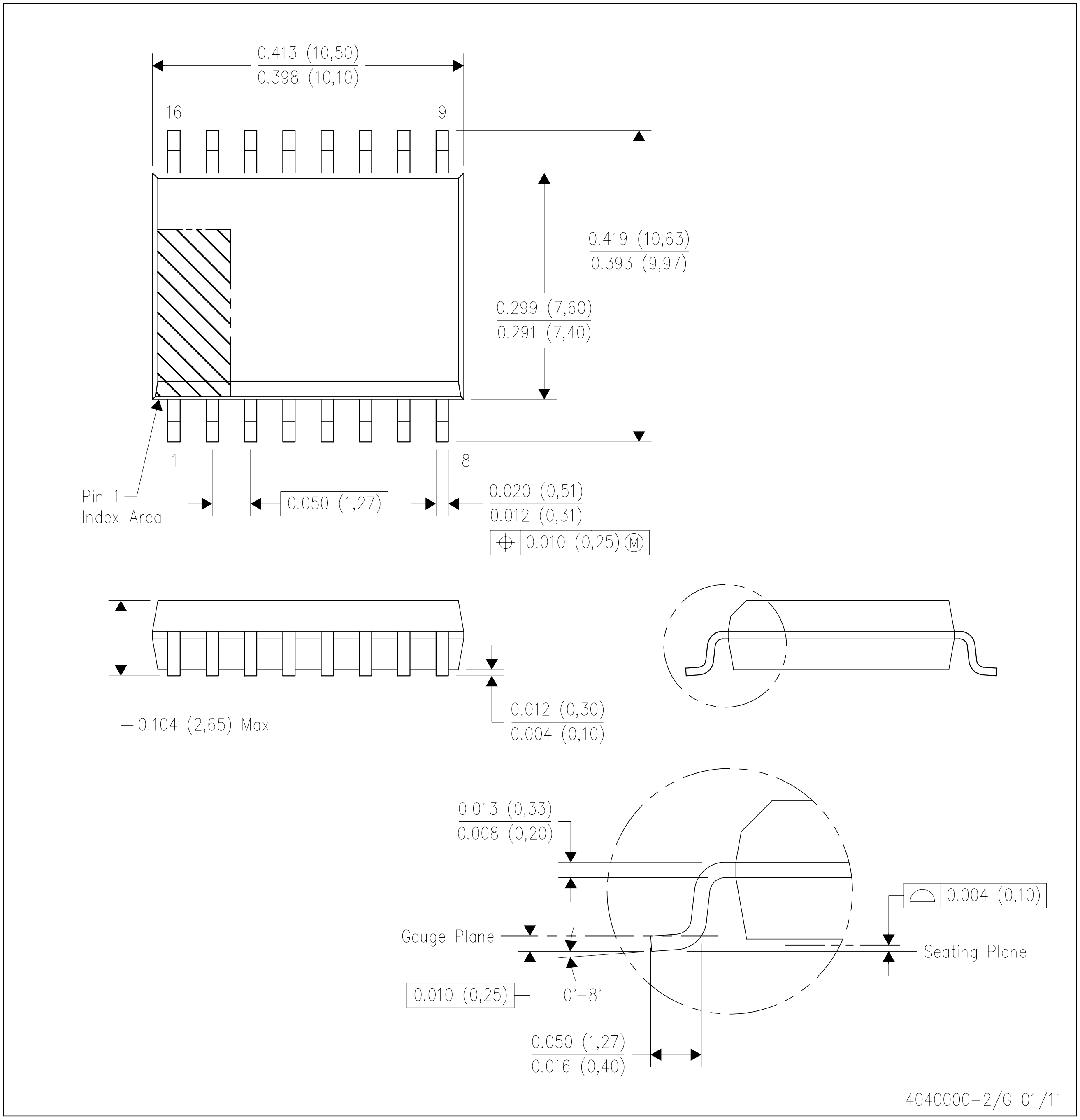
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM613IWMX	SOIC	DW	16	1000	358.0	343.0	63.0
LM613IWMX/NOPB	SOIC	DW	16	1000	358.0	343.0	63.0

DW (R-PDSO-G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS-013 variation AA.

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