

# LM6161/LM6261/LM6361

## High Speed Operational Amplifier

### General Description

The LM6161 family of high-speed amplifiers exhibits an excellent speed-power product in delivering 300 V/ $\mu$ s and 50 MHz unity gain stability with only 5 mA of supply current. Further power savings and application convenience are possible by taking advantage of the wide dynamic range in operating supply voltage which extends all the way down to +5V.

These amplifiers are built with National's VIPTM (Vertically Integrated PNP) process which provides fast PNP transistors that are true complements to the already fast NPN devices. This advanced junction-isolated process delivers high speed performance without the need for complex and expensive dielectric isolation.

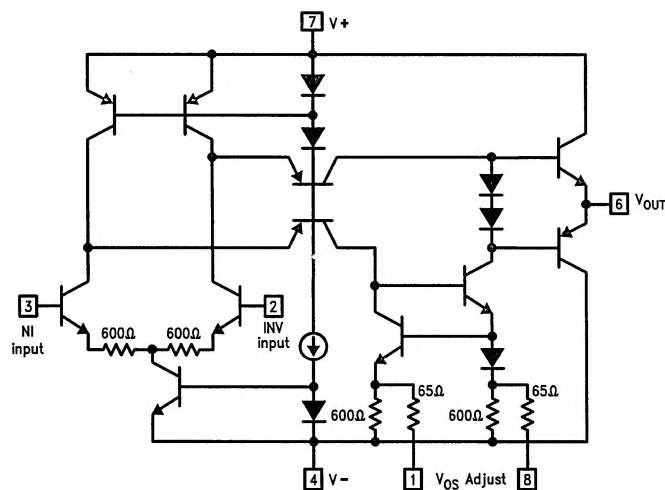
### Features

- High slew rate 300 V/ $\mu$ s
- High unity gain freq 50 MHz
- Low supply current 5 mA
- Fast settling 120 ns to 0.1%
- Low differential gain <0.1%
- Low differential phase 0.1°
- Wide supply range 4.75V to 32V
- Stable with unlimited capacitive load
- Well behaved; easy to apply

### Applications

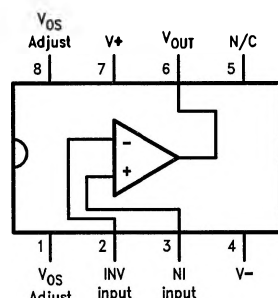
- Video amplifier
- High-frequency filter
- Wide-bandwidth signal conditioning

### Simplified Schematic



TL/H/9057-3

### Connection Diagram



TL/H/9057-5

**Order Number LM6161J or LM6261J**  
See NS Package Number J08A

**Order Number LM6261N or LM6361N**  
See NS Package Number N08E

**Order Number LM6361M**  
See NS Package Number M08A

## Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage ( $V^+ - V^-$ )	36V
Differential Input Voltage (Note 8)	$\pm 8V$
Common-Mode Voltage Range (Note 12)	$(V^+ - 0.7V)$ to $(V^- - 7V)$
Output Short Circuit to GND (Note 1)	Continuous
Soldering Information	
Dual-In-Line Package (N, J)	
Soldering (10 sec.)	260°C
Small Outline Package (M)	
Vapor Phase (60 sec.)	215°C
Infrared (15 sec.)	220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

Storage Temp Range	$-65^\circ\text{C}$ to $+150^\circ\text{C}$
Max Junction Temperature	150°C
ESD Tolerance (Notes 8 and 9)	$\pm 700V$

## Operating Ratings

Temperature Range (Note 2)	
LM6161	$-55^\circ\text{C} \leq T_J \leq +125^\circ\text{C}$
LM6261	$-25^\circ\text{C} \leq T_J \leq +85^\circ\text{C}$
LM6361	$0^\circ\text{C} \leq T_J \leq +70^\circ\text{C}$
Supply Voltage Range	4.75V to 32V

## DC Electrical Characteristics (Note 3)

Parameter	Conditions	Typ	LM6161		LM6261		LM6361		Units
			Tested Limit (Note 4)	Design Limit (Note 5)	Tested Limit (Note 4)	Design Limit (Note 5)	Tested Limit (Note 4)	Design Limit (Note 5)	
Input Offset Voltage		5	7 10		7	9	20	22	mV max
Input Offset Voltage Average Drift		10							$\mu\text{V}/^\circ\text{C}$
Input Bias Current		2	3 6		3	5	5	6	$\mu\text{A}$ max
Input Offset Current		150	350 800		350	600	1500	1900	nA max
Input Offset Current Average Drift		0.4							nA/ $^\circ\text{C}$
Input Resistance	Differential	325							k $\Omega$
Input Capacitance	$A_v = +1$ @ 10 MHz	1.5							pF
Large Signal Voltage Gain	$V_{OUT} = \pm 10V$ , $R_L = 2\text{ k}\Omega$ (Note 11)	750	550 300		550	400	400	350	V/V min
	$R_L = 10\text{ k}\Omega$	2900							V/V
Input Common-Mode Voltage Range	Supply = $\pm 15V$	+14.0	+13.9 +13.8		+13.9	+13.8	+13.8	+13.7	Volts min
		-13.2	-12.9 -12.7		-12.9	-12.7	-12.8	-12.7	Volts min
	Supply = +5V (Note 6)	4.0	3.9 3.8		3.9	3.8	3.8	3.7	Volts min
		1.8	2.0 2.2		2.0	2.2	2.1	2.2	Volts max
Common-Mode Rejection Ratio	$-10V \leq V_{CM} \leq +10V$	94	80 74		80	76	72	70	dB min
Power Supply Rejection Ratio	$\pm 10V \leq V \leq \pm 16V$	90	80 74		80	76	72	70	dB min

**DC Electrical Characteristics** (Note 3) (Continued)

Parameter	Conditions	Typ	LM6161		LM6261		LM6361		Units
			Tested Limit (Note 4)	Design Limit (Note 5)	Tested Limit (Note 4)	Design Limit (Note 5)	Tested Limit (Note 4)	Design Limit (Note 5)	
Output Voltage Swing	Supply = $\pm 15\text{V}$ and $R_L = 2\text{ k}\Omega$	+14.2	+13.5 <b>+13.3</b>		+13.5	<b>+13.3</b>	+13.4	<b>+13.3</b>	Volts min
		-13.4	-13.0 <b>-12.7</b>		-13.0	<b>-12.8</b>	-12.9	<b>-12.8</b>	Volts min
	Supply = $\pm 5\text{V}$ and $R_L = 2\text{ k}\Omega$ (Note 6)	4.2	3.5 <b>3.3</b>		3.5	<b>3.3</b>	3.4	<b>3.3</b>	Volts min
		1.3	1.7 <b>2.0</b>		1.7	<b>1.9</b>	1.8	<b>1.9</b>	Volts max
Output Short Circuit Current	Source	65	30 <b>20</b>		30	<b>25</b>	30	<b>25</b>	mA min
	Sink	65	30 <b>20</b>		30	<b>25</b>	30	<b>25</b>	mA min
Supply Current		5.0	6.5 <b>6.8</b>		6.5	<b>6.7</b>	6.8	<b>6.9</b>	mA max

**AC Electrical Characteristics** (Notes 3 & 7)

Parameter	Conditions	Typ	LM6161		LM6261		LM6361		Units
			Tested Limit (Note 4)	Design Limit (Note 5)	Tested Limit (Note 4)	Design Limit (Note 5)	Tested Limit (Note 4)	Design Limit (Note 5)	
Gain-Bandwidth Product	@ $F = 20\text{ MHz}$	50	40 <b>30</b>		40	<b>35</b>	35	<b>32</b>	MHz min
	Supply = $\pm 5\text{V}$	35							MHz
Slew Rate	$A_v = +1$ (Note 10)	300	200 <b>180</b>		200	<b>180</b>	200	<b>180</b>	V/ $\mu\text{s}$ min
	Supply = $\pm 5\text{V}$	200							V/ $\mu\text{s}$
Power Bandwidth	$V_{OUT} = 20\text{ V}_{pp}$	4.5							MHz
Settling Time	10V Step to 0.1% $A_v = -1, R_L = 2\text{ k}\Omega$	120							ns
Phase Margin		45							Deg
Differential Gain	NTSC, $A_v = +4$	<0.1							%
Differential Phase	NTSC, $A_v = +4$	0.1							Deg
Input Noise Voltage	$f = 10\text{ kHz}$	15							nV/ $\sqrt{\text{Hz}}$
Input Noise Current	$f = 10\text{ kHz}$	1.5							pA/ $\sqrt{\text{Hz}}$

**Note 1:** Continuous short-circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of  $150^\circ\text{C}$ .

**Note 2:** The typical junction-to-ambient thermal resistance of the molded plastic DIP (N) is  $105^\circ\text{C/W}$ , the molded plastic SO (M) package is  $155^\circ\text{C/W}$ , and the cerdip (J) package is  $125^\circ\text{C/W}$ . All numbers apply for packages soldered directly into a printed circuit board.

**Note 3:** Unless otherwise specified, all limits guaranteed for  $T_A = T_J = 25^\circ\text{C}$  with supply voltage =  $\pm 15\text{V}$ ,  $V_{CM} = 0\text{V}$ , and  $R_L \geq 100\text{ k}\Omega$ . **Boldface** limits apply over the range listed under "Operating Temperature Range" with  $T_A = T_J$  in the "Absolute Maximum Ratings" section.

**Note 4:** All limits guaranteed at room temperature (standard type face) and at **temperature extremes (bold type face)**. All limits are 100% production tested.

**Note 5:** All limits guaranteed at **temperature extremes (bold type face)** via correlation using standard Statistical Quality Control (SQC) methods.

**Note 6:** For single supply operation, the following conditions apply:  $V^+ = 5\text{V}$ ,  $V^- = 0\text{V}$ ,  $V_{CM} = 2.5\text{V}$ ,  $V_{OUT} = 2.5\text{V}$ . Pin 1 & Pin 8 (Vos Adjust) are each connected to Pin 4 ( $V^-$ ) to realize maximum output swing. This connection will degrade  $V_{OS}$ ,  $V_{OS}$  Drift, and Input Voltage Noise.

**Note 7:**  $C_L \leq 5\text{ pF}$ .

**Note 8:** In order to achieve optimum AC performance, the input stage was designed without protective clamps. Exceeding the maximum differential input voltage results in reverse breakdown of the base-emitter junction of one of the input transistors and probable degradation of the input parameters (especially Vos, Ios, and Noise).

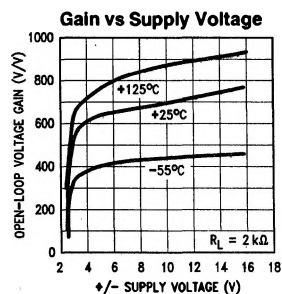
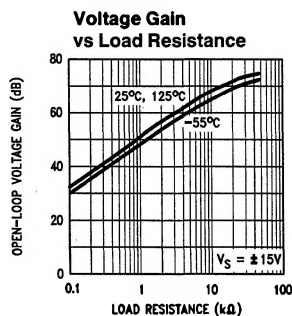
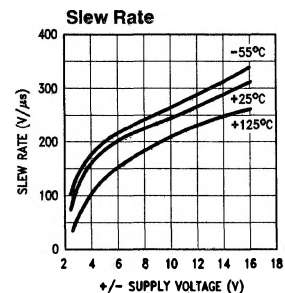
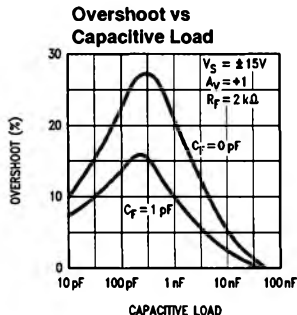
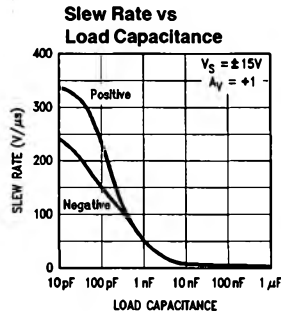
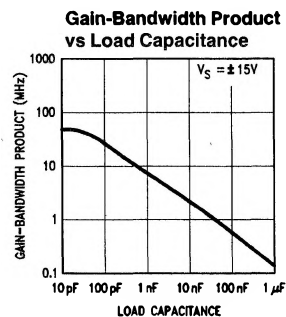
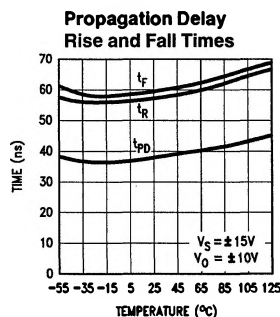
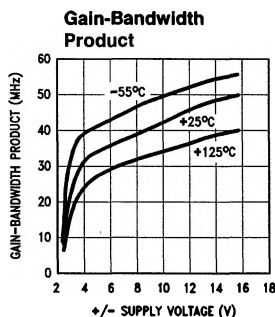
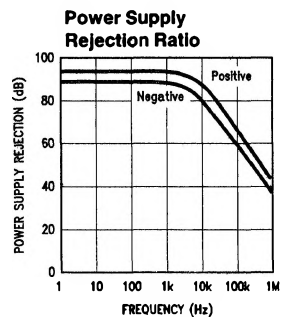
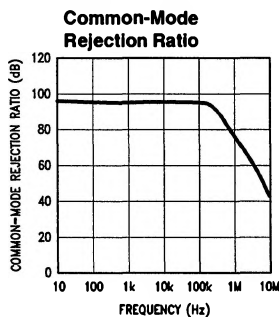
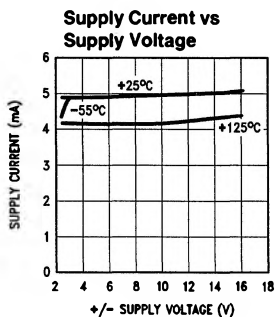
**Note 9:** The average voltage that the weakest pin combinations (those involving Pin 2 or Pin 3) can withstand and still conform to the datasheet limits. The test circuit used consists of the human body model of  $100\text{ pF}$  in series with  $1500\Omega$ .

**Note 10:**  $V_{IN} = 8\text{V}$  step. For supply =  $\pm 5\text{V}$ ,  $V_{IN} = 5\text{V}$  step.

**Note 11:** Voltage Gain is the total output swing (20V) divided by the input signal required to produce that swing.

**Note 12:** The voltage between  $V^+$  and either input pin must not exceed  $36\text{V}$ .

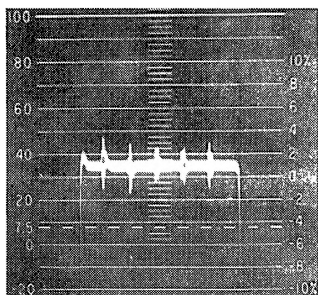
# Typical Performance Characteristics ( $R_L = 10\text{ k}\Omega$ , $T_A = 25^\circ\text{C}$ unless otherwise specified)



## Typical Performance Characteristics

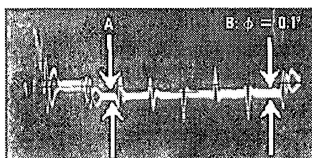
( $R_L = 10\text{ k}\Omega$ ,  $T_A = 25^\circ\text{C}$  unless otherwise specified) (Continued)

Differential Gain (Note)



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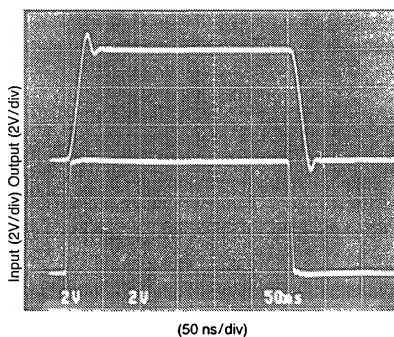
Differential Phase (Note)



TL/H/9057-8

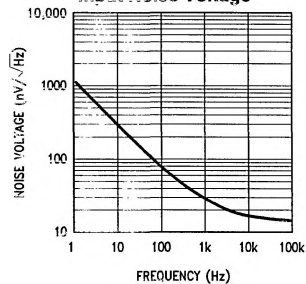
Note: Differential gain and differential phase measured for four series LM6361 op amps configured as unity-gain followers, in series with an LM6321 buffer. Error added by LM6321 is negligible. Test performed using Tektronix Type 520 NTSC test system.

Step Response;  $A_v = +1$

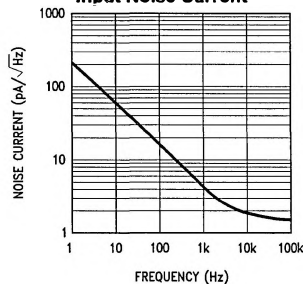


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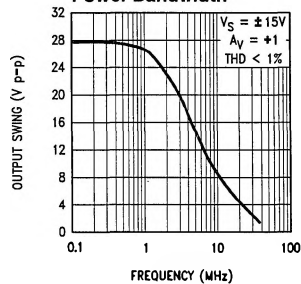
Input Noise Voltage



Input Noise Current



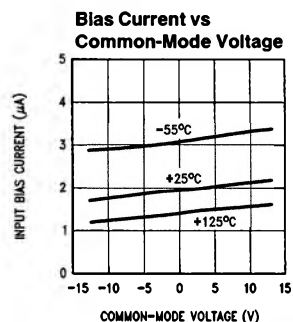
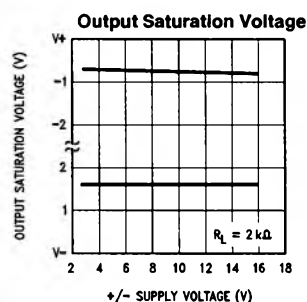
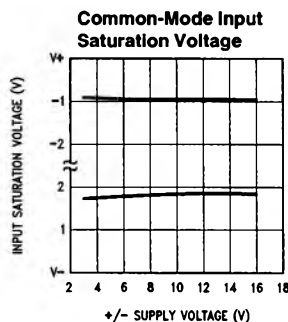
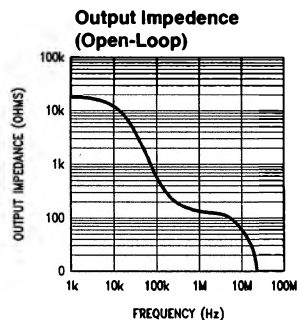
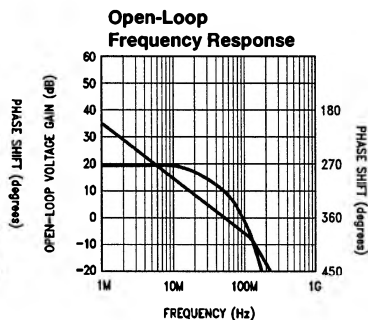
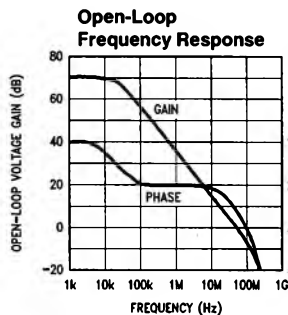
Power Bandwidth



TL/H/9057-9

## Typical Performance Characteristics

( $R_L = 10\text{ k}\Omega$ ,  $T_A = 25^\circ\text{C}$  unless otherwise specified) (Continued)



TL/H/9057-12

## Applications Tips

The LM6361 has been compensated for unity-gain operation. Since this compensation involved adding emitter-degeneration resistors to the op amp's input stage, the open-loop gain was reduced as the stability increased. Gain error due to reduced  $A_{VOL}$  is most apparent at high gains; thus, for gains between 5 and 25, the less-compensated LM6364 should be used, and the uncompensated LM6365 is appropriate for gains of 25 or more. The LM6361, LM6364, and LM6365 have the same high slew rate, regardless of their compensation.

The LM6361 is unusually tolerant of capacitive loads. Most op amps tend to oscillate when their load capacitance is greater than about 200 pF (especially in low-gain circuits). The LM6361's compensation is effectively increased with load capacitance, reducing its bandwidth and increasing its stability.

Power supply bypassing is not as critical for the LM6361 as it is for other op amps in its speed class. Bypassing will,

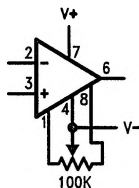
however, improve the stability and transient response and is recommended for every design. 0.01  $\mu\text{F}$  to 0.1  $\mu\text{F}$  ceramic capacitors should be used (from each supply "rail" to ground); if the device is far away from its power supply source, an additional 2.2  $\mu\text{F}$  to 10  $\mu\text{F}$  of tantalum may provide extra noise reduction.

Keep all leads short to reduce stray capacitance and lead inductance, and make sure ground paths are low-impedance, especially where heavier currents will be flowing. Stray capacitance in the circuit layout can cause signal coupling across adjacent nodes and can cause gain to unintentionally vary with frequency.

Breadboarded circuits will work best if they are built using generic PC boards with a good ground plane. If the op amps are used with sockets, as opposed to being soldered into the circuit, the additional input capacitance may degrade circuit performance.

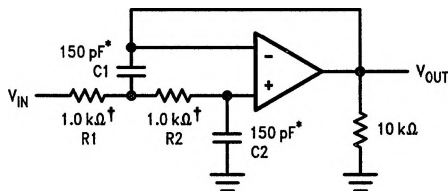
## Typical Applications

### Offset Voltage Adjustment



TL/H/9057-4

### 1 MHz Low-Pass Filter



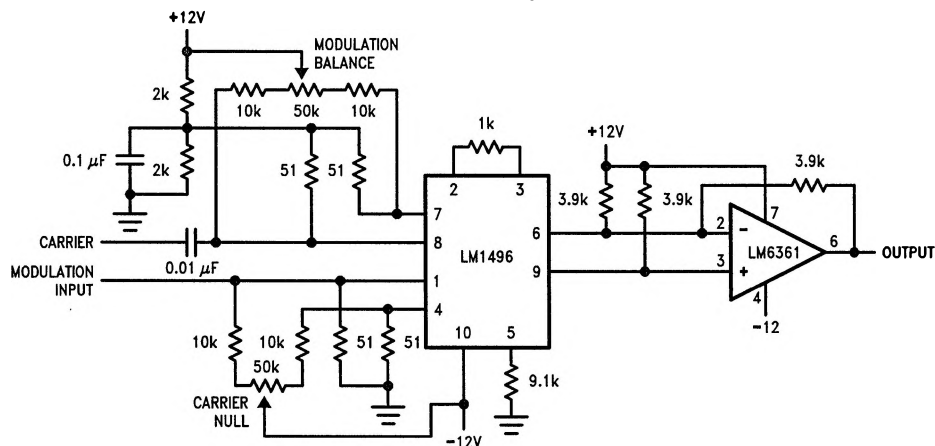
TL/H/9057-10

†1% tolerance

\*Matching determines filter precision

$$f_c = 2\pi \sqrt{(R1 R2 C1 C2)^{-1}}$$

### Modulator with Differential-to-Single-Ended Converter



TL/H/9057-11