National Semiconductor

LM6164/LM6264/LM6364 High Speed Operational Amplifier

General Description

The LM6164 family of high-speed amplifiers exhibits an excellent speed-power product in delivering 300V per μs and 175 MHz GBW (stable down to gains as low as +5) with only 5 mA of supply current. Further power savings and application convenience are possible by taking advantage of the wide dynamic range in operating supply voltage which extends all the way down to +5V.

These amplifiers are built with National's VIP™ (Vertically Integrated PNP) process which produces fast PNP transistors that are true complements to the already fast NPN devices. This advanced junction-isolated process delivers high speed performance without the need for complex and expensive dielectric isolation.

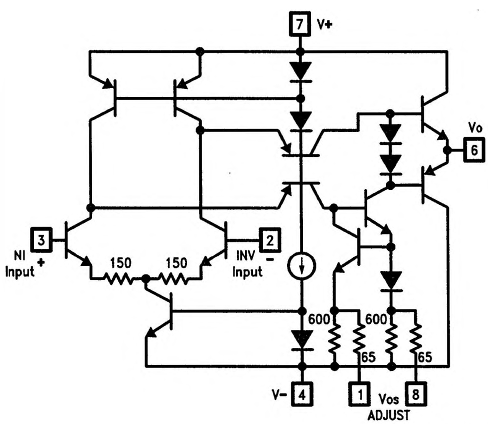
Features

- High slew rate — 300 V/μs
- High GBW product — 175 MHz
- Low supply current — 5 mA
- Fast settling — 100 ns to 0.1%
- Low differential gain — <0.1%
- Low differential phase — <0.1°
- Wide supply range — 4.75V to 32V
- Stable with unlimited capacitive load
- Well behaved; easy to apply

Applications

- Video amplifier
- Wide-bandwidth signal conditioning

Simplified Schematic



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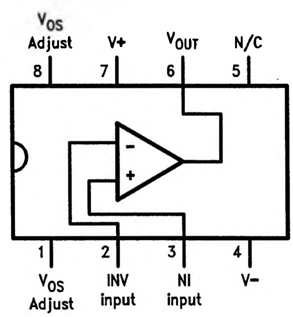
Connection Diagram



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Order Number LM6164J or LM6264J
See NS Package Number J08A

Order Number LM6364M
See NS Package Number M08A

Order Number LM6264N or LM6364N
See NS Package Number N08E

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage ($V^+ - V^-$)	36V
Differential Input Voltage (Note 8)	±8V
Common-Mode Input Voltage (Note 12)	(V^+ − 0.7V) to (V^- − 7V)
Output Short Circuit to Gnd (Note 1)	Continuous
Soldering Information	
Dual-In-Line Package (N, J)	
Soldering (10 sec.)	260°C
Small Outline Package (M)	
Vapor Phase (60 sec.)	215°C
Infrared (15 sec.)	220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

Storage Temperature Range	−65°C to +150°C
Max Junction Temperature (Note 2)	150°C
ESD Tolerance (Notes 8 & 9)	±700V

Operating Ratings

Temperature Range (Note 2)	
LM6161	$-55°C \le T_J \le +125°C$
LM6261	$-25°C \le T_J \le +85°C$
LM6361	$0°C \le T_J \le +70°C$
Supply Voltage Range	4.75V to 32V

DC Electrical Characteristics (Note 3)

Parameter	Conditions	Typ	LM6164		LM6264		LM6364		Units
			Tested Limit (Note 4)	Design Limit (Note 5)	Tested Limit (Note 4)	Design Limit (Note 5)	Tested Limit (Note 4)	Design Limit (Note 5)	
Input Offset Voltage		2	4 **6**		4	**6**	9	**11**	mV max
Input Offset Voltage Average Drift		6							μV/°C
Input Bias Current		2.5	3 **6**		3	**5**	5	**6**	μA max
Input Offset Current		150	350 **800**		350	**600**	1500	**1900**	nA max
Input Offset Current Average Drift		0.3							nA/°C
Input Resistance	Differential	100							kΩ
Input Capacitance		3.0							pF
Large Signal Voltage Gain	$V_{OUT} = \pm 10V$, $R_L = 2\ k\Omega$ (Note 11)	2.5	1.8 **0.9**		1.8	**1.2**	1.3	**1.1**	V/mV min
	$R_L = 10\ k\Omega$	9							
Input Common-Mode Voltage Range	Supply = ±15V	+14.0	+13.9 **+13.8**		+13.9	**+13.8**	+13.8	**+13.7**	V min
		−13.5	−13.3 **−13.1**		−13.3	**−13.1**	−13.2	**−13.1**	V min
	Supply = +5V (Note 6)	4.0	3.9 **3.8**		3.9	**3.8**	3.8	**3.7**	V min
		1.5	1.7 **1.9**		1.7	**1.9**	1.8	**1.9**	V max
Common-Mode Rejection Ratio	$-10V \le V_{CM} \le +10V$	105	86 **80**		86	**82**	80	**78**	dB min
Power Supply Rejection Ratio	$\pm 10V \le V\pm \le \pm 16V$	96	86 **80**		86	**82**	80	**78**	dB min
Output Voltage Swing	Supply = ±15V and $R_L = 2\ k\Omega$	+14.2	+13.5 **+13.3**		+13.5	**+13.3**	+13.4	**+13.3**	V min
		−13.4	−13.0 **−12.7**		−13.0	**−12.8**	−12.9	**−12.8**	V min

DC Electrical Characteristics (Note 3) (Continued)

Parameter	Conditions	Typ	LM6164		LM6264		LM6364		Units
			Tested Limit (Note 4)	Design Limit (Note 5)	Tested Limit (Note 4)	Design Limit (Note 5)	Tested Limit (Note 4)	Design Limit (Note 5)	
Output Voltage Swing	Supply = +5V and R_L = 2 kΩ (Note 6)	4.2	3.5 **3.3**		3.5	**3.3**	3.4	**3.3**	V min
		1.3	1.7 **2.0**		1.7	**1.9**	1.8	**1.9**	V max
Output Short Circuit Current	Source	65	30 **20**		30	**25**	30	**25**	mA min
	Sink	65	30 **20**		30	**25**	30	**25**	mA min
Supply Current		5.0	6.5 **6.8**		6.5	**6.7**	6.8	**6.9**	mA max

AC Electrical Characteristics (Notes 3 & 7)

Parameter	Conditions	Typ	LM6164		LM6264		LM6364		Units
			Tested Limit (Note 4)	Design Limit (Note 5)	Tested Limit (Note 4)	Design Limit (Note 5)	Tested Limit (Note 4)	Design Limit (Note 5)	
Gain-Bandwidth Product	@ F = 20 MHz	175	140 **100**		140	**120**	120	**100**	MHz min
	Supply = ±5V	120							
Slew Rate	A_V = +20 (Note 10)	300	200 **180**		200	**180**	200	**180**	V/µs min
	Supply = ±5V	200							
Power Bandwidth	V_{OUT} = 20 V_{PP}	4.5							MHz
Setting Time	10V Step to 0.1% A_V = −4, R_L = 2 kΩ	100							ns
Phase Margin	A_V = +5	45							Deg
Differential Gain	NTSC, A_V = +10	<0.1							%
Differential Phase	NTSC, A_V = +10	<0.1							Deg
Input Noise Voltage	F = 10 kHz	8							nV/$\sqrt{Hz}$
Input Noise Current	F = 10 kHz	1.5							pA/$\sqrt{Hz}$

Note 1: Continuous short-circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C.

Note 2: The typical junction-to-ambient thermal resistance of the molded plastic DIP (N) is 105°C/Watt, the molded plastic SO (M) package is 155°C/Watt, and the cerdip (J) package is 125°C/Watt. All numbers apply for packages soldered directly into a printed circuit board.

Note 3: Unless otherwise specified, all limits guaranteed for $T_A = T_J$ = 25°C with supply voltage = ±15V, V_{CM} = 0V, and $r_l \geq$ 100 KΩ **Boldface** limits apply over the range listed under "Operating Temperature Range".

Note 4: All limits guaranteed at room temperature (standard type face) and at **temperature extremes.** All limits are 100% production tested.

Note 5: All limits guaranteed at room temperature (standard type face) and at **temperature extremes.** All limits are guaranteed via correlation using standard Statistical Quality Control (SQC) methods.

Note 6: For single supply operation, the following conditions apply: V+ = 5V, V− = 0V, V_{CM} = 2.5V, V_{OUT} = 2.5V. Pin 1 & Pin 8 (V_{OS} Adjust) are each connected to Pin 4 (V−) to realize maximum output swing. This connection will degrade V_{OS}.

Note 7: $C_L \leq$ 5 pF.

Note 8: In order to achieve optimum AC performance, the input stage was designed without protective clamps. Exceeding the maximum differential input voltage results in reverse breakdown of the base-emitter junction of one of the input transistors and probable degradation of the input parameters (especially V_{OS}, I_{OS}, and Noise).

Note 9: The average voltage that the weakest pin combinations (those involving Pin 2 or Pin 3) can withstand and still conform to the datasheet limits. The test circuit used consists of the human body model of 100 pF in series with 1500Ω.

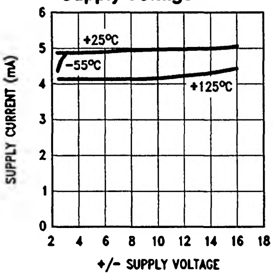
Note 10: V_{IN} = 4V step. For supply = ±5V, V_{IN} = 1V step.

Note 11: Voltage Gain is the total output swing (20V) divided by the input signal required to produce that swing.

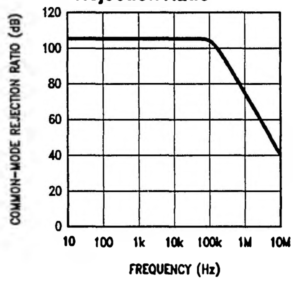
Note 12: The voltage between V^+ and either input pin must not exceed 36V.

Typical Performance Characteristics (R_L = 10 kΩ, T_A = 25°C unless otherwise specified)

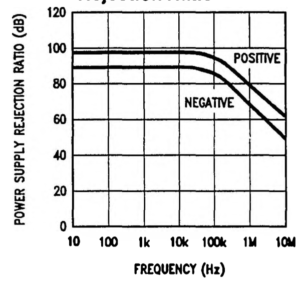
Supply Current vs Supply Voltage



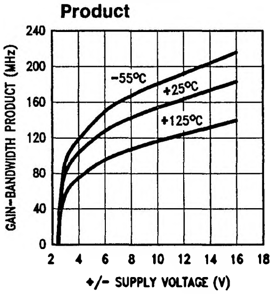
Common-Mode Rejection Ratio



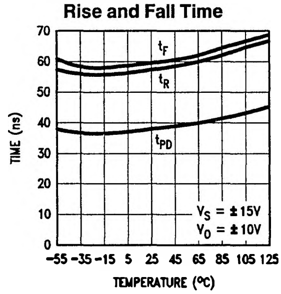
Power Supply Rejection Ratio



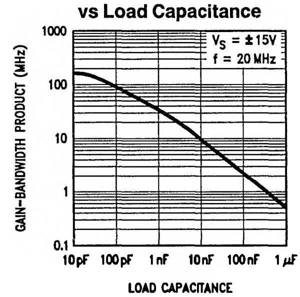
Gain-Bandwidth Product



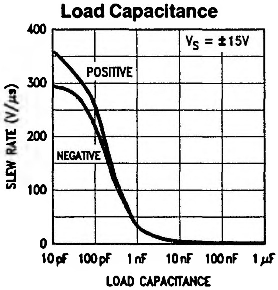
Propagation Delay Rise and Fall Time



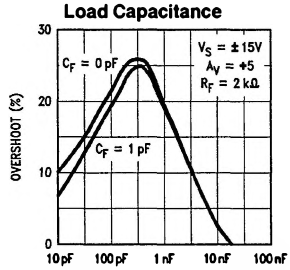
Gain-Bandwidth Product vs Load Capacitance



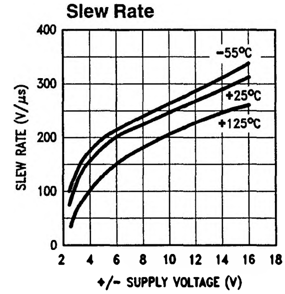
Slew Rate vs Load Capacitance



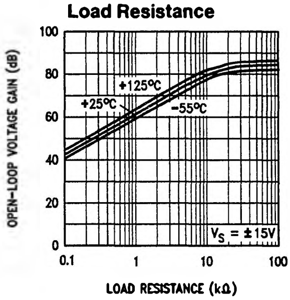
Overshoot vs Load Capacitance



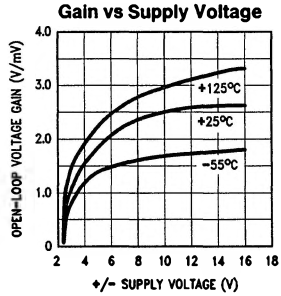
Slew Rate



Voltage Gain vs Load Resistance



Gain vs Supply Voltage



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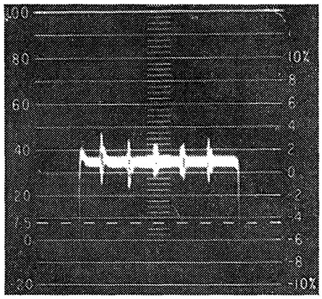
Typical Performance Characteristics

(R_L = 10 kΩ, T_A = 25°C unless otherwise specified) (Continued)

Differential Gain (Note)



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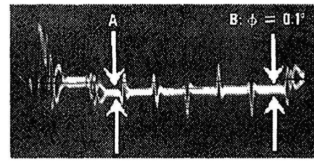
Differential Phase (Note)



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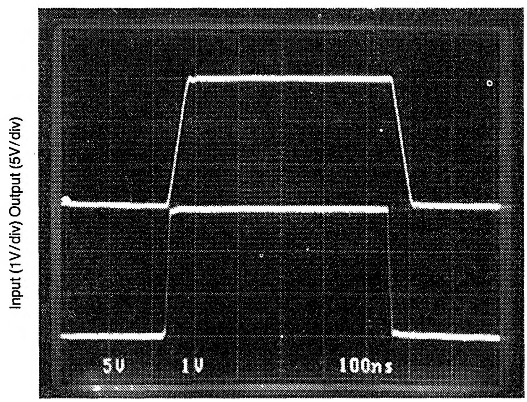
Note: Differential gain and differential phase measured for four series LM6364 op amps configured as unity-gain followers, in series with an LM6321 buffer. Error added by LM6321 is negligible. Test performed using Tektronix Type 520 NTSC test system.

Step Response; Av = +5



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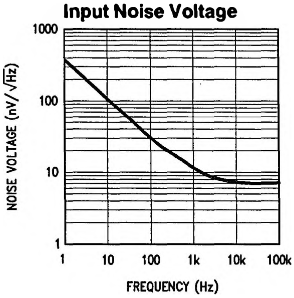
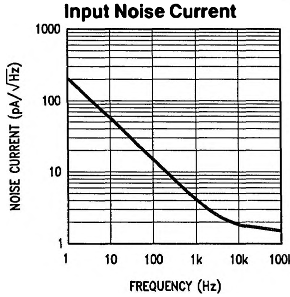
TIME (50 ns/div)

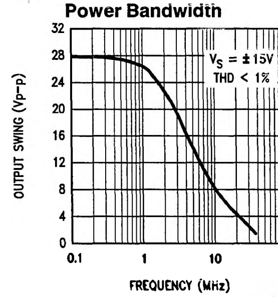
Input Noise Voltage



Input Noise Current



Power Bandwidth



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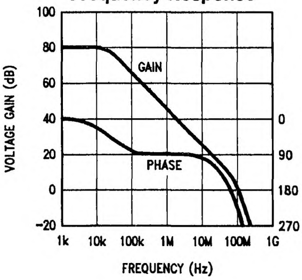
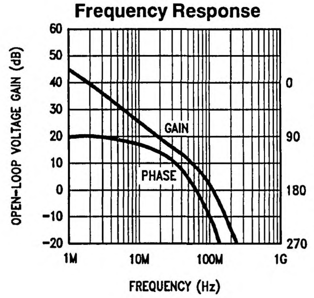
Typical Performance Characteristics

(R_L = 10 kΩ, T_A = 25°C unless otherwise specified) (Continued)

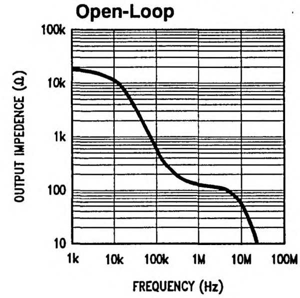
Open-Loop Frequency Response



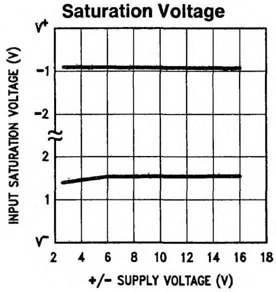
Open-Loop Frequency Response



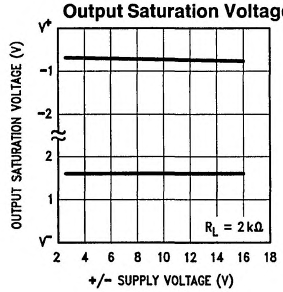
Output Resistance Open-Loop



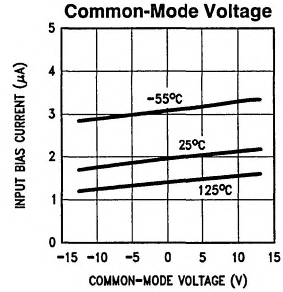
Common-Mode Input Saturation Voltage



Output Saturation Voltage



Bias Current vs Common-Mode Voltage



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Applications Tips

The LM6364 has been compensated for gains of 5 or greater (over specified ranges of temperature, power supply voltage, and load). Since this compensation involved adding emitter-degeneration resistors in the op amp's input stage, the open-loop gain was reduced as the stability increased. Gain error due to reduced A_{VOL} is most apparent at high gains; thus, the uncompensated LM6365 is appropriate for gains of 25 or more. If unity-gain operation is desired, the LM6361 should be used. The LM6361, LM6364, and LM6365 have the same high slew rate (typically 300 V/μs), regardless of their compensation.

The LM6364 is unusually tolerant of capacitive loads. Most op amps tend to oscillate when their load capacitance is greater than about 200 pF (in low-gain circuits). However, load capacitance on the LM6364 effectively increases its compensation capacitance, thus slowing the op amp's response and reducing its bandwidth. The compensation is not ideal, though, and ringing or oscillation may occur in low-gain circuits with large capacitive loads. To overcompensate the LM6364 for operation at gains less than 5, a series resistor-capacitor network should be added between the input pins (as shown in the Typical Applications, Noise Gain Compensation) so that the high-frequency noise gain rises to at least 5.

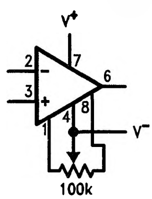
Power supply bypassing will improve the stability and transient response of the LM6364, and is recommended for every design. 0.01 μF to 0.1 μF ceramic capacitors should be used (from each supply "rail" to ground); if the device is far away from its power supply source, an additional 2.2 μF to 10 μF (tantalum) may be required for extra noise reduction.

Keep all leads short to reduce stray capacitance and lead inductance, and make sure ground paths are low-impedance, especially where heavier currents will be flowing. Stray capacitance in the circuit layout can cause signal coupling between adjacent nodes, so that circuit gain unintentionally varies with frequency.

Breadboarded circuits will work best if they are built using generic PC boards with a good ground plane. If the op amps are used with sockets, as opposed to being soldered into the circuit, the additional input capacitance may degrade circuit performance.

Typical Applications

Offset Voltage Adjustment



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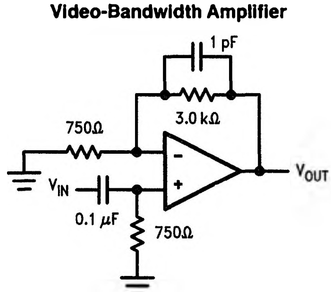
Video-Bandwidth Amplifier



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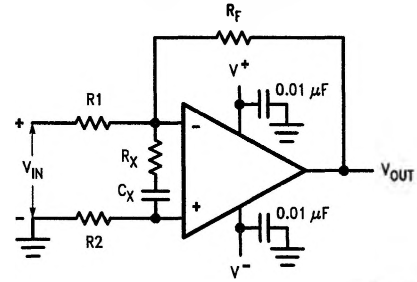
Noise-Gain Compensation for Gains ≤5



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$R_XC_X \geq (2\pi \cdot 25\text{ MHz})^{-1}$
$5\ R_X = R_1 + R_F(1 + R_1/R_2)$