

Ordering number: EN3035A

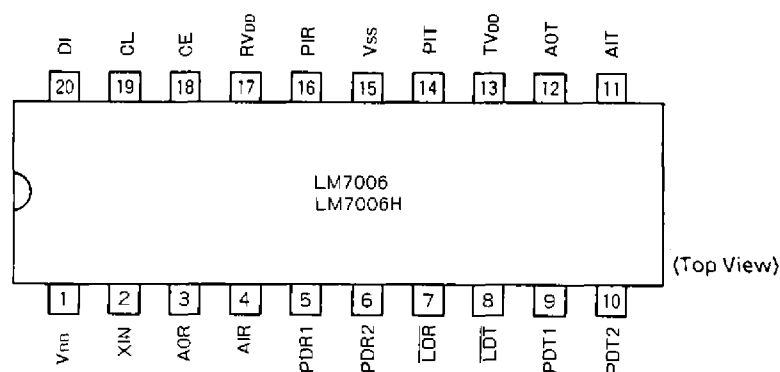
|  |          |                      |
|--|----------|----------------------|
| <b>SANYO</b>                           | No.3035A | NMOS LSI             |
|  |          | <b>LM7006, 7006H</b> |
| Dual PLL Frequency Synthesizer Circuit |          |                      |

#### Overview

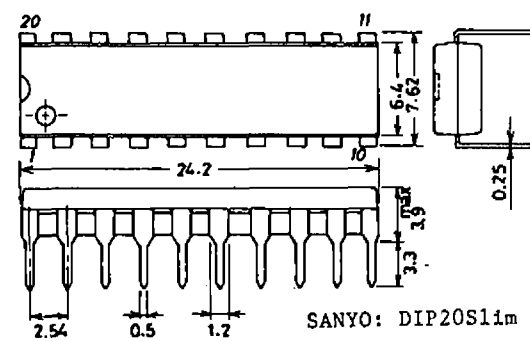
The LM7006, 7006H is a PLL Frequency Synthesizer circuit for use in cordless telephones. It incorporates separate programmable dividers, phase comparators and dual-gain charge pumps for the transmit and receive sides. (Transmit side is operated by an independent power supply for standby function.) Device operation is controlled by a 40-bit serial input word, enabling simple control from a micro-controller by CCB.

The LM7006, 7006H is available in a 20-pin plastic DIP (300MIL). It operates from a single 4.0 to 5.5V supply.

#### Pin Assignment : DIP20S



#### Package Dimensions 3021B-D20SIC (unit : mm)

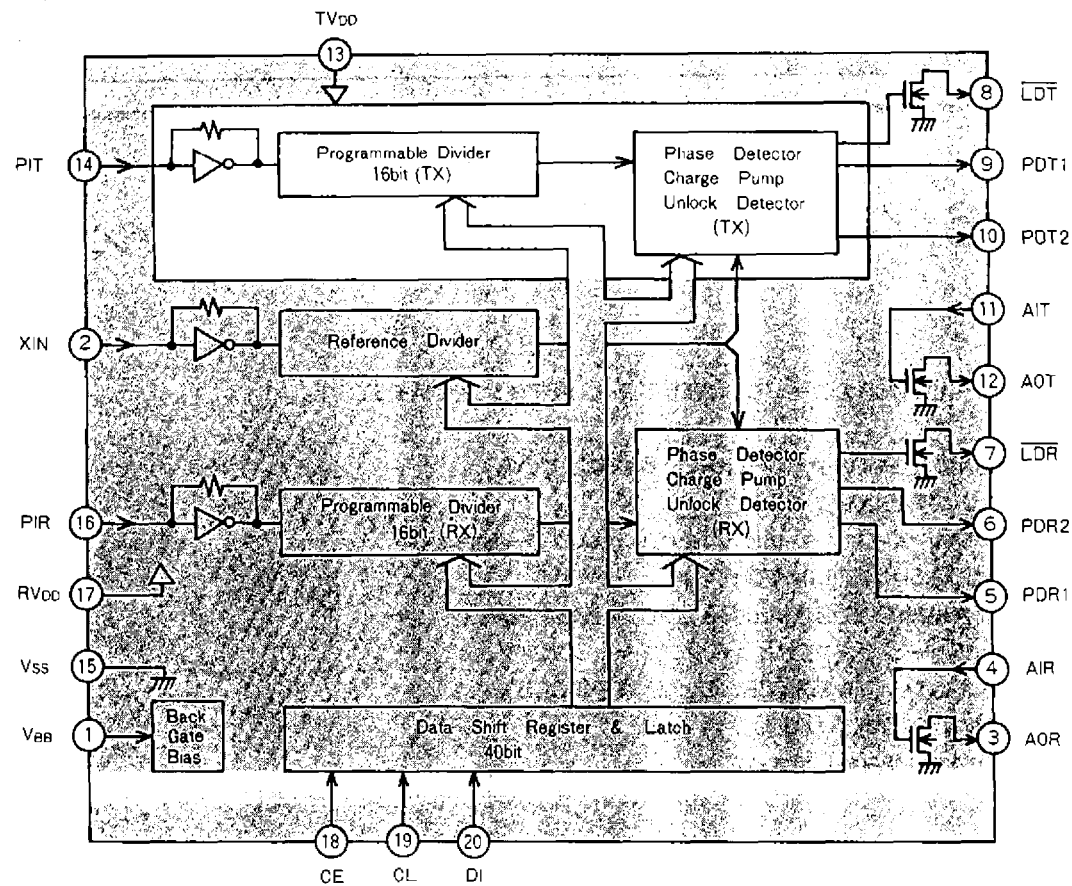


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8090JN,TA/3249TA/2019YT,TS (US) No.3035-1/7

# LM7006, 7006H

## Equivalent Circuit Block Diagram



|          |  |         |                                    |
|----------|--|---------|------------------------------------|
| PIT      | : TX local OSC signal input                | LDT     | : TX unlock detection (open-drain) |
| XIN      | : Reference OSC signal input (12.800MHz)   | PDT1    | : TX Charge pump output (main)     |
| PIR      | : RX local OSC signal input                | PDT2    | : TX Charge pump output (sub)      |
| RVDD     | : Power supply other than TVDD             | AIT,AOT | : TX Tr for L.P.F amp              |
| VSS      | : Ground                                   | LDR     | : RX unlock detection (open-drain) |
| VBB      | : Back gate bias pin                       | PDR1    | : RX Charge pump output (main)     |
| CE,CL,DI | : Serial data input                        | PDR2    | : RX Charge pump output (sub)      |
| TVDD     | : TX PLL supply ( : <input type="text"/> ) | AIR,AOR | : RX Tr for L.P.F amp              |

| Absolute Maximum Ratings at Ta = 25°C, VSS = 0V |            |                       |                 | unit |
|---|------------|-----------------------|-----------------|------|
| Supply Voltage                                  | VDD max    | RVDD,TVDD             | -0.3 to +6.0    | V    |
| Back Gate Bias                                  | VBB max    | VBB                   | -4.0 to -2.0    | V    |
| Input Voltage                                   | VIN(1) max | CE,CL,DI,AIR,AIT      | -0.3 to +7.0    | V    |
|   | VIN(2) max | All other input pins  | -0.3 to VDD+0.3 | V    |
| Output Voltage                                  | VOU(1) max | AOR,AOT,LDR,LDT       | -0.3 to +7.0    | V    |
|   | VOU(2) max | All other output pins | -0.3 to VDD+0.3 | V    |
| Output Current                                  | IOU(1) max | AOR,AOT,LDR,LDT       | 0 to 2.0        | mA   |
| Allowable Power Dissipation                     | Pd max     | Ta ≤ 75°C             | 350             | mW   |
| Operating Temperature                           | Topr       |                       | -40 to +75      | °C   |
| Storage Temperature                             | Tstg       |                       | -55 to +125     | °C   |

Note : Pins PIR and PIT are susceptible to damage by static discharge. Appropriate precautions should be taken during handling and operation.

# LM7006, 7006H

| Allowable Operating Conditions at Ta = -40 to +75°C, VSS = 0V   |                      |                          |   | min    | typ  | max  | unit  |
|---|----------------------|--------------------------|---|--------|------|------|-------|
| Supply Voltage  | VDD                  | RVDD, TVDD               |   | 4.0    |      | 5.5  | V     |
| Input 'H'-Level Voltage   | VIH                  | CE, CL, DI               |   | 2.5    |      | 5.5  | V     |
| Input 'L'-Level Voltage   | VIL                  | CE, CL, DI               |   | 0      |      | 0.5  | V     |
| Output Voltage  | VOU                  | AOR, AOT, LDR, LDT       |   | 0      |      | 5.5  | V     |
| Input Frequency   | fIN(1)               | XIN                      | Sine wave, capacitive coupling<br>VIN(1) = 50mVrms        | 3.0    | 12.8 | 13.5 | MHz   |
|   | fIN(2)               | PIR, PIT                 | Sine wave, capacitive coupling<br>VIN(2) = 70mVrms        | 200    |      | 400  | MHz   |
| Input Voltage   | VIN(1)               | XIN                      | Sine wave, capacitive coupling<br>fIN(1) = 3.0 to 13.5MHz | 50     |      | 1000 | mVrms |
|   | VIN(2)               | PIR, PIT                 | Sine wave, capacitive coupling<br>fIN(2) = 200 to 400MHz  | 70     |      | 500  | mVrms |
| Electrical Characteristics under Allowable Operating Conditions |                      |                          |   | min    | typ  | max  | unit  |
| Internal Feedback Resistor                                      | Rf                   | XIN, PIR, PIT            |   |        | 500  |      | kΩ    |
| Hysteresis Width  | Vh                   | CE, CL, DI               |   | 0.1    | 0.5  |      | V     |
| Input 'H'-Level Current   | I <sub>IH</sub> (1)  | CE, CL, DI               | V <sub>I</sub> = 5.5V                                     |        |      | 5.0  | μA    |
|   | I <sub>IH</sub> (2)  | XIN, PIR, PIT            | V <sub>I</sub> = VDD                                      |        |      | 40   | μA    |
|   | I <sub>IH</sub> (3)  | AIR, AIT                 | V <sub>I</sub> = 5.5V                                     |        | 0.01 | 10.0 | nA    |
| Input 'L'-Level Current   | I <sub>IL</sub> (1)  | CE, CL, DI               | V <sub>I</sub> = VSS                                      |        |      | 5.0  | μA    |
|   | I <sub>IL</sub> (2)  | XIN, PIR, PIT            | V <sub>I</sub> = VSS                                      |        |      | 40   | μA    |
|   | I <sub>IL</sub> (3)  | AIR, AIT                 | V <sub>I</sub> = VSS                                      |        | 0.01 | 10.0 | nA    |
| Output 'H'-Level Voltage  | VOH                  | PDR1, PDR2<br>PDT1, PDT2 | I <sub>O</sub> = 0.1mA                                    | 0.6VDD |      |      | V     |
| Output 'L'-Level Voltage  | VOL(1)               | PDR1, PDR2<br>PDT1, PDT2 | I <sub>O</sub> = 0.1mA                                    |        |      | 0.3  | V     |
|   | VOL(2)               | LDR, LDT                 | I <sub>O</sub> = 1.0mA                                    |        |      | 1.0  | V     |
|   | VOL(3)               | AOR, AOT                 | I <sub>O</sub> = 0.5mA                                    |        |      | 0.5  | V     |
| Output OFF-State Leakage Current                                | I <sub>OFF</sub> (1) | LDR, LDT                 | V <sub>O</sub> = 5.5V                                     |        |      | 5.0  | μA    |
|   | I <sub>OFF</sub> (2) | AOR, AOT                 | V <sub>O</sub> = 5.5V                                     |        |      | 1.0  | μA    |
|   | I <sub>OFF</sub> (3) | PDR1, PDR2<br>PDT1, PDT2 | V <sub>O</sub> = 0.3V, V <sub>O</sub> = 5.5V              |        | 0.01 | 10.0 | nA    |
| Input Capacitance   | CIN                  | XIN, PIR, PIT            |   |        | 2.5  |      | pF    |
| Supply Current  | I <sub>DD</sub> (1)  | RVDD                     | ※1  |        | 23   | 32   | mA    |
|   | I <sub>DD</sub> (2)  | RVDD + TVDD              | ※2  |        | 45   | 62   | mA    |

## LM7006 and LM7006H Difference

|         |                 |             |               | min | typ | max | unit |
|---------|-----------------|-------------|---------------|-----|-----|-----|------|
| LM7006  | I <sub>DD</sub> | RVDD + TVDD | ※2, Ta = 25°C |     |     | 50  | mA   |
| LM7006H | I <sub>DD</sub> | RVDD + TVDD | ※2, Ta = 25°C | 50  |     | 55  | mA   |

※1 XIN = 12.8MHz,  
PIR = 400MHz (70mVrms),  
other inputs : VSS,  
outputs : open

※2 XIN = 12.8MHz,  
PIR = 400MHz (70mVrms),  
PIT = 400MHz (70mVrms),  
other inputs : VSS,  
outputs : open

Note : The LM7006H is distinguished by an orange marking. I<sub>DD</sub> is the only difference between the two devices.

# LM7006, 7006H

## Pin Description

| Pin Name     | Pin No.  | Input/Output                        | Description   |
|--------------|----------|-------------------------------------|---|
| XIN          | 2        | Input                               | Reference OSC input<br>12.800MHz, 50mVrms minimum (TCX0)  |
| PIT          | 14       | Input                               | Transmit VCO input<br>200 to 400MHz, 70mVrms minimum. Division ratio of transmit programmable divider is set by the TD0 to TD15 control bits to between 256 and 65535.  |
| PIR          | 16       | Input                               | Receive VCO input<br>200 to 400MHz, 70mVrms minimum. Division ratio of receive programmable divider is set by the RD0 to RD15 control bits to between 256 and 65535.  |
| RVDD         | 17       | —                                   | Receive section power supply<br>4.0 to 5.5V to data shift register latch, reference divider, RX programmable divider, RX phase detector, RX unlock detector.  |
| TVDD         | 13       | —<br>※1                             | Transmit section power supply<br>4.0 to 5.5V to TX programmable divider, TX phase detector, TX unlock detector.   |
| VBB          | 1        | Output                              | Back gate bias pin<br>Requires a 0.01μF capacitor between VBB and ground.   |
| VSS          | 15       | —                                   | Ground  |
| LDT<br>LDR   | 8<br>7   | Output<br>[N-channel<br>Open drain] | N-channel open-drain lock/unlock outputs for transmit and receive PLLs<br>Lock : High-impedance<br>Unlock : LOW<br>The lock/unlock phase boundary is set by the UD0 to UD2 control bits. Extension of the phase difference signal is selected by the UE control flag.   |
| PDT1<br>PDR1 | 9<br>5   | Output<br>(Tri-state)               | Tri-state main charge pump outputs for transmit and receive PLLs<br>Driven by the phase error signal obtained by comparing PLL frequency divided by N (fosc/N) with the reference frequency (fref)<br>fosc/N > fref or leading: positive pulses<br>fosc/N < fref or lagging: negative pulses<br>fosc/N = fref: high-impedance |
| PDT2<br>PDR2 | 10<br>6  | Output<br>(Tri-state)               | Tri-state auxiliary charge pump outputs for transmit and receive PLLs<br>Driven by the PLLs phase error outputs only while PLL is out of lock, and high-impedance while PLL is in the lock range set by UD0 to UD2. Same polarity as main charge pump outputs.  |
| AIT<br>AOR   | 11<br>12 | Input<br>Output                     | MOS N-channel transistor for TX PLL loop filter   |
| AIR<br>AOR   | 4<br>3   | Input<br>Output                     | MOS N-channel transistor for RX PLL loop filter   |
| CE           | 18       | Input<br>※2                         | Chip enable input<br>A HIGH level enables serial data transfer into the LM7006.   |
| CL           | 19       | Input ※2                            | Serial input data clock   |
| DI           | 20       | Input ※2                            | Serial data input   |

※1 TVDD Pin is connected to VSS when transmit circuit is in power-off state (standby mode).

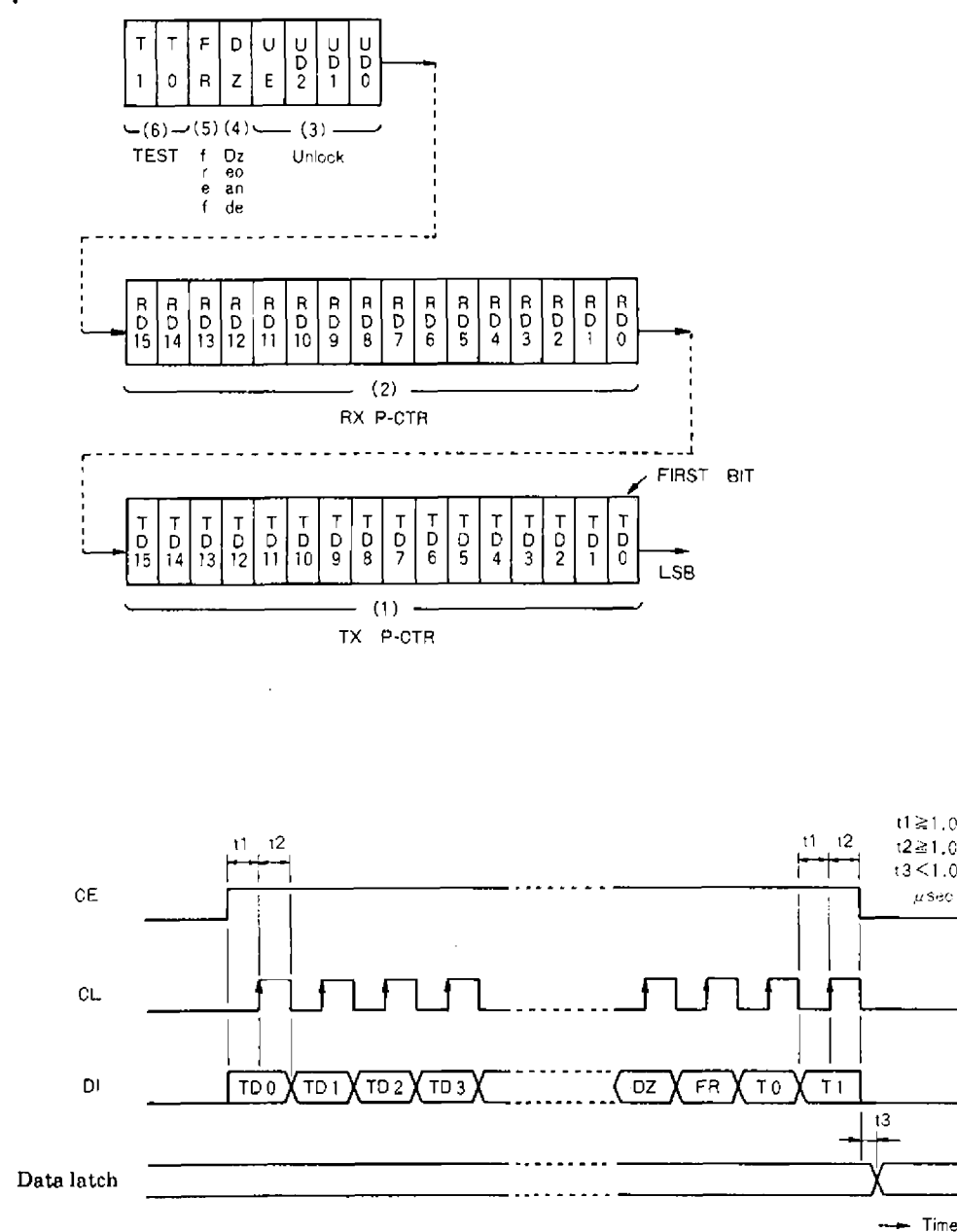
For instance, connect resistor (47kΩ to 100kΩ) between TVDD and VSS.

※2 High and Low input voltages on CE, CL, DI are held in the following range, respectively, regardless of the supply voltage (RVDD).

V<sub>IH</sub> = 2.5 to 5.5V, V<sub>IL</sub> = 0 to 0.5V

## LM7006, 7006H

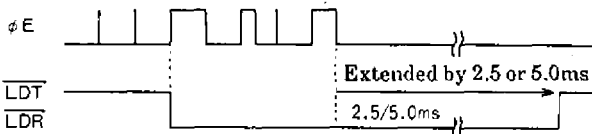
### Device Control



※ As the state of output pins of the LM7006 is unsettled when power is applied to them, the data must be sent from microcontroller as soon as possible.

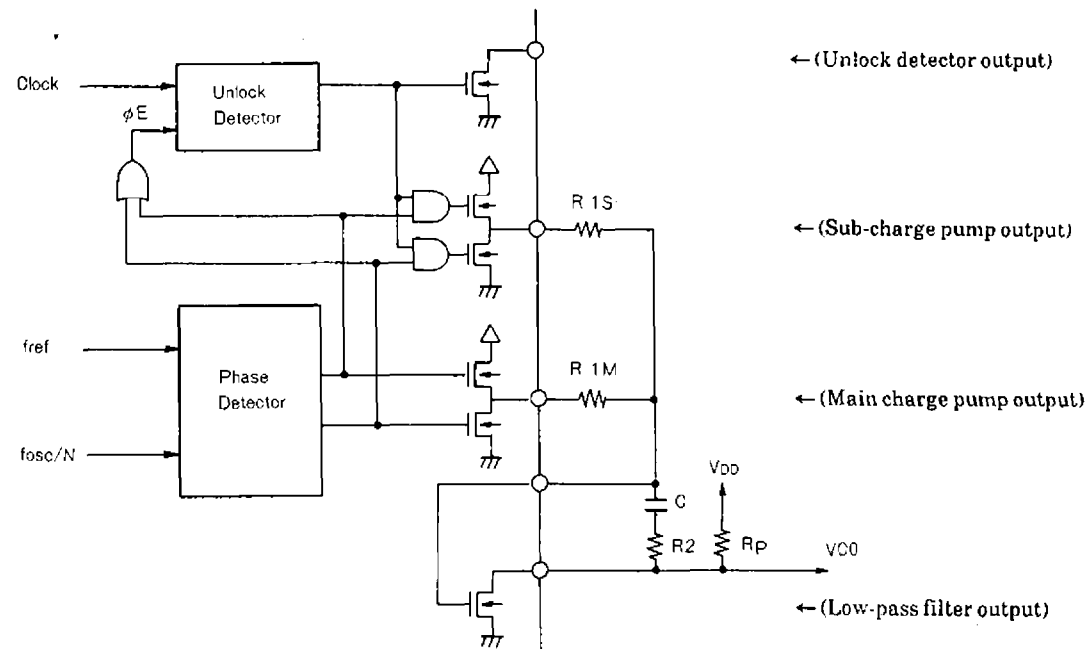
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LM7006, 7006H

| No.          | Data   | Description   | Associated data bits       |   |     |             |   |   |   |   |      |              |   |   |   |      |                 |   |   |   |      |                 |   |   |   |      |                 |   |   |   |      |                 |   |   |   |      |                 |   |   |   |      |                 |   |   |   |      |                  |             |    |   |      |     |  |              |   |   |  |   |   |  |
|--------------|--|---|----------------------------|---|-----|-------------|---|---|---|---|------|--------------|---|---|---|------|-----------------|---|---|---|------|-----------------|---|---|---|------|-----------------|---|---|---|------|-----------------|---|---|---|------|-----------------|---|---|---|------|-----------------|---|---|---|------|------------------|-------------|----|---|------|-----|--|--------------|---|---|--|---|---|--|
| (1)          | TX Programmable Divider :<br>TD0 to TD15                 | TD0 to TD15 form the TX side programmable divider ratio. TD0 is the least significant bit, and TD15 the most significant bit. The divider ratio must be between 256 and 65535, inclusive.   | FR                         |   |     |             |   |   |   |   |      |              |   |   |   |      |                 |   |   |   |      |                 |   |   |   |      |                 |   |   |   |      |                 |   |   |   |      |                 |   |   |   |      |                 |   |   |   |      |                  |             |    |   |      |     |  |              |   |   |  |   |   |  |
| (2)          | RX Programmable Divider :<br>RD0 to RD15                 | RD0 to RD15 form the RX side programmable divider ratio. RD0 is the least significant bit, and RD15 the most significant bit. The divider ratio must be between 256 and 65535, inclusive.   | FR                         |   |     |             |   |   |   |   |      |              |   |   |   |      |                 |   |   |   |      |                 |   |   |   |      |                 |   |   |   |      |                 |   |   |   |      |                 |   |   |   |      |                 |   |   |   |      |                  |             |    |   |      |     |  |              |   |   |  |   |   |  |
| (3)          | UD0<br>UD1<br>UD2<br><br>Unlock Detector Control :<br>UE | <p>UD0 to UD2 set the lock detector phase difference lock/unlock limit, as shown in the table below.</p> <table><tr><th>UD2</th><th>UD1</th><th>UD0</th><th>Signal Name</th><th>Phase Difference (<math>\phi E</math>)<br/>Detection Width (<math>\mu</math>sec)</th></tr><tr><td>0</td><td>0</td><td>0</td><td>ULD0</td><td><math>\phi E &gt; 0</math></td></tr><tr><td>0</td><td>0</td><td>1</td><td>ULD1</td><td><math>\phi E &gt; 1.25</math></td></tr><tr><td>0</td><td>1</td><td>0</td><td>ULD2</td><td><math>\phi E &gt; 0.30</math></td></tr><tr><td>0</td><td>1</td><td>1</td><td>ULD3</td><td><math>\phi E &gt; 5.00</math></td></tr><tr><td>1</td><td>0</td><td>0</td><td>ULD4</td><td><math>\phi E &gt; 0.15</math></td></tr><tr><td>1</td><td>0</td><td>1</td><td>ULD5</td><td><math>\phi E &gt; 2.50</math></td></tr><tr><td>1</td><td>1</td><td>0</td><td>ULD6</td><td><math>\phi E &gt; 0.60</math></td></tr><tr><td>1</td><td>1</td><td>1</td><td>ULD7</td><td><math>\phi E &gt; 10.00</math></td></tr></table> <p>UE controls the format of the lock detector <math>\overline{LDT}</math> and <math>\overline{LDR}</math> output signals. The figure below illustrates this operation.</p> <table><tr><th>Signal Name</th><th>UE</th><th><math>\overline{LDT}/\overline{LDR}</math> Outputs</th></tr><tr><td>ULD0</td><td>0/1</td><td>Directly output the phase error signal</td></tr><tr><td>ULD0 to ULD7</td><td>0</td><td>The phase error signal is extended by 2.5ms</td></tr><tr><td></td><td>1</td><td>The phase error signal is extended by 5.0ms</td></tr></table>  | UD2                        | UD1   | UD0 | Signal Name | Phase Difference ( $\phi E$ )<br>Detection Width ( $\mu$ sec) | 0 | 0 | 0 | ULD0 | $\phi E > 0$ | 0 | 0 | 1 | ULD1 | $\phi E > 1.25$ | 0 | 1 | 0 | ULD2 | $\phi E > 0.30$ | 0 | 1 | 1 | ULD3 | $\phi E > 5.00$ | 1 | 0 | 0 | ULD4 | $\phi E > 0.15$ | 1 | 0 | 1 | ULD5 | $\phi E > 2.50$ | 1 | 1 | 0 | ULD6 | $\phi E > 0.60$ | 1 | 1 | 1 | ULD7 | $\phi E > 10.00$ | Signal Name | UE | $\overline{LDT}/\overline{LDR}$ Outputs | ULD0 | 0/1 | Directly output the phase error signal | ULD0 to ULD7 | 0 | The phase error signal is extended by 2.5ms |  | 1 | The phase error signal is extended by 5.0ms |  |
| UD2          | UD1  | UD0   | Signal Name                | Phase Difference ( $\phi E$ )<br>Detection Width ( $\mu$ sec) |     |             |   |   |   |   |      |              |   |   |   |      |                 |   |   |   |      |                 |   |   |   |      |                 |   |   |   |      |                 |   |   |   |      |                 |   |   |   |      |                 |   |   |   |      |                  |             |    |   |      |     |  |              |   |   |  |   |   |  |
| 0            | 0  | 0   | ULD0                       | $\phi E > 0$  |     |             |   |   |   |   |      |              |   |   |   |      |                 |   |   |   |      |                 |   |   |   |      |                 |   |   |   |      |                 |   |   |   |      |                 |   |   |   |      |                 |   |   |   |      |                  |             |    |   |      |     |  |              |   |   |  |   |   |  |
| 0            | 0  | 1   | ULD1                       | $\phi E > 1.25$   |     |             |   |   |   |   |      |              |   |   |   |      |                 |   |   |   |      |                 |   |   |   |      |                 |   |   |   |      |                 |   |   |   |      |                 |   |   |   |      |                 |   |   |   |      |                  |             |    |   |      |     |  |              |   |   |  |   |   |  |
| 0            | 1  | 0   | ULD2                       | $\phi E > 0.30$   |     |             |   |   |   |   |      |              |   |   |   |      |                 |   |   |   |      |                 |   |   |   |      |                 |   |   |   |      |                 |   |   |   |      |                 |   |   |   |      |                 |   |   |   |      |                  |             |    |   |      |     |  |              |   |   |  |   |   |  |
| 0            | 1  | 1   | ULD3                       | $\phi E > 5.00$   |     |             |   |   |   |   |      |              |   |   |   |      |                 |   |   |   |      |                 |   |   |   |      |                 |   |   |   |      |                 |   |   |   |      |                 |   |   |   |      |                 |   |   |   |      |                  |             |    |   |      |     |  |              |   |   |  |   |   |  |
| 1            | 0  | 0   | ULD4                       | $\phi E > 0.15$   |     |             |   |   |   |   |      |              |   |   |   |      |                 |   |   |   |      |                 |   |   |   |      |                 |   |   |   |      |                 |   |   |   |      |                 |   |   |   |      |                 |   |   |   |      |                  |             |    |   |      |     |  |              |   |   |  |   |   |  |
| 1            | 0  | 1   | ULD5                       | $\phi E > 2.50$   |     |             |   |   |   |   |      |              |   |   |   |      |                 |   |   |   |      |                 |   |   |   |      |                 |   |   |   |      |                 |   |   |   |      |                 |   |   |   |      |                 |   |   |   |      |                  |             |    |   |      |     |  |              |   |   |  |   |   |  |
| 1            | 1  | 0   | ULD6                       | $\phi E > 0.60$   |     |             |   |   |   |   |      |              |   |   |   |      |                 |   |   |   |      |                 |   |   |   |      |                 |   |   |   |      |                 |   |   |   |      |                 |   |   |   |      |                 |   |   |   |      |                  |             |    |   |      |     |  |              |   |   |  |   |   |  |
| 1            | 1  | 1   | ULD7                       | $\phi E > 10.00$  |     |             |   |   |   |   |      |              |   |   |   |      |                 |   |   |   |      |                 |   |   |   |      |                 |   |   |   |      |                 |   |   |   |      |                 |   |   |   |      |                 |   |   |   |      |                  |             |    |   |      |     |  |              |   |   |  |   |   |  |
| Signal Name  | UE   | $\overline{LDT}/\overline{LDR}$ Outputs   |                            |   |     |             |   |   |   |   |      |              |   |   |   |      |                 |   |   |   |      |                 |   |   |   |      |                 |   |   |   |      |                 |   |   |   |      |                 |   |   |   |      |                 |   |   |   |      |                  |             |    |   |      |     |  |              |   |   |  |   |   |  |
| ULD0         | 0/1  | Directly output the phase error signal  |                            |   |     |             |   |   |   |   |      |              |   |   |   |      |                 |   |   |   |      |                 |   |   |   |      |                 |   |   |   |      |                 |   |   |   |      |                 |   |   |   |      |                 |   |   |   |      |                  |             |    |   |      |     |  |              |   |   |  |   |   |  |
| ULD0 to ULD7 | 0  | The phase error signal is extended by 2.5ms   |                            |   |     |             |   |   |   |   |      |              |   |   |   |      |                 |   |   |   |      |                 |   |   |   |      |                 |   |   |   |      |                 |   |   |   |      |                 |   |   |   |      |                 |   |   |   |      |                  |             |    |   |      |     |  |              |   |   |  |   |   |  |
|              | 1  | The phase error signal is extended by 5.0ms   |                            |   |     |             |   |   |   |   |      |              |   |   |   |      |                 |   |   |   |      |                 |   |   |   |      |                 |   |   |   |      |                 |   |   |   |      |                 |   |   |   |      |                 |   |   |   |      |                  |             |    |   |      |     |  |              |   |   |  |   |   |  |
| (4)          | Dead Zone Control :<br>DZ                                | Selects the width of the phase comparator insensitive region.<br>DZ=0 : narrow<br>DZ=1 : wide   |                            |   |     |             |   |   |   |   |      |              |   |   |   |      |                 |   |   |   |      |                 |   |   |   |      |                 |   |   |   |      |                 |   |   |   |      |                 |   |   |   |      |                 |   |   |   |      |                  |             |    |   |      |     |  |              |   |   |  |   |   |  |
| (5)          | Reference frequency Select :<br>FR                       | FR=0 : reference frequency = 25.0kHz<br>FR=1 : reference frequency = 12.5kHz  | TD0 to TD15<br>RD0 to RD15 |   |     |             |   |   |   |   |      |              |   |   |   |      |                 |   |   |   |      |                 |   |   |   |      |                 |   |   |   |      |                 |   |   |   |      |                 |   |   |   |      |                 |   |   |   |      |                  |             |    |   |      |     |  |              |   |   |  |   |   |  |
| (6)          | Device Test Flags :<br>T0,T1                             | T0 and T1 are used to test the LM7006. They should both be set to "0" for normal operation.   |                            |   |     |             |   |   |   |   |      |              |   |   |   |      |                 |   |   |   |      |                 |   |   |   |      |                 |   |   |   |      |                 |   |   |   |      |                 |   |   |   |      |                 |   |   |   |      |                  |             |    |   |      |     |  |              |   |   |  |   |   |  |

## LM7006, 7006H

### Dual Charge Pump



The dual charge pump circuit ensures good performance during normal tracking and fast lock-in shown input frequency changes. During normal operation, only the main charge pump is employed to keep the PLL in sync. The auxiliary charge pump output is high-impedance. The loop filter time constant is relatively high, thus ensuring good sideband and modulation characteristics. When channels are changed, the PLL will lose lock and the auxiliary charge pump is activated. The filter resistor now consists of both R1S and R1M in parallel, reducing the filter time constant. PLL lock-in is thus accelerated.

### Sample Application Circuit

