Ordering number: EN3888

NMOS LSI

No. 3888

LM7007M, LM7007HM

Dual-PLL Frequency Synthesizers

OVERVIEW

The LM7007M and LM7007HM are dual-PLL frequency synthesizer ICs for use in 250 to 380 MHz cordless telephone transceivers.

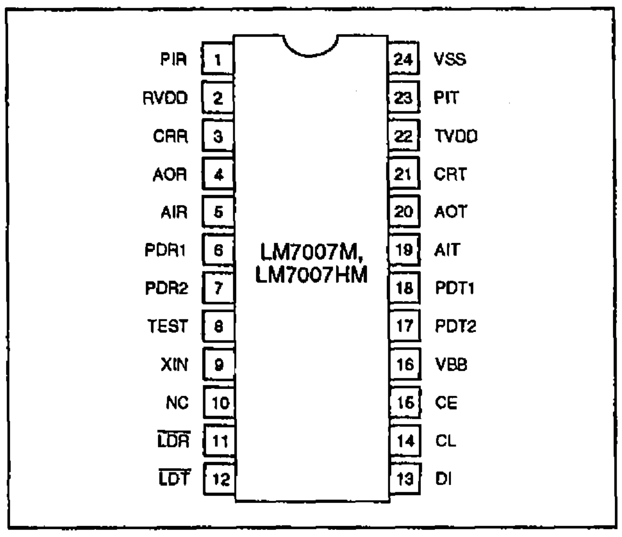
The LM7007M and LM7007HM comprise two PLL circuits, 16-bit transmit and receive programmable dividers, a temperature-compensated crystal oscillator (TCXO) amplifier and two transistors for external low-pass filters (LPF). Each PLL comprises a dual charge pump and fast-lockup circuit. The standard TCXO frequencies are 10.625, 12.8 and 21.25 MHz. Serial data transfer is controlled from a three-wire, serial, computer control bus (C^2B).

The LM7007H and LM7007HM operate from a 2.8 to 4.5 V supply and are available in 24-pin MFPs.

FEATURES

- Dual charge pump and fast-lockup circuit in each PLL for rapid locking
- 10.625, 12.8 and 21.25 MHz TCXO frequencies
- TCXO input amplifier
- Dual LPF transistors
- C^2B serial interface
- 2.8 to 4.5 V supply
- 24-pin MFP

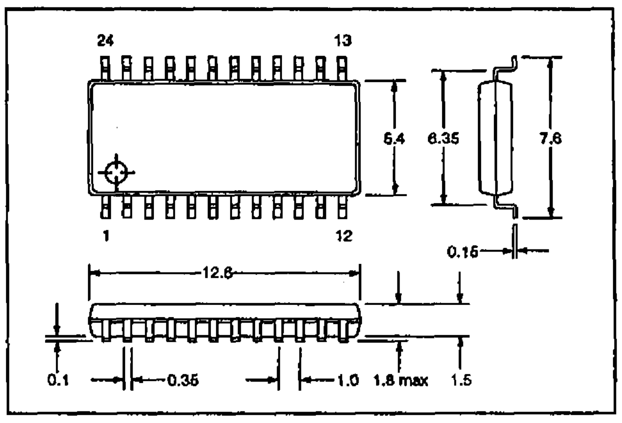
PINOUT



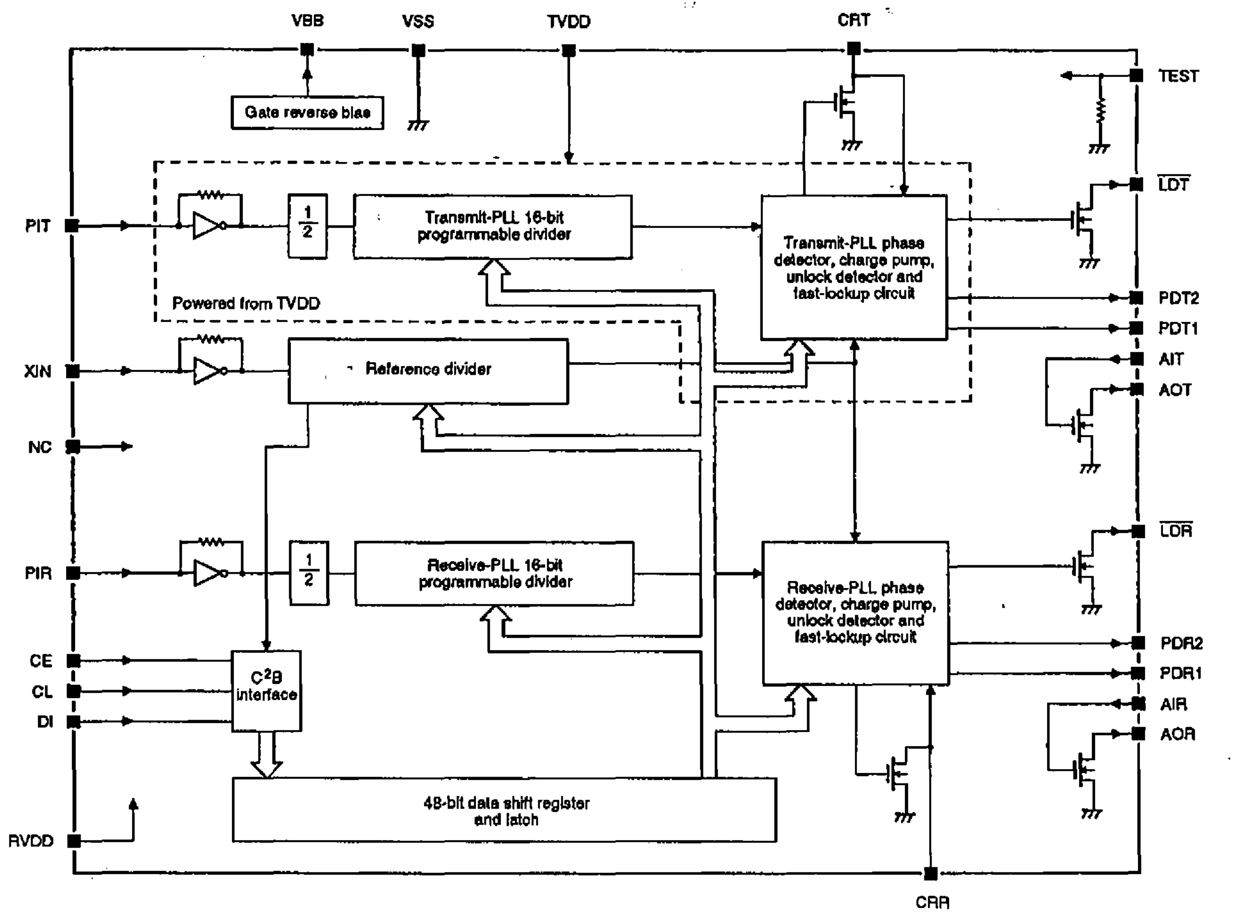
PACKAGE DIMENSIONS

Unit: mm

3112-MFP24S



BLOCK DIAGRAM



PIN DESCRIPTION

Number	Name	Description
1	PIR	Receive-PLL local-oscillator input
2	RVDD	Receive-PLL 2.8 to 4.5 V supply
3	CRR	Receive-PLL fast-lockup circuit resistor and capacitor connection
4	AOR	Receive-PLL LPF, n-channel MOS transistor output
5	AIR	Receive-PLL LPF, n-channel MOS transistor input
6	PDR1	Receive-PLL phase detector main tristate output
7	PDR2	Receive-PLL phase detector secondary tristate output
8	TEST	Test input
9	XIN	Reference oscillator input
10	NC	No connection
11	$\overline{\text{LDR}}$	Receive-PLL unlock detector n-channel, open-drain output
12	$\overline{\text{LDT}}$	Transmit-PLL unlock detector n-channel, open-drain output
13	DI	Serial data input
14	CL	Clock input
15	CE	Chip enable input
16	VBB	Gate reverse-bias capacitor connection

Number	Name	Description
17	PDT2	Transmit-PLL phase detector secondary tristate output
18	PDT1	Transmit-PLL phase detector main tristate output
19	AIT	Transmit-PLL LPF, n-channel MOS transistor input
20	AOT	Transmit-PLL LPF, n-channel MOS transistor output
21	CRT	Transmit-PLL fast-lockup circuit resistor and capacitor connection
22	TVDD	Transmit-PLL 2.8 to 4.5 V supply
23	PIT	Transmit-PLL local-oscillator input
24	VSS	Ground

SPECIFICATIONS

Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Receive-PLL supply voltage range	RV_{DD}	−0.3 to 5.5	V
Transmit-PLL supply voltage range	TV_{DD}	−0.3 to 5.5	V
Gate reverse-bias voltage range	V_{BB}	−4 to −1	V
XIN, TEST, PIR, PIT, AIR, AIT, CE, CL, DI, CRR and CRT input voltage range	V_I	−0.3 to 6.0	V
AOR, AOT, $\overline{LDR}$, $\overline{LDT}$, PDR1, PDR2, PDT1, PDT2, CRR and CRT output voltage range	V_O	−0.3 to 6.0	V
AOR, AOT, $\overline{LDR}$ and $\overline{LDT}$ output current range	I_O	0 to 2	mA
Power dissipation	P_D	350	mW
Operating temperature range	Topr	−20 to 75	°C
Storage temperature range	T_{stg}	−55 to 125	°C

Recommended Operating Conditions

T_a = 25 °C

Parameter	Symbol	Rating	Unit
Receive-PLL supply voltage range	RV_{DD}	2.8 to 4.5	V
Transmit-PLL supply voltage range	TV_{DD}	2.8 to 4.5	V

Electrical Characteristics

$V_{DD} = RV_{DD} = TV_{DD}$ = 2.8 to 4.5 V, V_{SS} = 0 V, T_a = 25 °C unless otherwise noted

Parameter	Symbol	Condition	Rating min	Rating typ	Rating max	Unit
RVDD supply current	I_{DD1}	LM7007M. See note 1.	–	17	22	mA
		LM7007HM. See note 1.	–	20	25	
RVDD + TVDD supply current	I_{DD2}	LM7007M. See note 2.	–	30	39	mA
		LM7007MH. See note 2.	–	37	45	
CE, CL, DI, CRR and CRT LOW-level input voltage	V_{IL}		0	–	0.4	V

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
CE, CL, DI, CRR and CRT HIGH-level input voltage	V_{IH}		2.0	–	5.5	V
XIN rms input voltage	V_{I1}	Sinewave, capacitive coupling, f_I = 5 to 23 MHz	50	–	1000	mV
PIR and PIT rms input voltage	V_{I2}	Sinewave, capacitive coupling, f_I = 200 to 400 MHz	70	–	500	mV
		Sinewave, capacitive coupling, V_{DD} = 2.8 to 3.3 V, f_I = 200 to 520 MHz	100	–	500	
PDR1 and PDT1 LOW-level output voltage	V_{OL1}	I_O = 0.1 mA	–	–	0.3	V
PDR2 and PDT2 LOW-level output voltage	V_{OL2}	I_O = 5 mA	–	–	1.5	V
$\overline{LDR}$ and $\overline{LDT}$ LOW-level output voltage	V_{OL3}	I_O = 1 mA	–	–	1	V
CRR and CRT LOW-level output voltage	V_{OL4}	I_O = 2 mA, V_{DD} = 3 V	0.7	1.0	1.4	V
AOR and AOT LOW-level output voltage	V_{OL5}	I_O = 0.5 mA, V_{AIR} = V_{AIT} = 1.2 V	–	–	0.5	V
		I_O = 1 mA, V_{AIR} = V_{AIT} = 1.3 V	–	–	0.5	
PDR1 and PDT1 HIGH-level output voltage	V_{OH1}	I_O = 0.1 mA	$0.6V_{DD}$	–	–	V
PDR2 and PDT2 HIGH-level output voltage	V_{OH2}	I_O = 0.1 mA	$0.6V_{DD}$	–	–	V
		I_O = 5 mA	$0.1V_{DD}$	–	–	
AOR, AOT, $\overline{LDR}$, $\overline{LDT}$, CRR and CRT output voltage	V_O		0	–	5.5	V
CE, CL, DI, CRR and CRT LOW-level input current	I_{IL1}	V_I = 0 V	–	–	5	µA
XIN LOW-level input current	I_{IL2}	V_I = 0 V	1	–	6	µA
PIR and PIT LOW-level input current	I_{IL3}	V_I = 0 V	2	–	12	µA
AIR and AIT LOW-level input current	I_{IL4}	V_I = 0 V	–	0.01	10.0	nA
TEST LOW-level input current	I_{IL5}	V_I = 0 V	–	–	5	µA
CE, CL, DI, CRR and CRT HIGH-level input current	I_{IH1}	V_I = 4.5 V	–	–	5	µA
XIN HIGH-level input current	I_{IH2}	V_I = 4.5 V	1	–	6	µA
PIR and PIT HIGH-level input current	I_{IH3}	V_I = 4.5 V	2	–	12	µA
AIR and AIT HIGH-level input current	I_{IH4}	V_I = 4.5 V	–	0.01	10.0	nA
TEST HIGH-level input current	I_{IH5}	V_I = 4.5 V	–	225	–	µA
$\overline{LDR}$, $\overline{LDT}$, CRR and CRT output leakage current	I_{OFF1}	V_O = 4.5 V	–	–	5	µA
AOR and AOT output leakage current	I_{OFF2}	V_O = 4.5 V	–	–	10	µA
PDR1, PDT1, PDR2 and PDT2 output leakage current	I_{OFF3}	V_O = 0.4 V or 4.5 V	–	0.01	10.0	nA

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
XIN input frequency	f_{I1}	Sinewave, capacitive coupling, V_I = 50 mV	6	–	23	MHz
PIR and PIT input frequency	f_{I2}	Sinewave, capacitive coupling, V_I = 70 mV	200	–	400	MHz
		Sinewave, capacitive coupling, V_{DD} = 2.8 to 3.2 V, V_I = 100 mV	200	–	520	
XIN feedback resistance	R_{f1}	V_{DD} = 4.5 V	750	1000	4500	kΩ
PIR and PIT feedback resistance	R_{f2}	V_{DD} = 4.5 V	375	500	2250	kΩ
TEST pull-down resistance	R_D		–	20	–	kΩ
XIN, PIR and PIT input capacitance	C_I		–	2.5	–	pF

Notes

1. f_{XIN} = 12.8 MHz, V_{PIR} = 70 mV at 400 MHz, all other inputs = 0 V, all outputs open
2. f_{XIN} = 12.8 MHz, V_{PIR} = V_{PIT} = 70 mV at 400 MHz, all other inputs = 0 V, all outputs open

FUNCTIONAL DESCRIPTION

C²B Data Format

The C²B input data format is shown in figure 1, and the input timing, in figure 2. The input data comprises 48 bits input serially on DI. TD0 is the first bit received.

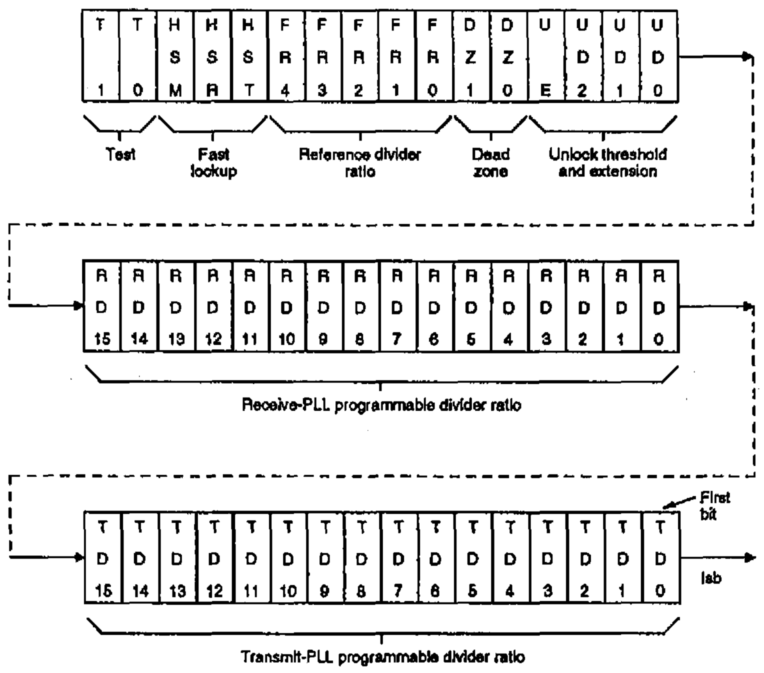


Figure 1. C²B data format

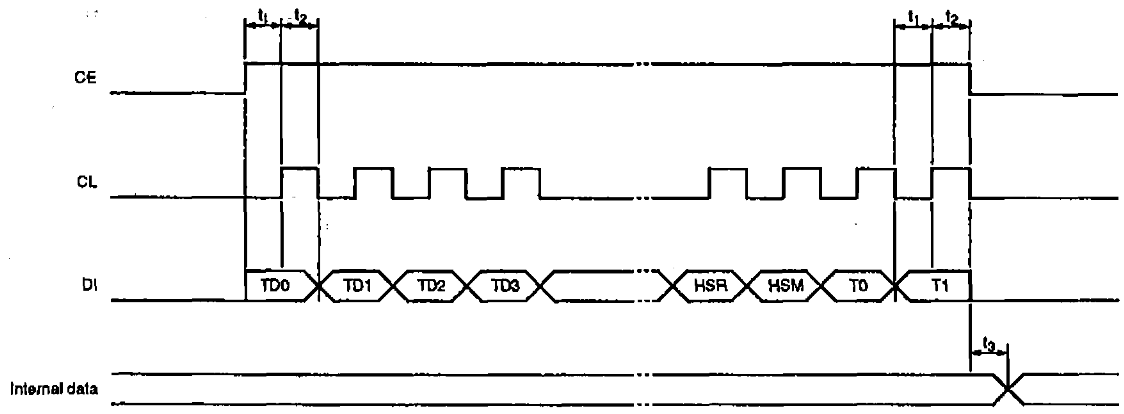


Figure 2. Serial data timing

The timing diagram parameters t_i (t_1, t_2 and t_3) should all be greater than $32/f_{XIN}$, where f_{XIN} is the XIN TCXO frequency. For TCXO frequencies of 10.625, 12.8 and 21.25 MHz, t_i should be greater than 3.02, 2.5 and 1.52 μs, respectively.

The outputs are undefined until the frequency synthesizer is programmed. The serial data should be input only after RVDD and f_{XIN} have become stable. Note that CE, CL and DI HIGH-level and LOW-level voltages are independent of RVDD.

Reference Divider

Data bits FR0 to FR4 set the reference frequency divider ratio. The standard temperature-compensated crystal oscillator (TXCO) input frequencies, f_{XIN}, are 12.8, 10.625 and 21.25 MHz.

The reference divider ratios for f_{ref} = 6.25 kHz with 12.5 kHz channel spacing for f_{XIN} are shown in table 1.

Table 1. Reference divider ratios

f_{XIN} (MHz)	FR4	FR3	FR2	FR1	FR0	Divider ratio
12.8	0	0	0	0	0	2048
10.625	1	1	1	1	1	1700
21.25	0	0	1	1	1	3400

Transmit- and Receive-PLL Programmable Dividers

Data bits TD0 to TD15 and RD0 to RD15 set the transmit- and receive-PLL programmable divider ratios, respectively. Bits TD0 and RD0 are the least significant bits.

The allowable divider ratios are in the range 256 to 65535. The PLL frequency divisions are two times the division setting of f_{OSC}/12.5 kHz.

Phase Detector

The phase detector output states of PDT1 (PDR1) are shown in table 2. When the PLL unlocks, $\overline{\text{LDT}}$ ($\overline{\text{LDR}}$) is pulled down and PDT2 (PDR2) has the same output state as PDT1 (PDR1).

Table 2. Phase detector output states

Condition		PDT1 (PDR1)
$f_{IN}/N_T > f_{ref}$	Leading	HIGH
$f_{IN}/N_T < f_{ref}$	Lagging	LOW
$f_{IN}/N_T = f_{ref}$	Coincidence	High impedance

Unlock-detector Threshold

Data bits UD0 to UD2 determine the unlock-detector threshold. The PLL unlock-detector output, $\overline{\text{LDT}}$ ($\overline{\text{LDR}}$), is pulled LOW when the phase error between the reference and the divided input, ϕ_E, exceeds the threshold. The threshold values for the standard frequencies are shown in table 3.

Table 3. Unlock-detector thresholds

UD2	UD1	UD0	Phase-error threshold (μs)		
			f_{XIN} = 12.8 MHz	f_{XIN} = 10.625 MHz	f_{XIN} = 21.25 MHz
0	0	0	0	0	0
0	0	1	0.15	0.19	0.09
0	1	0	0.3	Illegal	0.19

Table 3. Unlock-detector thresholds—continued

UD2	UD1	UD0	Phase-error threshold (μs)		
			f_{XIN} = 12.8 MHz	f_{XIN} = 10.625 MHz	f_{XIN} = 21.25 MHz
0	1	1	Illegal	Illegal	Illegal
1	0	0	1.25	0.94 ±0.19	0.94 ±0.19
1	0	1	1.25	0.94 ±0.19	0.94 ±0.19
1	1	0	5	4.70 ±0.94	4.70 ±0.94
1	1	1	5	4.70 ±0.94	4.70 ±0.94

Unlock Extension

Data bit UE selects the unlock extension period. The period is extended by 2.5 ms, when UE = 0, and by 5 ms, when UE = 1, as shown in figure 3. The unlock extension is ignored when UD0 = UD1 = UD2 = 0.

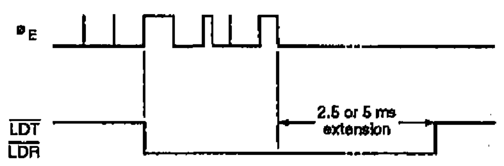


Figure 3. Unlock extension

Dead-zone Mode

Data bits DZ0 and DZ1 select the phase-insensitive bandwidth, or dead zone, of the PLL phase comparator as shown in table 4. Modes DZB, DZC and DZD have successively larger dead zones.

Table 4. Dead-zone modes

DZ1	DZ0	Dead-zone mode
0	0	Illegal
0	1	DZB
1	0	DZC
1	1	DZD

Fast-lockup Control

Data bits HST and HSR select fast-lockup mode for the transmit and receive PLLs, respectively. Fast-lockup mode is selected when each data bit is 1, and deselected, when 0.

Data bit HSM selects the fast-lockup operating mode as shown in figure 4. Fast-lockup operates continuously, when HSM = 1, and during unlock only, when HSM = 0.

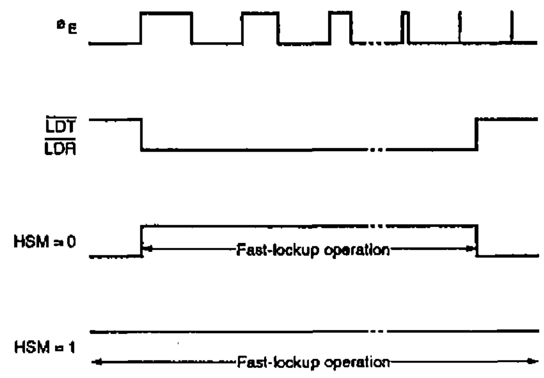


Figure 4. Fast-lockup operating modes

When fast lockup is not selected, CRT and CRR should be either open or tied to ground.

Power Supply

TVDD supplies the transmit-PLL programmable divider, phase detector, unlock detector and fast-lockup circuits. RVDD supplies the C²B interface, reference divider and receive-PLL circuits.

LPF Transistors

Open-drain transistors are provided for the transmit- and receive-PLL loop filters.

Test Mode (T0, T1)

Data bits T0 and T1 are normally not used and should be set to 0. Also, TEST should be open or tied to ground.

DESIGN INFORMATION

Dual Charge Pump and Fast-lockup Circuit

The dual charge pump and fast-lockup circuit is shown in figure 5. The phase detector secondary output goes active after a channel change causes the PLL to unlock. R1 becomes R1M||R1S, reducing the LPF time constant and decreasing the PLL lock time.

When the PLL locks, the phase detector secondary output becomes high impedance and R1 becomes R1M, thereby increasing the LPF time constant and improving sideband and FM response.

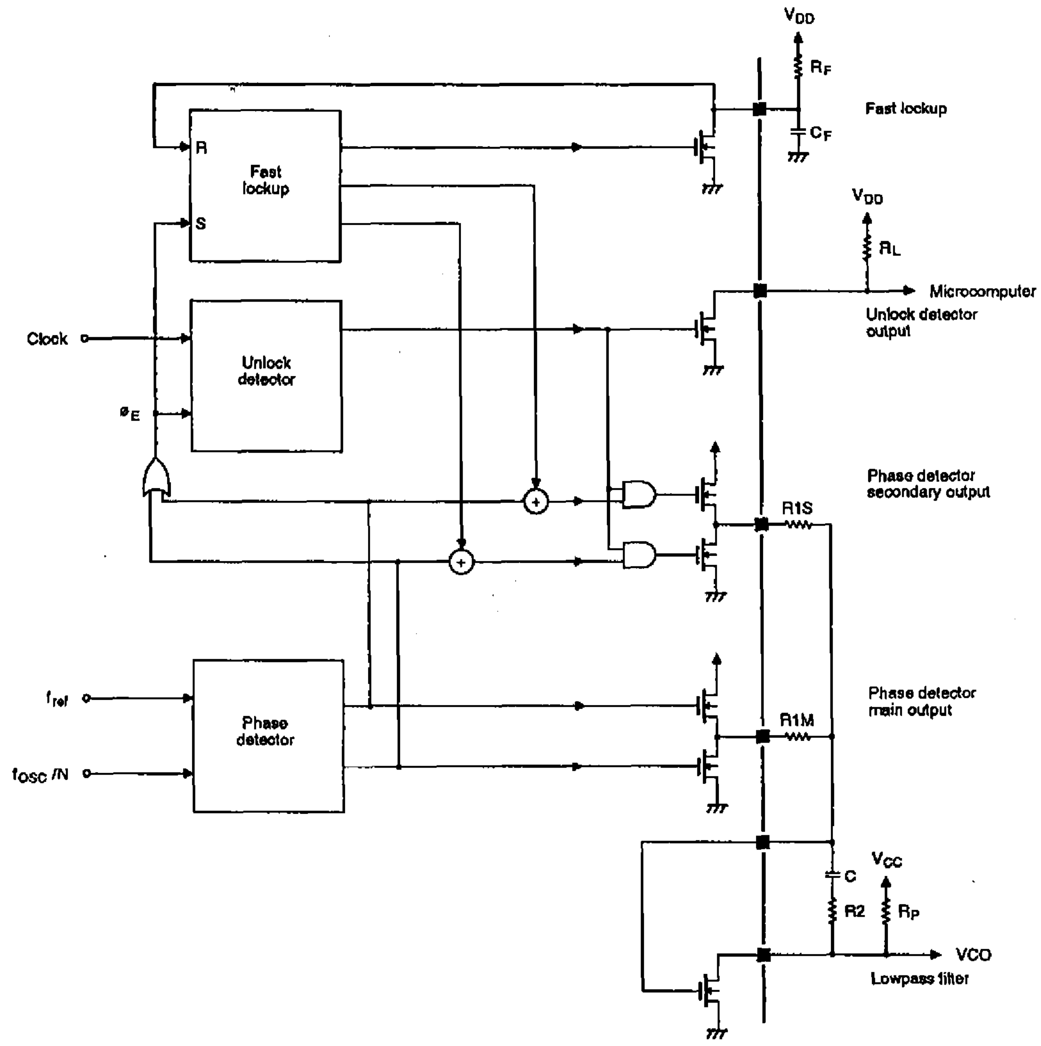


Figure 5. Dual charge pump and fast-lockup circuit

Phase-error Threshold

The phase-error threshold should be small during channel change to ensure precise phase-error checking and phase-detector secondary output operation. Unlocking caused by phase error is unlikely during FM operation. The phase-error threshold should be large after the PLL locks.

Gate Reverse Bias

A 0.01 µF capacitor should be connected between VBB and ground for the gate reverse bias.

TYPICAL APPLICATION