

SNVS317-FEBRUARY 2005

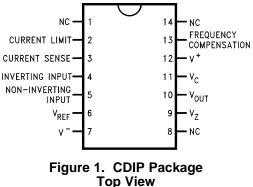
LM723JAN Voltage Regulator

Check for Samples: LM723JAN

FEATURES

- 150 mA Output Current without External Pass
 Transistor
- Output Currents in Excess of 10A Possible by Adding External Transistors
- Input Voltage 40V Max
- Output Voltage Adjustable from 2V to 37V
- Can be Used as Either a Linear or a Switching Regulator

Connection Diagram



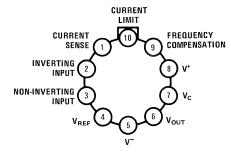
Top View See Package J0014A

Equivalent Circuit

DESCRIPTION

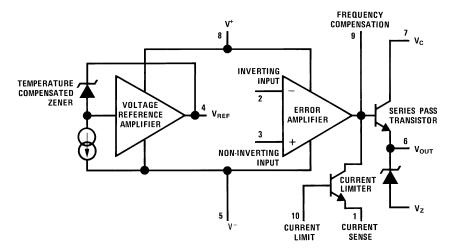
The LM723 is a voltage regulator designed primarily for series regulator applications. By itself, it will supply output currents up to 150 mA; but external transistors can be added to provide any desired load current. The circuit features extremely low standby current drain, and provision is made for either linear or foldback current limiting.

The LM723 is also useful in a wide range of other applications such as a shunt regulator, a current regulator or a temperature controller.



NOTE: Pin 5 connected to case.

Figure 2. Metal Can Package Top View See Package LME0010C



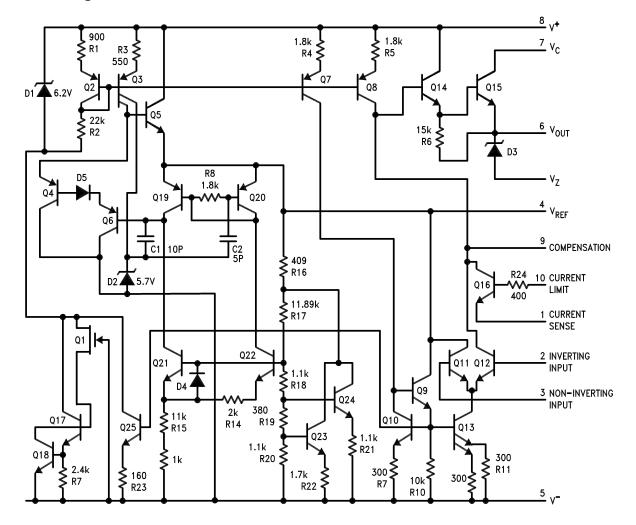
Pin numbers refer to metal can package.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet. All trademarks are the property of their respective owners. SNVS317-FEBRUARY 2005



www.ti.com

Schematic Diagram





These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings⁽¹⁾

Pulse Voltage from V ⁺ to V ⁻ (50 ms)		50V
Continuous Voltage from V ⁺ to V ⁻		40V
Input-Output Voltage Differential		40V
Differential Input Voltage		±5V
Voltage between non-inverting input and V	+8V	
Current from V _Z	25 mA	
Current from V _{REF}	15 mA	
Internal Power Dissipation ($T_A = 125^{\circ}C$)	Metal Can ⁽²⁾	300 mW
	CDIP ⁽²⁾	400 mW
Maximum T _J	+175°C	
Storage Temperature Range		-65°C ≤ T _A ≤ +150°C
Lead Temperature (Soldering, 4 sec. max.)		300°C
Thermal Resistance		
θ _{JA}	CDIP (Still Air)	100°C/W
	CDIP (500LF/ Min Air flow)	61°C/W
	Metal Can (Still Air)	156°C/W
	Metal Can (500LF/ Min Air flow)	89°C/W
θ _{JC}	CDIP	22°C/W
	Metal Can	37°C/W
ESD Tolerance ⁽³⁾	·	1200V

(1) "Absolute Maximum Ratings" indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not ensure specific performance limits. For ensured specifications and test conditions, see the Electrical Characteristics. The ensured specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

(2) The maximum power dissipation for these devices must be derated at elevated temperatures and is dictated by T_{JMAX}, θ_{JA}, and the ambient temperature, T_A. The maximum available power dissipation at any temperature is P_d = (T_{JMAX} - T_A)/θ_{JA} or the number given in the Absolute Maximum Ratings, whichever is less. See derating curves for maximum power rating above 25°C.

(3) Human body model, 1.5 k Ω in series with 100 pF.

Recommended Operating Conditions

Input Voltage Range	9.5V to 40V _{DC}
Output Voltage Range	2V to 37V _{DC}
Input-Output Voltage Differential	2.5 V to 38V _{DC}
Ambient Operating Temperature Range	−55°C ≤ T _A ≤ +125°C

Quality Conformance Inspection

MIL-STD-883, Method 5004 and Method 5005

Subgroup	Description	Temp (°C)
1	Static tests at	+25
2	Static tests at	+125
3	Static tests at	-55
4	Dynamic tests at	+25
5	Dynamic tests at	+125
6	Dynamic tests at	-55
7	Functional tests at	+25
8A	Functional tests at	+125
8B	Functional tests at	-55

LM723JAN



SNVS317-FEBRUARY 2005

www.ti.com

Subgroup	Description	Temp (°C)
9	Switching tests at	+25
10	Switching tests at	+125
11	Switching tests at	-55

Electrical Characteristics

DC Parameters ⁽¹⁾

Symbol	Parameter	Conditions	Notes	Min	Мах	Units	Sub- groups
V _{Rline}	Line Regulation	$12V \le V_{IN} \le 15V, V_{OUT} = 5V,$		-0.1	0.1	%V _{OUT}	1
		$I_L = 1mA$		-0.2	0.2	%V _{OUT}	2
				-0.3	0.3	%V _{OUT}	3
		$\begin{array}{l} 12V \leq V_{\text{IN}} \leq 40V, \ V_{\text{OUT}} = 2V, \\ I_{\text{L}} = 1\text{mA} \end{array}$		-0.2	0.2	%V _{OUT}	1
		$9.5V \le V_{IN} \le 40V, V_{OUT} = 5V,$ $I_L = 1mA$		-0.3	0.3	%V _{OUT}	1
		$12V \le V_{IN} \le 15V, V_{OUT} = 5V,$ $I_L = 1mA$		-10. 0	+10. 0	mV	1
				-20. 0	+20. 0	mV	2
				-30. 0	+30. 0	mV	3
V _{Rload}	Load Regulation	$1mA \le I_L \le 50mA, V_{IN} = 12V, V_{OUT} = 5V$		-0.1 5	0.15	%V _{OUT}	1
				-0.4	0.4	%V _{OUT}	2
				-0.6	0.6	%V _{OUT}	3
		$1mA \le I_L \le 10mA, V_{IN} = 40V, \\ V_{OUT} = 37V$		-0.5	0.5	%V _{OUT}	1
		$\begin{array}{l} 6mA \leq I_L \leq 12mA, \ V_{IN} = 10V, \\ V_{OUT} = 7.5V \end{array}$		-0.2	0.2	%V _{OUT}	1
		$1mA \le I_L \le 50mA, V_{IN} = 12V, V_{OUT} = 5V$		-15. 0	+15. 0	mV	1
				-40. 0	+40. 0	mV	2
				-60. 0	+60. 0	mV	3
V_{REF}	Voltage Reference	$I_{REF} = 1mA, V_{IN} = 12V$		6.95	7.35	V	1
				6.9	7.4	V	2, 3
I _{SCD}	Standby Current	$V_{\rm IN} = 30V, \ I_{\rm L} = I_{\rm REF} = 0,$		0.5	3	mA	1
		$V_{OUT} = V_{REF}$		0.5	2.4	mA	2
				0.5	3.5	mA	3
I _{OS}	Short Circuit Current	$\label{eq:Vout} \begin{array}{l} V_{OUT}=5V, \ V_{IN}=12V, \\ R_{SC}=10\Omega, \ R_L=0 \end{array}$		45	85	mA	1
Vz	Zener Voltage	I _Z = 1mA		(2)(3) 5.58	6.82	V	1
V _{OUT}	Output Voltage	V _{IN} = 12V, V _{OUT} = 5V, I _L = 1mA	(4)	4.5	5.5	V	1, 2, 3

(1) Unless otherwise specified, $T_A = 25^{\circ}C$, $V_{IN} = V^+ = V_C = 12V$, $V^- = 0$, $V_{OUT} = 5V$, $I_L = 1$ mA, $R_{SC} = 0$, $C_1 = 100$ pF, $C_{REF} = 0$ and divider impedance as seen by error amplifier $\leq 10 \text{ k}\Omega$ connected as shown in Figure 14. Line and load regulation specifications are given for the condition of constant chip temperature. Temperature drifts must be taken into account separately for high dissipation conditions. For metal can applications where V_Z is required, an external 6.2V zener diode should be connected in series with V_{OUT} .

(2)

Tested for 14 – lead DIP only. (3)

(4) Setup test for Temp. Coeff.

4 Submit Documentation Feedback



Electrical Characteristics (continued)

DC Parameters (1)

Symbol	Parameter	Conditions	Notes	Min	Мах	Units	Sub- groups
Delta V _{OUT} / Delta T	Average Temperature Coefficient of Output Voltage	$25^{\circ}C \le T_A \le +125^{\circ}C, V_{IN} = 12V, V_{OUT} = 5V, I_L = 1mA$	(5)	-0.0 1	0.01	%/°C	8A
		-55° C ≤ T _A ≤ +25°C, V _{IN} = 12V, V _{OUT} = 5V, I _L = 1mA	(5)	-0.0 15	0.01 5	%/°C	8B
Delta V _{OUT} / Delta V _{IN}	Ripple Rejection	$ f = 10 \text{KHz}, C_{\text{REF}} = 0\text{F}, \\ V_{\text{INS}} = 2V_{\text{RMS}} $		64		dB	4
		$ f = 10 KHz, C_{REF} = 5 \mu F, \\ V_{INS} = 2 V_{RMS} $		76		dB	4
N _O	Output Noise Voltage	100Hz ≤ f ≤ 10KHz, V _{INS} = 0V _{RMS} , C _{REF} = 0µF			120	μV_{RMS}	4
		100Hz ≤ f ≤ 10KHz, V _{INS} = 0V _{RMS} , C _{REF} = 5µF			7	μV_{RMS}	4
Delta V _{OUT} / Delta V _{IN}	Line Transient Response	$ \begin{array}{l} V_{\text{IN}} = 12V, V_{\text{OUT}} = 5V, \\ I_{\text{L}} = 1\text{mA}, C_{\text{REF}} = 5\mu\text{F}, \\ R_{\text{SC}} = 0\Omega, \\ \text{Delta} V_{\text{IN}} = 3V \text{ for } 25\mu\text{sec} \end{array} $		0	10	mV/V	4
Delta V _{OUT} / Delta I _L	Load Transient Response	$ \begin{array}{l} V_{\text{IN}} = 12V, V_{\text{OUT}} = 5V, \\ I_{\text{L}} = 40\text{mA}, C_{\text{REF}} = 5\mu\text{F}, \\ R_{\text{SC}} = 0\Omega, \\ \text{Delta } I_{\text{L}} = 10\text{mA for } 25\mu\text{sec} \end{array} $		-1.5	0	mV/mA	4

(5) Calculated parameter

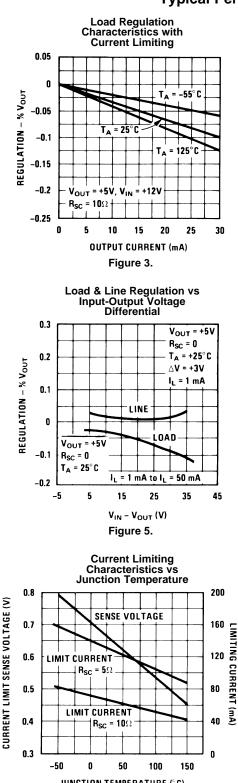
DC Parameters: Drift Values

Delta calculations performed on JAN S and QMLV devices at Group B, Subgroup 5, only.

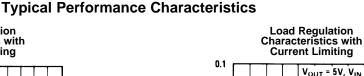
Symbol	Parameters	Conditions	Notes	Min	Max	Unit	Sub- groups
V _{Rline}	Line Regulation	$\begin{array}{l} 12V \leq V_{IN} \leq 15V, V_{OUT} = 5V, \\ I_L = 1mA, \pm 1mV, \text{or} \pm 15\% \\ (\text{whichever is greater}) \end{array}$		-1.0	1.0	mV	1
V _{Rload}	Load Regulation	$ \begin{array}{l} 1mA \leq I_L \leq 50mA, \ V_{IN} = 12V, \\ V_{OUT} = 5V, \ \pm 1mV, \ or \ \pm 20\% \\ (whichever is greater) \end{array} $			1.0	mV	1
V _{REF}	Reference Voltage	$I_{REF} = 1 \text{mA}, V_{IN} = 12 \text{V}$		-15	15	mV	1
I _{SCD}	Standby Current Drain	$V_{IN} = 30V, I_L = I_{REF} = 0,$ $V_{OUT} = V_{REF}$		-10	10	%	1

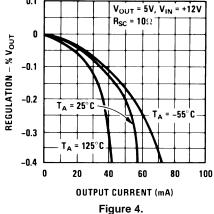


SNVS317-FEBRUARY 2005

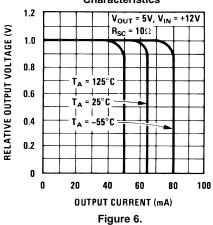


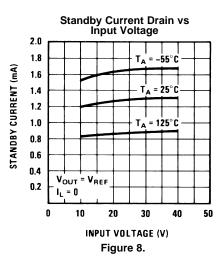






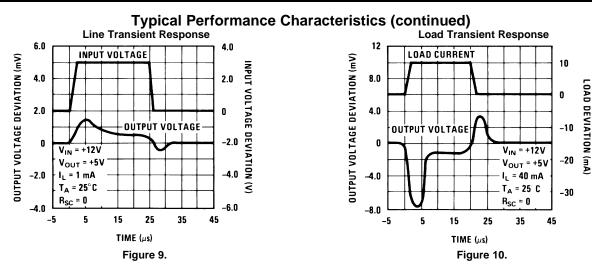
Current Limiting Characteristics



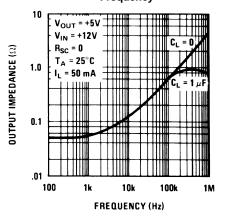


6



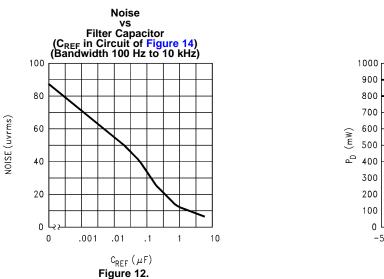


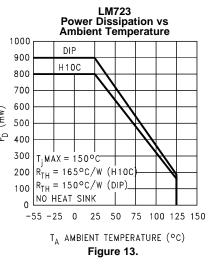
Output Impedence vs Frequency













SNVS317-FEBRUARY 2005

	Table 1. Resistor Values (kΩ) for Standard Output Voltage																																																	
Positive Output Voltage	Applicable Figures ⁽¹⁾		ked It ±5%	Ad	Output Adjustable ±10% ⁽²⁾		Adjustable		Adjustable		Adjustable		Adjustable		Adjustable		Adjustable		Adjustable		Adjustable		Adjustable		Adjustable		Adjustable		Adjustable		Adjustable		Adjustable		Adjustable		Adjustable		Adjustable		Adjustable		Adjustable Outp	Negative Output Voltage	Applicable Figures	Fixed Output ±5%		5% Output Adjustable ±10%		able
		R1	R2	R1	P1	R2			R1	R2	R1	P1	R2																																					
+3.0	Figure 14, Figure 18, Figure 19, Figure 22, Figure 25 (Figure 17)	4.12	3.01	1.8	0.5	1.2	+100	Figure 20	3.57	102	2.2	10	91																																					
+3.6	Figure 14, Figure 18, Figure 19, Figure 22, Figure 25 (Figure 17)	3.57	3.65	1.5	0.5	1.5	+250	Figure 20	3.57	255	2.2	10	240																																					
+5.0	Figure 14, Figure 18, Figure 19, Figure 22, Figure 25 (Figure 17)	2.15	4.99	0.75	0.5	2.2	-6 ⁽³⁾	Figure 16, (Figure 23)	3.57	2.43	1.2	0.5	0.75																																					
+6.0	Figure 14, Figure 18, Figure 19, Figure 22, Figure 25 (Figure 17)	1.15	6.04	0.5	0.5	2.7	-9	Figure 16, Figure 23	3.48	5.36	1.2	0.5	2.0																																					
+9.0	Figure 15, Figure 17, (Figure 18, Figure 19, Figure 22, Figure 25)	1.87	7.15	0.75	1.0	2.7	-12	Figure 16, Figure 23	3.57	8.45	1.2	0.5	3.3																																					
+12	Figure 15, Figure 17, (Figure 18, Figure 19, Figure 22, Figure 25)	4.87	7.15	2.0	1.0	3.0	-15	Figure 16, Figure 23	3.65	11.5	1.2	0.5	4.3																																					
+15	Figure 15, Figure 17, (Figure 18, Figure 19, Figure 22, Figure 25)	7.87	7.15	3.3	1.0	3.0	-28	Figure 16, Figure 23	3.57	24.3	1.2	0.5	10																																					
+28	Figure 15, Figure 17, (Figure 18, Figure 19, Figure 22, Figure 25)	21.0	7.15	5.6	1.0	2.0	-45	Figure 21	3.57	41.2	2.2	10	33																																					
+45	Figure 20	3.57	48.7	2.2	10	39	-100	Figure 21	3.57	97.6	2.2	10	91																																					
+75	Figure 20	3.57	78.7	2.2	10	68	-250	Figure 21	3.57	249	2.2	10	240																																					

Figures in parentheses may be used if R1/R2 divider is placed on opposite input of error amp. Replace R1/R2 in figures with divider shown in Figure 26. V⁺ and V_{CC} must be connected to a +3V or greater supply. (1)

(2) (3)

Table 2. Formulae for Intermediate Output Voltages

Outputs from +2 to +7 volts	Outputs from +4 to +250 volts	Current Limiting
(Figure 14, Figure 17, Figure 18, Figure 19, Figure 22, Figure 25)	(Figure 20)	
$V_{OUT} = \left(V_{REF} \times \frac{R2}{R1 + R2}\right)$	$V_{OUT} = \left(rac{V_{REF}}{2} imes rac{R2 - R1}{R1} ight); R3 = R4$	$I_{\text{LIMIT}} = \frac{V_{\text{SENSE}}}{R_{\text{SC}}}$
Outputs from +7 to +37 volts	Outputs from −6 to −250 volts	Foldback Current Limiting
(Figure 15, Figure 17, Figure 18, Figure 19, Figure 22, Figure 25)	(Figure 16, Figure 21, Figure 23)	$I_{\text{KNEE}} = \left(\frac{V_{\text{OUT}} \text{ R3}}{\text{R}_{\text{SC}} \text{ R4}} + \frac{V_{\text{SENSE}} (\text{R3} + \text{R4})}{\text{R}_{\text{SC}} \text{ R4}}\right)$
$V_{OUT} = \left(V_{REF} \times \frac{R1 + R2}{R2}\right)$	$V_{OUT} = \left(rac{V_{REF}}{2} imes rac{R1 + R2}{R1} ight); R3 = R4$	$I_{SHORT CKT} = \left(\frac{V_{SENSE}}{R_{SC}} \times \frac{R3 + R4}{R4}\right)$

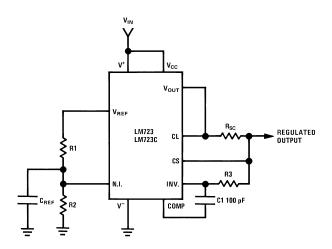
. ~



SNVS317-FEBRUARY 2005

www.ti.com

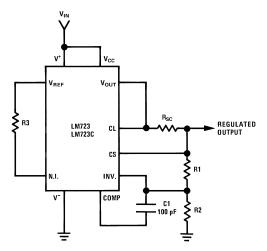
TYPICAL APPLICATIONS



Note: $R3 = \frac{R1R2}{R1 + R2}$ for minimum temperature drift

Figure 14. Basic Low Voltage Regulator (V_{OUT} = 2 to 7 Volts)

Typical Performance			
Regulated Output Voltage	5V		
Line Regulation ($\Delta V_{IN} = 3V$)	0.5mV		
Load Regulation ($\Delta I_L = 50 \text{ mA}$)	1.5mV		



R1 R2 Note: R3 = $\frac{R1 R2}{R1 + R2}$ for minimum temperature drift. R3 may be eliminated for minimum component count.

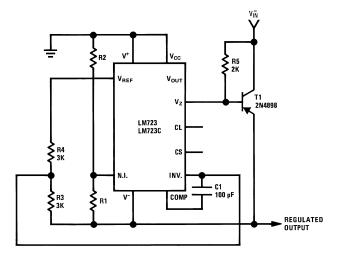
Figure 15. Basic High Voltage Regulator (V_{OUT} = 7 to 37 Volts)

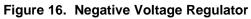
Typical Performance			
Regulated Output Voltage	15V		
Line Regulation ($\Delta V_{IN} = 3V$)	1.5 mV		
Load Regulation ($\Delta I_L = 50 \text{ mA}$)	4.5 mV		

SNVS317-FEBRUARY 2005

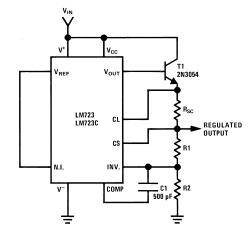


www.ti.com





Typical Performance		
Regulated Output Voltage	-15V	
Line Regulation ($\Delta V_{IN} = 3V$)	1 mV	
Load Regulation ($\Delta I_L = 100 \text{ mA}$)	2 mV	





Typical Performance	
Regulated Output Voltage	+15V
Line Regulation ($\Delta V_{IN} = 3V$)	1.5 mV
Load Regulation ($\Delta I_L = 1A$)	15 mV



SNVS317-FEBRUARY 2005

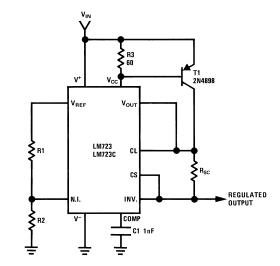
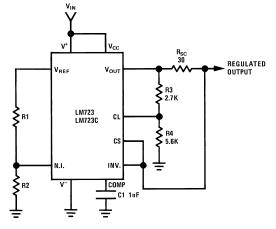
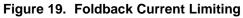


Figure 18. Positive Voltage Regulator (External PNP Pass Transistor)

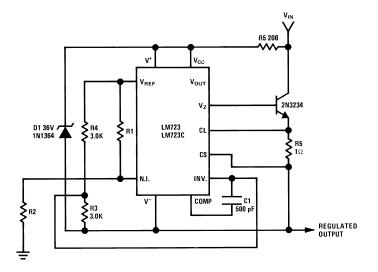
Typical Performance	
Regulated Output Voltage	+5V
Line Regulation ($\Delta V_{IN} = 3V$)	0.5 mV
Load Regulation ($\Delta I_L = 1A$)	5 mV





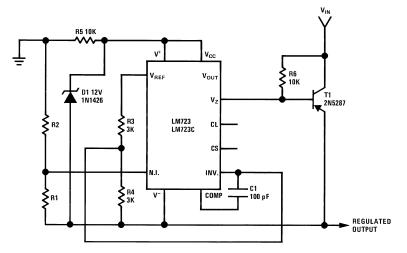
Typical Performance				
Regulated Output Voltage	+5V			
Line Regulation ($\Delta V_{IN} = 3V$)	0.5 mV			
Load Regulation ($\Delta I_L = 10 \text{ mA}$)	1 mV			
Short Circuit Current	20 mA			







Typical Performance					
Regulated Output Voltage	+50V				
Line Regulation ($\Delta V_{IN} = 20V$)	15 mV				
Load Regulation ($\Delta I_L = 50 \text{ mA}$)	20 mV				

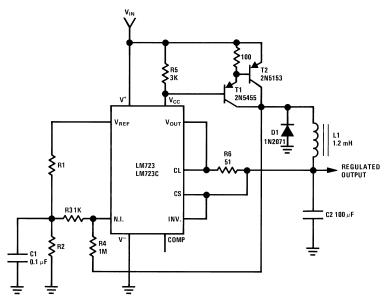




Typical Performance	
Regulated Output Voltage	-100V
Line Regulation ($\Delta V_{IN} = 20V$)	30 mV
Load Regulation ($\Delta I_L = 100 \text{ mA}$)	20 mV



SNVS317-FEBRUARY 2005



 L_1 is 40 turns of No. 20 enameled copper wire wound on Ferroxcube P36/22-3B7 pot core or equivalent with 0.009 in. air gap.

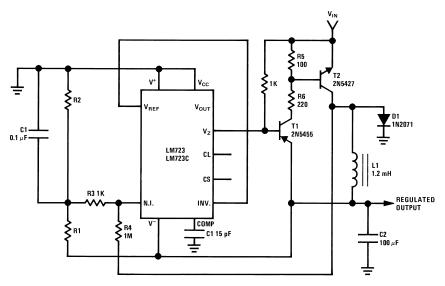
Figure 22. Positive Switching Regulator

Typical Performance				
Regulated Output Voltage	+5V			
Line Regulation ($\Delta V_{IN} = 30V$)	10 mV			
Load Regulation ($\Delta I_L = 2A$)	80 mV			

SNVS317-FEBRUARY 2005



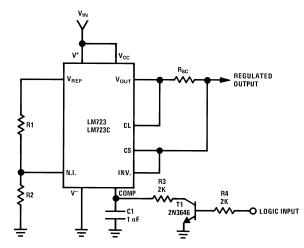
www.ti.com



 L_1 is 40 turns of No. 20 enameled copper wire wound on Ferroxcube P36/22-3B7 pot core or equivalent with 0.009 in. air gap.

Figure 23. Negative Switching Regulator

Typical Performance	
Regulated Output Voltage	-15V
Line Regulation ($\Delta V_{IN} = 20V$)	8 mV
Load Regulation ($\Delta I_L = 2A$)	6 mV



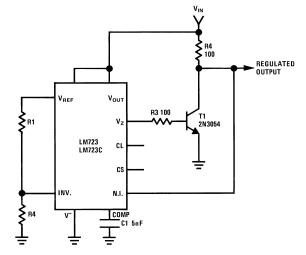
Note: Current limit transistor may be used for shutdown if current limiting is not required.

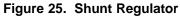
Figure 24. Remote Shutdown Regulator with Current Limiting

Typical Performance	
Regulated Output Voltage	+5V
Line Regulation ($\Delta V_{IN} = 3V$)	0.5 mV
Load Regulation ($\Delta I_L = 50 \text{ mA}$)	1.5 mV

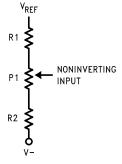


SNVS317-FEBRUARY 2005





Regulated Output Voltage	+5V
Line Regulation ($\Delta V_{IN} = 10V$)	0.5 mV
Load Regulation ($\Delta I_L = 100 \text{ mA}$)	1.5 mV



NOTE: Replace R1/R2 in figures with divider shown in Figure 26

Figure 26. Output Voltage Adjust

TEXAS INSTRUMENTS

www.ti.com

SNVS317-FEBRUARY 2005

REVISION HISTORY SECTION

Date Released	Revision	Section	Originator	Changes
02/15/05	A	New Release, Corporate format		1 MDS data sheet converted into one Corp. data sheet format. MJLM723-X, Rev. 1A0. MDS data sheet will be archived.



PACKAGING INFORMATION

Orderable Device	Status	Package Type	Package	Pins	Package Qty	Eco Plan	Lead/Ball Finish	MSL Peak Temp	Op Temp (°C)	Top-Side Markings	Samples
	(1)		Drawing			(2)		(3)		(4)	
JL723SCA	ACTIVE	CDIP	J	14	25	TBD	Call TI	Call TI	-55 to 125	JL723SCA JM38510/10201SCA Q	Samples
JL723SIA	ACTIVE	TO-100	LME	10	20	TBD	Call TI	Call TI	-55 to 125	JL723SIA JM38510/10201SIA Q ACO JM38510/10201SIA Q >T	Samples
JM38510/10201SCA	ACTIVE	CDIP	J	14	25	TBD	Call TI	Call TI	-55 to 125	JL723SCA JM38510/10201SCA Q	Samples
JM38510/10201SIA	ACTIVE	TO-100	LME	10	20	TBD	Call TI	Call TI	-55 to 125	JL723SIA JM38510/10201SIA Q ACO JM38510/10201SIA Q >T	Samples
M38510/10201SCA	ACTIVE	CDIP	J	14	25	TBD	Call TI	Call TI	-55 to 125	JL723SCA JM38510/10201SCA Q	Samples
M38510/10201SIA	ACTIVE	TO-100	LME	10	20	TBD	Call TI	Call TI	-55 to 125	JL723SIA JM38510/10201SIA Q ACO JM38510/10201SIA Q >T	Samples

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes. **Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

⁽⁴⁾ Only one of markings shown within the brackets will appear on the physical device.



9-Mar-2013

Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

J (R-GDIP-T**) 14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE

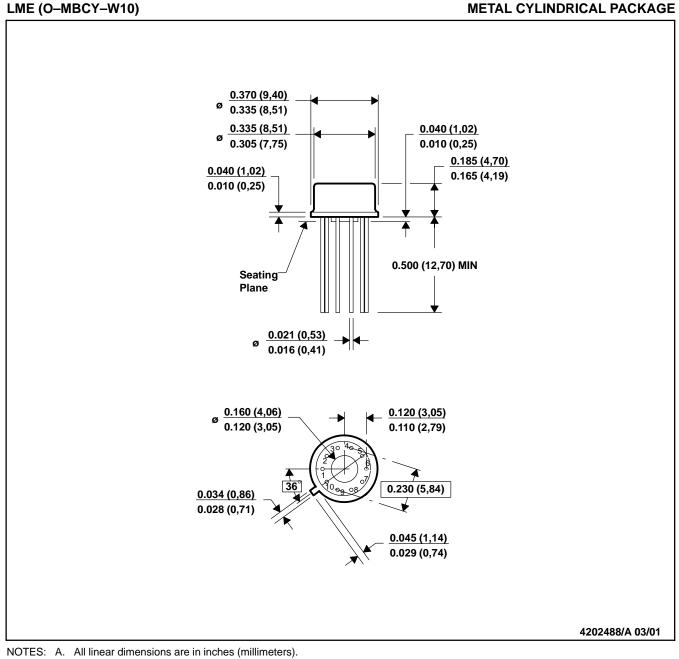


NOTES: A. All linear dimensions are in inches (millimeters).

- B. This drawing is subject to change without notice.
- C. This package is hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
- E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

MECHANICAL DATA

MMBC006 - MARCH 2001



- B. This drawing is subject to change without notice.
- C. Leads in true position within 0.010 (0,25) R @ MMC at seating plane.
- D. Pin numbers shown for reference only. Numbers may not be marked on package.
- E. Falls within JEDEC MO-006/TO-100.



IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as "components") are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI's terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers' products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers' products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI's goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or "enhanced plastic" are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have *not* been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Products		Applications	
Audio	www.ti.com/audio	Automotive and Transportation	www.ti.com/automotive
Amplifiers	amplifier.ti.com	Communications and Telecom	www.ti.com/communications
Data Converters	dataconverter.ti.com	Computers and Peripherals	www.ti.com/computers
DLP® Products	www.dlp.com	Consumer Electronics	www.ti.com/consumer-apps
DSP	dsp.ti.com	Energy and Lighting	www.ti.com/energy
Clocks and Timers	www.ti.com/clocks	Industrial	www.ti.com/industrial
Interface	interface.ti.com	Medical	www.ti.com/medical
Logic	logic.ti.com	Security	www.ti.com/security
Power Mgmt	power.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
RFID	www.ti-rfid.com		
OMAP Applications Processors	www.ti.com/omap	TI E2E Community	e2e.ti.com
Wireless Connectivity	www.ti.com/wirelessconne	ectivity	

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265 Copyright © 2013, Texas Instruments Incorporated