National Semiconductor

LMC567 Low Power Tone Decoder

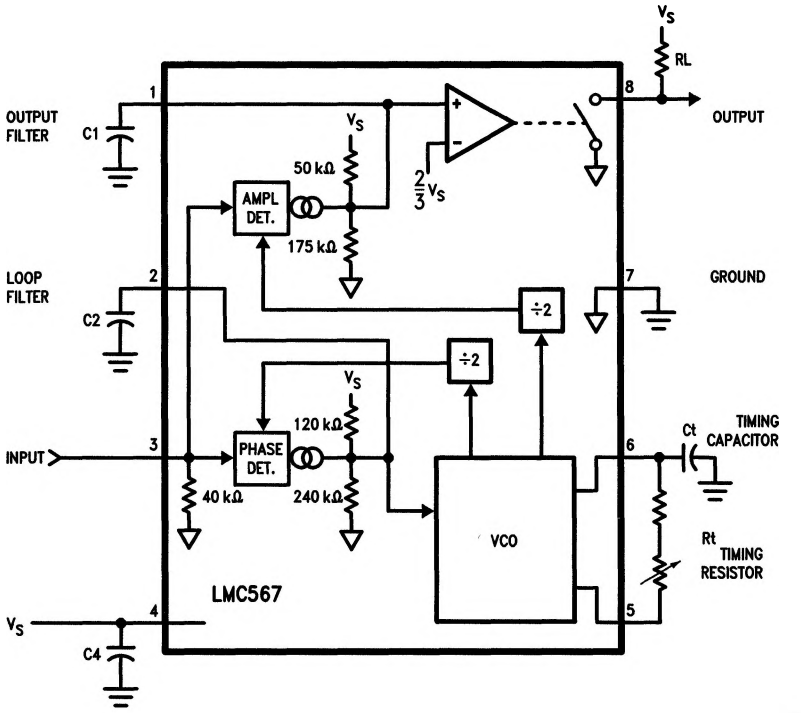
General Description

The LMC567 is a low power general purpose LMCMOS™ tone decoder which is functionally similar to the industry standard LM567. It consists of a twice frequency voltage-controlled oscillator (VCO) and quadrature dividers which establish the reference signals for phase and amplitude detectors. The phase detector and VCO form a phase-locked loop (PLL) which locks to an input signal frequency which is within the control range of the VCO. When the PLL is locked and the input signal amplitude exceeds an internally pre-set threshold, a switch to ground is activated on the output pin. External components set up the oscillator to run at twice the input frequency and determine the phase and amplitude filter time constants.

Features

- Functionally similar to LM567
- 2V to 9V supply voltage range
- Low supply current drain
- No increase in current with output activated
- Operates to 500 kHz input frequency
- High oscillator stability
- Ground-referenced input
- Hysteresis added to amplitude comparator
- Out-of-band signals and noise rejected
- 20 mA output current capability

Block Diagram (with External Components)



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Order Number LMC567CM or LMC567CN
See NS Package Number M08A or N08E

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Input Voltage, Pin 3	2 V_{p-p}
Supply Voltage, Pin 4	10V
Output Voltage, Pin 8	13V
Voltage at All Other Pins	Vs to Gnd
Output Current, Pin 8	30 mA
Package Dissipation	500 mW
Operating Temperature Range (T_A)	−25°C to +125°C
Storage Temperature Range	−55°C to +150°C
Soldering Information	
Dual-In-Line Package	
Soldering (10 sec.)	260°C
Small Outline Package	
Vapor Phase (60 sec.)	215°C
Infrared (15 sec.)	220°C

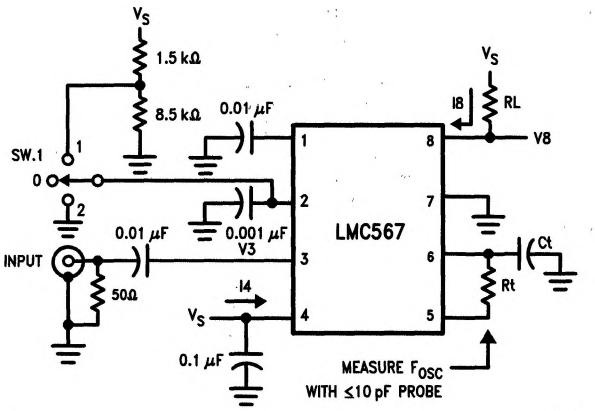
See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

Electrical Characteristics

Test Circuit, T_A = 25°C, V_s = 5V, RtCt #2, Sw. 1 Pos. 0, and no input, unless otherwise noted.

Symbol	Parameter	Conditions		Min	Typ	Max	Units
I4	Power Supply Current	RtCt #1, Quiescent or Activated	V_s = 2V		0.3		mAdc
			V_s = 5V		0.5	0.8	
			V_s = 9V		0.8	1.3	
V3	Input D.C. Bias				0		mVdc
R3	Input Resistance				40		kΩ
I8	Output Leakage				1	100	nAdc
f_0	Center Frequency, $F_{osc} \div 2$	RtCt #2, Measure Oscillator Frequency and Divide by 2	V_s = 2V		98		kHz
			V_s = 5V	92	103	113	
			V_s = 9V		105		
Δf_0	Center Frequency Shift with Supply	$\frac{f_0\|_{9V} - f_0\|_{2V}}{7\, f_0\|_{5V}} \times 100$			1.0	2.0	%/V
V_{in}	Input Threshold	Set Input Frequency Equal to f_0 Measured Above, Increase Input Level Until Pin 8 Goes Low.	V_s = 2V	11	20	27	mVrms
			V_s = 5V	17	30	45	
			V_s = 9V		45		
ΔV_{in}	Input Hysteresis	Starting at Input Threshold, Decrease Input Level Until Pin 8 goes High.			1.5		mVrms
V8	Output 'Sat' Voltage	Input Level > Threshold Choose RL for Specified I8	I8 = 2 mA		0.06	0.15	Vdc
			I8 = 20 mA		0.7		
L.D.B.W.	Largest Detection Bandwidth	Measure F_{osc} with Sw. 1 in Pos. 0, 1, and 2; L.D.B.W = $\frac{F_{osc}\|_{P2} - F_{osc}\|_{P1}}{F_{osc}\|_{P0}} \times 100$	V_s = 2V	7	11	15	%
			V_s = 5V	11	14	17	
			V_s = 9V		15		
ΔBW	Bandwidth Skew	Skew = $\left(\frac{F_{osc}\|_{P2} + F_{osc}\|_{P1}}{2\, F_{osc}\|_{P0}} - 1\right) \times 100$			0	±1.0	%
f_{max}	Highest Center Freq.	RtCt #3, Measure Oscillator Frequency and Divide by 2			700		kHz
V_{in}	Input Threshold at f_{max}	Set Input Frequency Equal to f_{max} measured Above, Increase Input Level Until Pin 8 goes Low.			35		mVrms

Test Circuit



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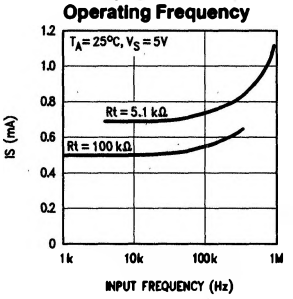
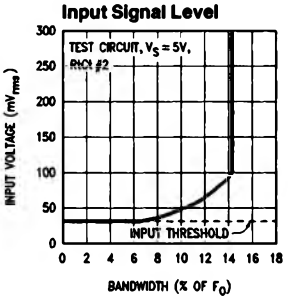
RtCt	Rt	Ct
#1	100k	300 pF
#2	10k	300 pF
#3	5.1k	62 pF

Typical Performance Characteristics

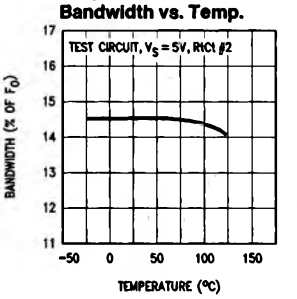
Supply Current vs. Operating Frequency



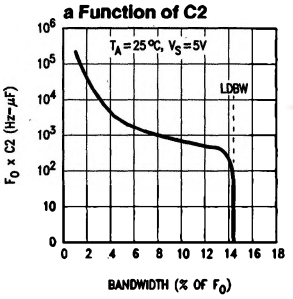
Bandwidth vs. Input Signal Level



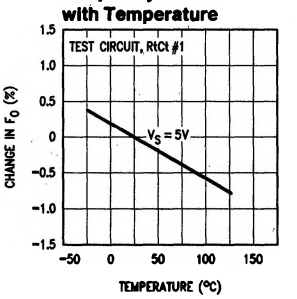
Largest Detection Bandwidth vs. Temp.



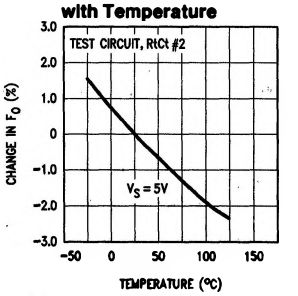
Bandwidth as a Function of C2



Frequency Drift with Temperature



Frequency Drift with Temperature



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Applications Information (refer to Block Diagram)

GENERAL

The LMC567 low power tone decoder can be operated at supply voltages of 2V to 9V and at input frequencies ranging from 1 Hz up to 500 kHz.

The LMC567 can be directly substituted in most LM567 applications with the following provisions:

1. Oscillator timing capacitor Ct must be halved to double the oscillator frequency relative to the input frequency (See OSCILLATOR TIMING COMPONENTS).
2. Filter capacitors C1 and C2 must be reduced by a factor of 8 to maintain the same filter time constants.
3. The output current demanded of pin 8 must be limited to the specified capability of the LMC567.

OSCILLATOR TIMING COMPONENTS

The voltage-controlled oscillator (VCO) on the LMC567 must be set up to run at twice the frequency of the input signal tone to be decoded. The center frequency of the VCO is set by timing resistor Rt and timing capacitor Ct connected to pins 5 and 6 of the IC. The center frequency as a function of Rt and Ct is given by:

$$F_{osc} \cong \frac{1}{1.4\ Rt\ Ct}\ Hz$$

Since this will cause an input tone of half F_{osc} to be decoded,

$$F_{input} \cong \frac{1}{2.8\ Rt\ Ct}\ Hz$$

This equation is accurate at low frequencies; however, above 50 kHz (F_{osc} = 100 kHz), internal delays cause the actual frequency to be lower than predicted.

The choice of Rt and Ct will be a tradeoff between supply current and practical capacitor values. An additional supply current component is introduced due to Rt being switched to V_s every half cycle to charge Ct:

$$I_s \text{ due to } Rt = V_s/(4Rt)$$

Thus the supply current can be minimized by keeping Rt as large as possible (see supply current vs. operating frequency curves). However, the desired frequency will dictate an RtCt product such that increasing Rt will require a smaller Ct. Below Ct = 100 pF, circuit board stray capacitances begin to play a role in determining the oscillation frequency which ultimately limits the minimum Ct.

To allow for I.C. and component value tolerances, the oscillator timing components will require a trim. This is generally accomplished by using a variable resistor as part of Rt, although Ct could also be padded. The amount of initial frequency variation due to the LMC567 itself is given in the electrical specifications; the total trim range must also accommodate the tolerances of Rt and Ct.

SUPPLY DECOUPLING

The decoupling of supply pin 4 becomes more critical at high supply voltages with high operating frequencies, requiring C4 to be placed as close as possible to pin 4.

INPUT PIN

The input pin 3 is internally ground-referenced with a nominal 40 kΩ resistor. Signals which are already centered on 0V may be directly coupled to pin 3; however, any d.c. potential must be isolated via a coupling capacitor. Inputs of multiple LMC567 devices can be paralleled without individual d.c. isolation.

LOOP FILTER

Pin 2 is the combined output of the phase detector and control input of the VCO for the phase-locked loop (PLL). Capacitor C2 in conjunction with the nominal 80 kΩ pin 2 internal resistance forms the loop filter.

For small values of C2, the PLL will have a fast acquisition time and the pull-in range will be set by the built in VCO frequency stops, which also determine the largest detection bandwidth (LDBW). Increasing C2 results in improved noise immunity at the expense of acquisition time, and the pull-in range will begin to become narrower than the LDBW (see Bandwidth as a Function of C2 curve). However, the maximum hold-in range will always equal the LDBW.

OUTPUT FILTER

Pin 1 is the output of a negative-going amplitude detector which has a nominal 0 signal output of 7/9 V_s. When the PLL is locked to the input, an increase in signal level causes the detector output to move negative. When pin 1 reaches 2/3 V_s the output is activated (see OUTPUT PIN).

Capacitor C1 in conjunction with the nominal 40 kΩ pin 1 internal resistance forms the output filter. The size of C1 is a tradeoff between slew rate and carrier ripple at the output comparator. Low values of C1 produce the least delay between the input and output for tone burst applications, while larger values of C1 improve noise immunity.

Pin 1 also provides a means for shifting the input threshold higher or lower by connecting an external resistor to supply or ground. However, reducing the threshold using this technique increases sensitivity to pin 1 carrier ripple and also results in more part to part threshold variation.

OUTPUT PIN

The output at pin 8 is an N-channel FET switch to ground which is activated when the PLL is locked and the input tone is of sufficient amplitude to cause pin 1 to fall below 2/3 V_s. Apart from the obvious current component due to the external pin 8 load resistor, no additional supply current is required to activate the switch. The on resistance of the switch is inversely proportional to supply; thus the 'sat' voltage for a given output current will increase at lower supplies.