

LMC6064EP Precision CMOS Quad Micropower Operational Amplifier

Check for Samples: [LMC6064EP](#)

FEATURES

- (Typical Unless Otherwise Noted)
- Low offset voltage: 100 μ V
- Ultra low supply current: 16 μ A/Amplifier
- Operates from 4.5V to 15V single supply
- Ultra low input bias current: 10 fA
- Output swing within 10 mV of supply rail, 100k load
- Input common-mode range includes V^-
- High voltage gain: 140 dB

- Improved latchup immunity

APPLICATIONS

- Instrumentation amplifier
- Photodiode and infrared detector preamplifier
- Transducer amplifiers
- D/A converter
- Selected Military Applications
- Selected Avionics Applications

DESCRIPTION

The LMC6064EP is a precision quad low offset voltage, micropower operational amplifier, capable of precision single supply operation. Performance characteristics include ultra low input bias current, high voltage gain, rail-to-rail output swing, and an input common mode voltage range that includes ground. These features, plus its low power consumption make the LMC6064EP ideally suited for battery powered applications.

Other applications using the LMC6064EP include precision full-wave rectifiers, integrators, references, sample-and-hold circuits, and true instrumentation amplifiers.

This device is built with National's advanced double-Poly Silicon-Gate CMOS process.

For designs that require higher speed, see the LMC6084 precision quad operational amplifier.

For single or dual operational amplifier with similar features, see the LMC6061 or LMC6062 respectively.

ENHANCED PLASTIC

- Extended Temperature Performance of -40°C to $+85^{\circ}\text{C}$
- Baseline Control - Single Fab & Assembly Site
- Process Change Notification (PCN)
- Qualification & Reliability Data
- Solder (PbSn) Lead Finish is standard
- Enhanced Diminishing Manufacturing Sources (DMS) Support

PATENT PENDING



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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Connection Diagram

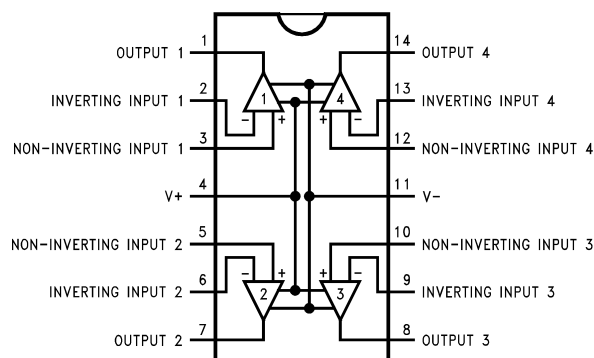


Figure 1. 14-Pin DIP/SO - Top View

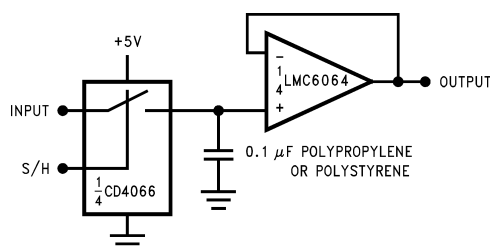


Figure 2. Low-Leakage Sample and Hold



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings ⁽¹⁾

Differential Input Voltage	±Supply Voltage
Voltage at Input/Output Pin	(V ⁺) +0.3V, (V ⁻) -0.3V
Supply Voltage (V ⁺ - V ⁻)	16V
Output Short Circuit to V ⁺	(2)
Output Short Circuit to V ⁻	(3)
Lead Temperature	
(Soldering, 10 sec.)	260°C
Storage Temp. Range	-65°C to +150°C
Junction Temperature	150°C
ESD Tolerance ⁽⁴⁾	2 kV
Current at Input Pin	±10 mA
Current at Output Pin	±30 mA
Current at Power Supply Pin	40 mA
Power Dissipation	(5)

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed.

(2) Do not connect output to V⁺, when V⁺ is greater than 13V or reliability will be adversely affected.

(3) Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C. Output currents in excess of ±30 mA over long term may adversely affect reliability.

(4) Human body model, 1.5 kΩ in series with 100 pF.

(5) The maximum power dissipation is a function of T_{J(Max)}, θ_{JA}, and T_A. The maximum allowable power dissipation at any ambient temperature is P_D = (T_{J(Max)} - T_A)/θ_{JA}.

Operating Ratings ⁽¹⁾

Temperature Range	
LMC6064AIEP, LMC6064IEP	$-40^{\circ}\text{C} \leq T_J \leq +85^{\circ}\text{C}$
Supply Voltage	$4.5\text{V} \leq V^+ \leq 15.5\text{V}$
Thermal Resistance (θ_{JA}) ⁽²⁾	
14-Pin Molded DIP	81°C/W
14-Pin SO	126°C/W
Power Dissipation	⁽³⁾

- (1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed.
- (2) All numbers apply for packages soldered directly into a PC board.
- (3) For operating at elevated temperatures the device must be derated based on the thermal resistance θ_{JA} with $P_D = (T_J - T_A) / \theta_{JA}$.

DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $T_J = 25^\circ\text{C}$. **Boldface** limits apply at the temperature extremes. $V^+ = 5\text{V}$, $V^- = 0\text{V}$, $V_{CM} = 1.5\text{V}$, $V_O = 2.5\text{V}$ and $R_L > 1\text{M}$ unless otherwise specified. ⁽¹⁾

				Typ	LMC6064AIEP	LMC6064IEP	
Symbol	Parameter	Conditions		(2)	Limit	Limit	Units
					(3)	(3)	
V _{OS}	Input Offset Voltage			100	350	800	μV
					900	1300	Max
TCV _{OS}	Input Offset Voltage			1.0			μV/°C
	Average Drift						
I _B	Input Bias Current			0.010			pA
					4	4	Max
I _{OS}	Input Offset Current			0.005			pA
					2	2	Max
R _{IN}	Input Resistance			>10			Tera Ω
CMRR	Common Mode	0V ≤ V _{CM} ≤ 12.0V		85	75	66	dB
	Rejection Ratio	V ⁺ = 15V			72	63	Min
+PSRR	Positive Power Supply	5V ≤ V ⁺ ≤ 15V		85	75	66	dB
	Rejection Ratio	V _O = 2.5V			72	63	Min
−PSRR	Negative Power Supply	0V ≤ V [−] ≤ −10V		100	84	74	dB
	Rejection Ratio				81	71	Min
V _{CM}	Input Common-Mode	V ⁺ = 5V and 15V		−0.4	−0.1	−0.1	V
	Voltage Range	for CMRR ≥ 60 dB			0	0	Max
				V ⁺ − 1.9	V ⁺ − 2.3	V ⁺ − 2.3	V
					V⁺ − 2.5	V⁺ − 2.5	Min
A _V	Large Signal	R _L = 100 kΩ ⁽⁴⁾	Sourcing	4000	400	300	V/mV
	Voltage Gain				300	200	Min
			Sinking	3000	180	90	V/mV
					100	60	Min
		R _L = 25 kΩ	Sourcing	3000	400	200	V/mV
		⁽⁴⁾			150	80	Min
			Sinking	2000	100	70	V/mV
					50	35	Min

(1) "Testing and other quality control techniques are used to the extent deemed necessary to ensure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific PARAMETRIC testing, product performance is assured by characterization and/or design."

(2) Typical values represent the most likely parametric norm.

(3) All limits are guaranteed by testing or statistical analysis.

(4) $V^+ = 15\text{V}$, $V_{CM} = 7.5\text{V}$ and R_L connected to 7.5V . For Sourcing tests, $7.5\text{V} \leq V_O \leq 11.5\text{V}$. For Sinking tests, $2.5\text{V} \leq V_O \leq 7.5\text{V}$.

DC Electrical Characteristics (continued)

Unless otherwise specified, all limits guaranteed for $T_J = 25^\circ\text{C}$. **Boldface** limits apply at the temperature extremes. $V^+ = 5\text{V}$, $V^- = 0\text{V}$, $V_{CM} = 1.5\text{V}$, $V_O = 2.5\text{V}$ and $R_L > 1\text{M}$ unless otherwise specified. ⁽¹⁾

Symbol	Parameter	Conditions	Typ (2)	LMC6064AIEP Limit (3)	LMC6064IEP Limit (3)	Units
V_O	Output Swing	$V^+ = 5\text{V}$	4.995	4.990	4.950	V
		$R_L = 100\text{ k}\Omega$ to 2.5V		4.980	4.925	Min
			0.005	0.010	0.050	V
				0.020	0.075	Max
		$V^+ = 5\text{V}$	4.990	4.975	4.950	V
		$R_L = 25\text{ k}\Omega$ to 2.5V		4.965	4.850	Min
			0.010	0.020	0.050	V
				0.035	0.150	Max
		$V^+ = 15\text{V}$	14.990	14.975	14.950	V
		$R_L = 100\text{ k}\Omega$ to 7.5V		14.965	14.925	Min
			0.010	0.025	0.050	V
				0.035	0.075	Max
		$V^+ = 15\text{V}$	14.965	14.900	14.850	V
		$R_L = 25\text{ k}\Omega$ to 7.5V		14.850	14.800	Min
			0.025	0.050	0.100	V
				0.150	0.200	Max
I_O	Output Current	Sourcing, $V_O = 0\text{V}$	22	16	13	mA
		$V^+ = 5\text{V}$		10	8	Min
		Sinking, $V_O = 5\text{V}$	21	16	16	mA
				8	8	Min
I_O	Output Current	Sourcing, $V_O = 0\text{V}$	25	15	15	mA
		$V^+ = 15\text{V}$		10	10	Min
		Sinking, $V_O = 13\text{V}$	26	20	20	mA
		⁽⁵⁾		8	8	Min
I_S	Supply Current	All Four Amplifiers	64	76	92	μA
		$V^+ = +5\text{V}$, $V_O = 1.5\text{V}$		92	112	Max
		All Four Amplifiers		94	114	μA
		$V^+ = +15\text{V}$, $V_O = 7.5\text{V}$	80	110	132	Max

(5) Do not connect output to V^+ , when V^+ is greater than 13V or reliability will be adversely affected.

AC Electrical Characteristics

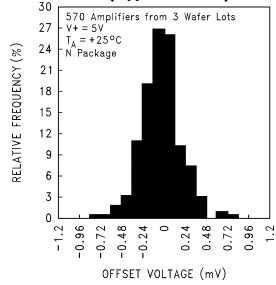
Unless otherwise specified, all limits guaranteed for $T_J = 25^\circ\text{C}$, **Boldface** limits apply at the temperature extremes. $V^+ = 5\text{V}$, $V^- = 0\text{V}$, $V_{CM} = 1.5\text{V}$, $V_O = 2.5\text{V}$ and $R_L > 1\text{M}$ unless otherwise specified. ⁽¹⁾

Symbol	Parameter	Conditions	Typ (2)	LMC6064AIEP Limit (3)	LMC6064IEP Limit (3)	Units
SR	Slew Rate	(4)	35	20	15	V/ms
				10	7	Min
GBW	Gain-Bandwidth Product		100			kHz
θ_m	Phase Margin		50			Deg
	Amp-to-Amp Isolation	(5)	155			dB
e_n	Input-Referred Voltage Noise	$F = 1\text{ kHz}$	83			$\frac{\text{nV}}{\sqrt{\text{Hz}}}$ (1)
i_n	Input-Referred Current Noise	$F = 1\text{ kHz}$	0.0002			$\frac{\text{pA}}{\sqrt{\text{Hz}}}$ (2)
T.H.D.	Total Harmonic Distortion	$F = 1\text{ kHz}$, $A_V = -5$				
		$R_L = 100\text{ k}\Omega$, $V_O = 2\text{ V}_{PP}$	0.01			%
		$\pm 5\text{V}$ Supply				

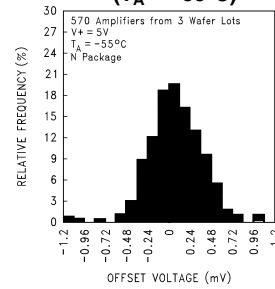
- (1) "Testing and other quality control techniques are used to the extent deemed necessary to ensure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific PARAMETRIC testing, product performance is assured by characterization and/or design."
- (2) Typical values represent the most likely parametric norm.
- (3) All limits are guaranteed by testing or statistical analysis.
- (4) $V^+ = 15\text{V}$. Connected as Voltage Follower with 10V step input. Number specified is the slower of the positive and negative slew rates.
- (5) Input referred $V^+ = 15\text{V}$ and $R_L = 100\text{ k}\Omega$ connected to 7.5V. Each amp excited in turn with 100 Hz to produce $V_O = 12\text{ V}_{PP}$.

Typical Performance Characteristics

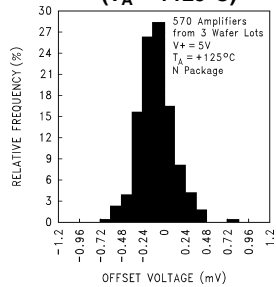
**Distribution of LMC6064AIMEP
Input Offset Voltage
($T_A = +25^\circ\text{C}$)**



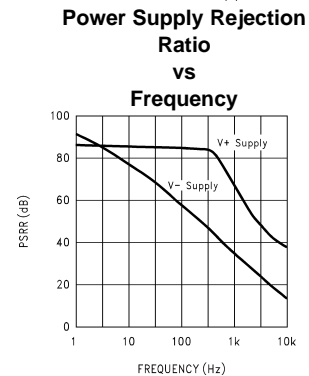
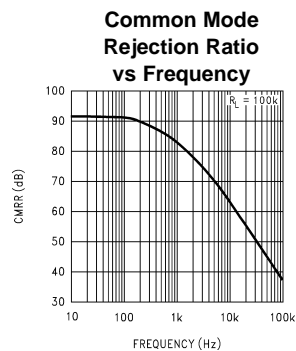
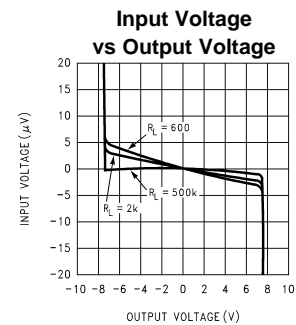
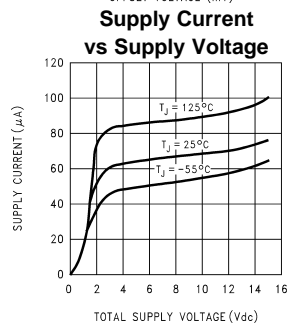
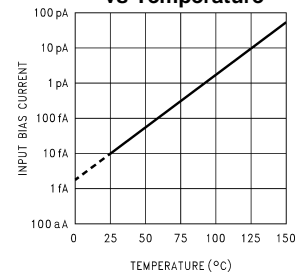
**Distribution of LMC6064AIMEP
Input Offset Voltage
($T_A = -55^\circ\text{C}$)**



**Distribution of LMC6064AIMEP
Input Offset Voltage
($T_A = +125^\circ\text{C}$)**

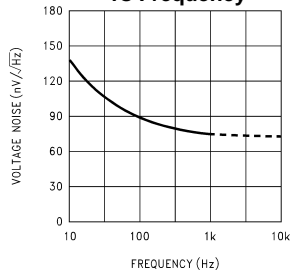


**Input Bias Current
vs Temperature**

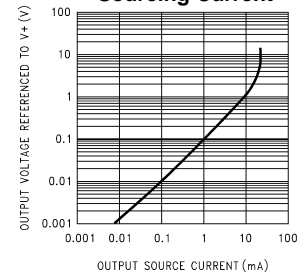


Typical Performance Characteristics (continued)

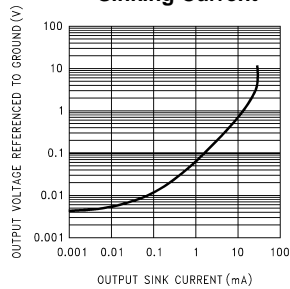
**Input Voltage Noise
vs Frequency**



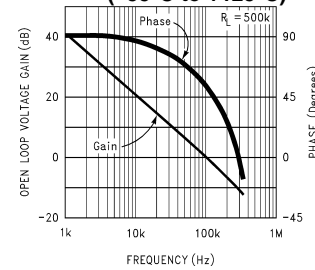
**Output Characteristics
Sourcing Current**



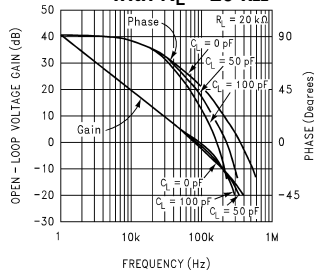
**Output Characteristics
Sinking Current**



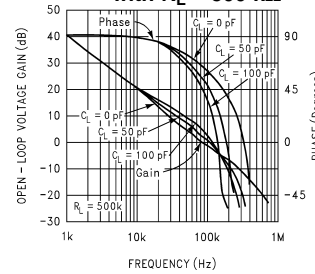
**Gain and Phase Response
vs Temperature
(-55°C to +125°C)**



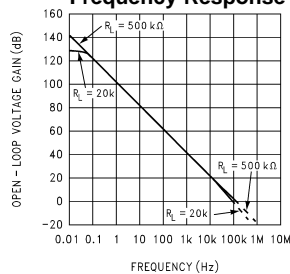
**Gain and Phase
Response
vs
Capacitive Load
with $R_L = 20\text{ k}\Omega$**



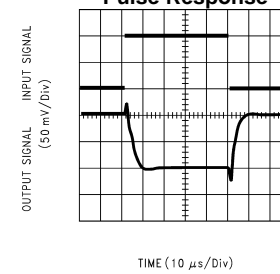
**Gain and Phase
Response
vs
Capacitive Load
with $R_L = 500\text{ k}\Omega$**



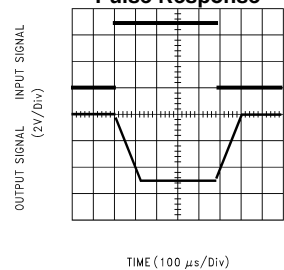
**Open Loop
Frequency Response**



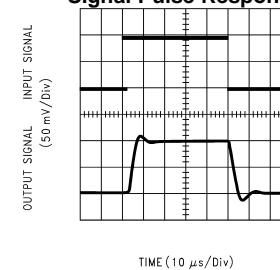
**Inverting Small Signal
Pulse Response**



**Inverting Large Signal
Pulse Response**

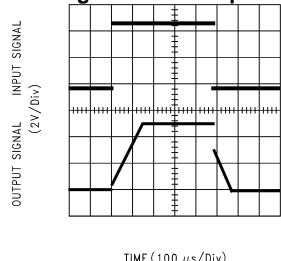


**Non-Inverting Small
Signal Pulse Response**



Typical Performance Characteristics (continued)

**Non-Inverting Large
Signal Pulse Response**

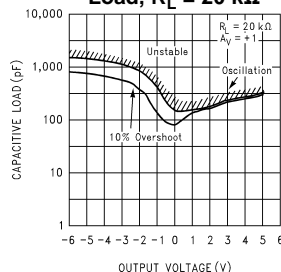


Stability

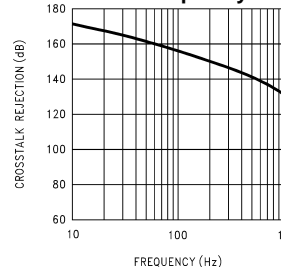
vs

Capacitive

Load, $R_L = 20\text{ k}\Omega$



**Crosstalk Rejection
vs Frequency**

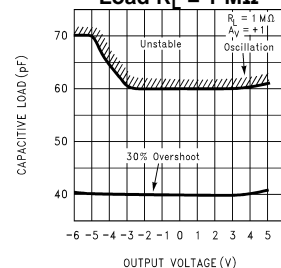


Stability

vs

Capacitive

Load $R_L = 1\text{ M}\Omega$



Applications Hints

AMPLIFIER TOPOLOGY

The LMC6064EP incorporates a novel op-amp design topology that enables it to maintain rail-to-rail output swing even when driving a large load. Instead of relying on a push-pull unity gain output buffer stage, the output stage is taken directly from the internal integrator, which provides both low output impedance and large gain. Special feed-forward compensation design techniques are incorporated to maintain stability over a wider range of operating conditions than traditional micropower op-amps. These features make the LMC6064EP both easier to design with, and provide higher speed than products typically found in this ultra-low power class.

COMPENSATING FOR INPUT CAPACITANCE

It is quite common to use large values of feedback resistance for amplifiers with ultra-low input current, like the LMC6064EP.

Although the LMC6064EP is highly stable over a wide range of operating conditions, certain precautions must be met to achieve the desired pulse response when a large feedback resistor is used. Large feedback resistors and even small values of input capacitance, due to transducers, photodiodes, and circuit board parasitics, reduce phase margins.

When high input impedances are demanded, guarding of the LMC6064EP is suggested. Guarding input lines will not only reduce leakage, but lowers stray input capacitance as well. (See **Printed-Circuit-Board Layout for High Impedance Work**).

The effect of input capacitance can be compensated for by adding a capacitor. Place a capacitor, C_f , around the feedback resistor (as in Figure 3) such that:

$$\frac{1}{2\pi R_1 C_{IN}} \geq \frac{1}{2\pi R_2 C_f} \quad (3)$$

$$\text{or} \quad (4)$$

$$R_1 C_{IN} \leq R_2 C_f \quad (5)$$

Since it is often difficult to know the exact value of C_{IN} , C_f can be experimentally adjusted so that the desired pulse response is achieved. Refer to the LMC660 and the LMC662 for a more detailed discussion on compensating for input capacitance.

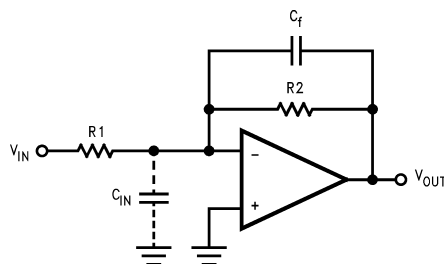


Figure 3. Canceling the Effect of Input Capacitance

CAPACITIVE LOAD TOLERANCE

All rail-to-rail output swing operational amplifiers have voltage gain in the output stage. A compensation capacitor is normally included in this integrator stage. The frequency location of the dominate pole is affected by the resistive load on the amplifier. Capacitive load driving capability can be optimized by using an appropriate resistive load in parallel with the capacitive load (see typical curves).

Direct capacitive loading will reduce the phase margin of many op-amps. A pole in the feedback loop is created by the combination of the op-amp's output impedance and the capacitive load. This pole induces phase lag at the unity-gain crossover frequency of the amplifier resulting in either an oscillatory or underdamped pulse response. With a few external components, op amps can easily indirectly drive capacitive loads, as shown in [Figure 4](#).

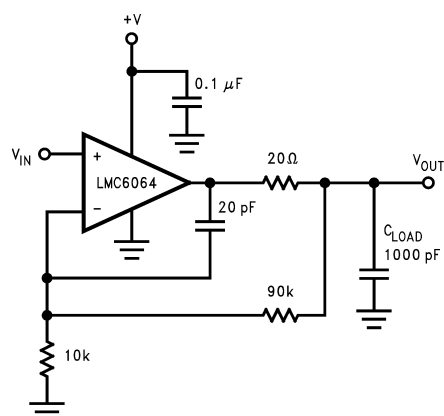


Figure 4. LMC6064EP Noninverting Gain of 10 Amplifier, Compensated to Handle Capacitive Loads

In the circuit of [Figure 4](#), R1 and C1 serve to counteract the loss of phase margin by feeding the high frequency component of the output signal back to the amplifier's inverting input, thereby preserving phase margin in the overall feedback loop.

Capacitive load driving capability is enhanced by using a pull up resistor to V⁺ ([Figure 5](#)). Typically a pull up resistor conducting 10 μA or more will significantly improve capacitive load responses. The value of the pull up resistor must be determined based on the current sinking capability of the amplifier with respect to the desired output swing. Open loop gain of the amplifier can also be affected by the pull up resistor (see Electrical Characteristics).

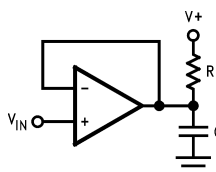


Figure 5. Compensating for Large Capacitive Loads with a Pull Up Resistor

PRINTED-CIRCUIT-BOARD LAYOUT FOR HIGH-IMPEDANCE WORK

It is generally recognized that any circuit which must operate with less than 1000 pA of leakage current requires special layout of the PC board. When one wishes to take advantage of the ultra-low bias current of the LMC6064EP, typically less than 10 fA, it is essential to have an excellent layout. Fortunately, the techniques of obtaining low leakages are quite simple. First, the user must not ignore the surface leakage of the PC board, even though it may sometimes appear acceptably low, because under conditions of high humidity or dust or contamination, the surface leakage will be appreciable.

To minimize the effect of any surface leakage, lay out a ring of foil completely surrounding the LMC6064EP's inputs and the terminals of capacitors, diodes, conductors, resistors, relay terminals etc. connected to the op-amp's inputs, as in Figure 6. To have a significant effect, guard rings should be placed on both the top and bottom of the PC board. This PC foil must then be connected to a voltage which is at the same voltage as the amplifier inputs, since no leakage current can flow between two points at the same potential. For example, a PC board trace-to-pad resistance of $10^{12}\Omega$, which is normally considered a very large resistance, could leak 5 pA if the trace were a 5V bus adjacent to the pad of the input. This would cause a 100 times degradation from the LMC6064EP's actual performance. However, if a guard ring is held within 5 mV of the inputs, then even a resistance of $10^{11}\Omega$ would cause only 0.05 pA of leakage current. See Figure 9 for typical connections of guard rings for standard op-amp configurations.

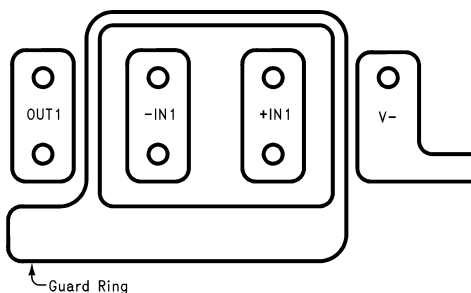


Figure 6. Example of Guard Ring in P.C. Board Layout

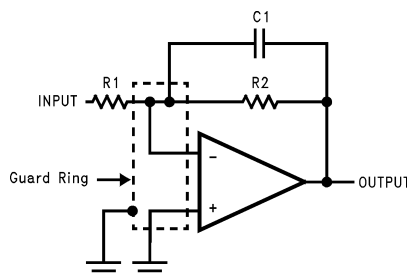


Figure 7. Inverting Amplifier

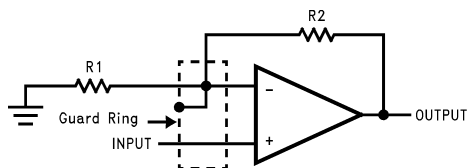
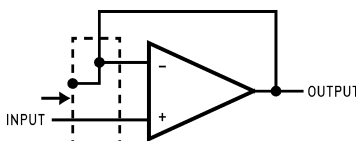


Figure 8. Non-Inverting Amplifier



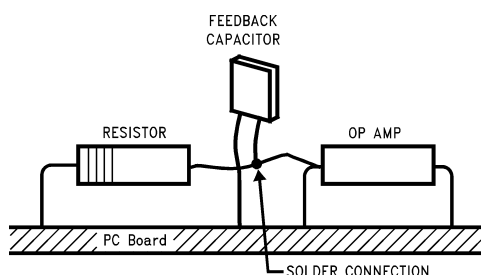
Follower

Figure 9. Typical Connections of Guard Rings

The designer should be aware that when it is inappropriate to lay out a PC board for the sake of just a few circuits, there is another technique which is even better than a guard ring on a PC board: Don't insert the amplifier's input pin into the board at all, but bend it up in the air and use only air as an insulator. Air is an excellent insulator. In this case you may have to forego some of the advantages of PC board construction, but the advantages are sometimes well worth the effort of using point-to-point up-in-the-air wiring. See [Figure 10](#).

Latchup

CMOS devices tend to be susceptible to latchup due to their internal parasitic SCR effects. The (I/O) input and output pins look similar to the gate of the SCR. There is a minimum current required to trigger the SCR gate lead. The LMC6064EP and LMC6082 are designed to withstand 100 mA surge current on the I/O pins. Some resistive method should be used to isolate any capacitance from supplying excess current to the I/O pins. In addition, like an SCR, there is a minimum holding current for any latchup mode. Limiting current to the supply pins will also inhibit latchup susceptibility.



(Input pins are lifted out of PC board and soldered directly to components. All other pins connected to PC board).

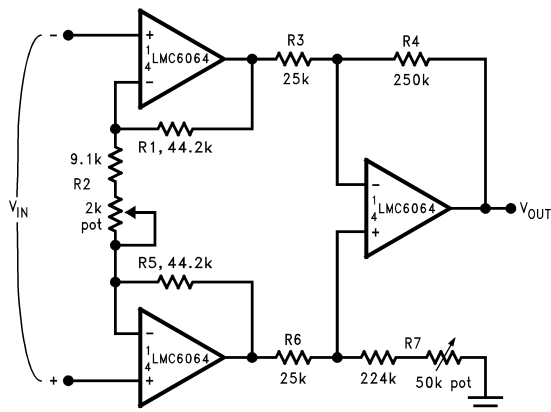
Figure 10. Air Wiring

Typical Single-Supply Applications

($V^+ = 5.0 V_{DC}$)

The extremely high input impedance, and low power consumption, of the LMC6064EP make it ideal for applications that require battery-powered instrumentation amplifiers. Examples of these types of applications are hand-held pH probes, analytic medical instruments, magnetic field detectors, gas detectors, and silicon based pressure transducers.

[Figure 11](#) shows an instrumentation amplifier that features high differential and common mode input resistance ($>10^{14}\Omega$), 0.01% gain accuracy at $A_V = 100$, excellent CMRR with 1 k Ω imbalance in bridge source resistance. Input current is less than 100 fA and offset drift is less than 2.5 $\mu V/^\circ C$. R_2 provides a simple means of adjusting gain over a wide range without degrading CMRR. R_7 is an initial trim used to maximize CMRR without using super precision matched resistors. For good CMRR over temperature, low drift resistors should be used.



If $R_1 = R_5$, $R_3 = R_6$, and $R_4 = R_7$; then

$$\frac{V_{OUT}}{V_{IN}} = \frac{R_2 + 2R_1}{R_2} \times \frac{R_4}{R_3}$$

$\therefore A_V \approx 100$ for circuit shown ($R_2 = 9.822k$).

Figure 11. Instrumentation Amplifier

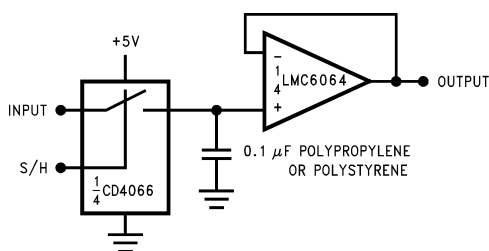


Figure 12. Low-Leakage Sample and Hold

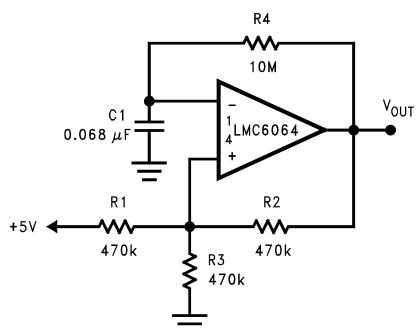


Figure 13. 1 Hz Square Wave Oscillator

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